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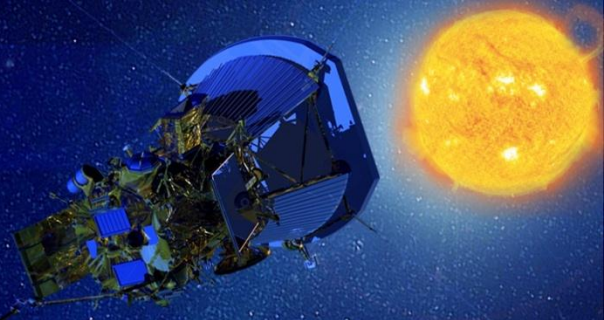

SPP Spacecraft Emulator (SCE)
Full Emulator
Design/Schematic Peer Review

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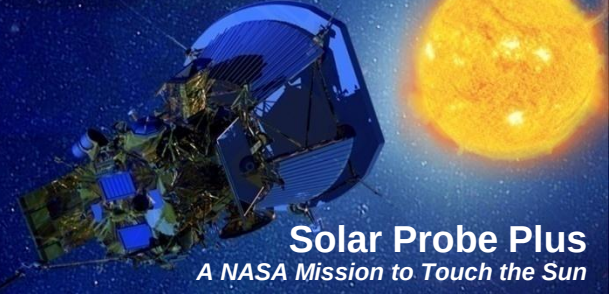
January 31, 2014

APL
The Johns Hopkins University
APPLIED PHYSICS LABORATORY

Agenda



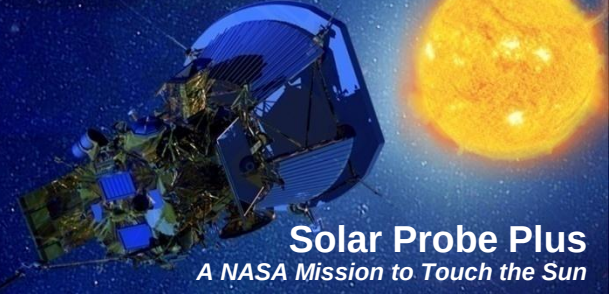
- Timeline (Emulator Development)
  - Purpose of Review
  - Deliverables
  - Status
- SPP Full-Emulator Overview
  - Electrical Block Diagram
  - Box Front/Rear Panel Diagram
- SPP Full-Emulator Updates (From RBSP Design)
- First Circuits
- SC Emulator Requirement Review: Action Item Review
- Schematic Review
  - PWA Preliminary Layout/Power Estimate/Part Change Summary
- Conclusion
- Backup

Timeline (Emulator Development)

- **FEB 2013** — SCE Emulator Intro Review w/Instrument Teams
- **APR 2013** — Mini Emulator Schematic Review
- **JUN-AUG 2013** — Mini Emulators Delivered to Instrument Teams
  - Included GSEOS UART SW Only, No SpW SW
- **JUN 2013** — SC Emulator Requirements Peer Review
- **NOV 2013** — Started Full Emulator Design

- **JAN 2014** — Full Emulator Schematic Peer Review
- **FEB 2014** — Layout Full Emulator PWB
- **FEB 2014** — Mini Emulator Space Wire Code Test/Delivery
- **MAR 2014** — SCE EDR/PDR (FINAL)
- **APR-MAY 2014** — Full Emulator Deliveries
- **JUN–DEC 2014** — Support of Full Emulator Deliveries

Purpose of Review



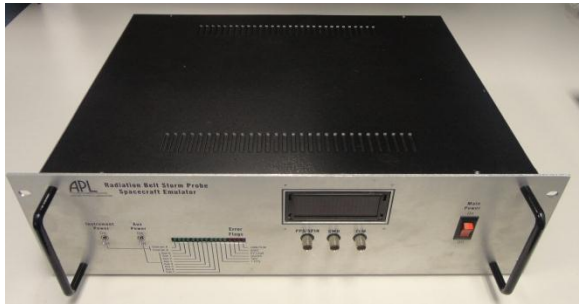
- **Primary Purpose:**
  - **Review FULL Emulator design, specifically those related to physical interfaces to the instrument**
    - **SC Emulator Requirements Review was held in June 2013, this is last chance to review design before fabbing hardware (Full EDR scheduled for March 2014)**
  - **APL Independent Reviews**
    - **RBSP Emulator Lead**
      - **Joe Sheehi**
    - **SPP Avionics HW/SW GSE Leads**
      - **Taylor Green**
      - **Dave Stott**
      - **Kyle Weber**
      - **Andrew Harris**

Emulator Deliverables

- **Full-Emulator earliest Instrument delivery is in April 2014, last Delivery in May 2014. (All Mini Emulators Delivered)**

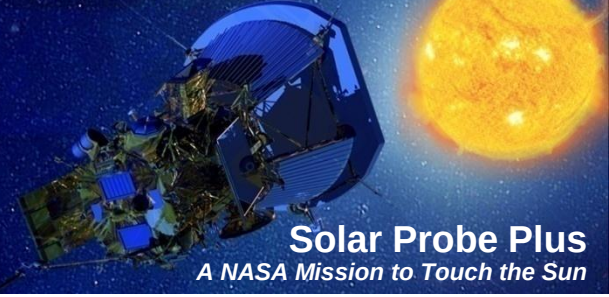
	Total QTY	FIELDS	WISPR	ISIS	SWEAP	Project Spares
Mini-Emulators	14	4	2	3	3	2
Full Emulators	11	2	2	3	2	2

- **Development units, 3 Mini's and 1 Full**



REF: RBSP Full Emulator

Emulator Status



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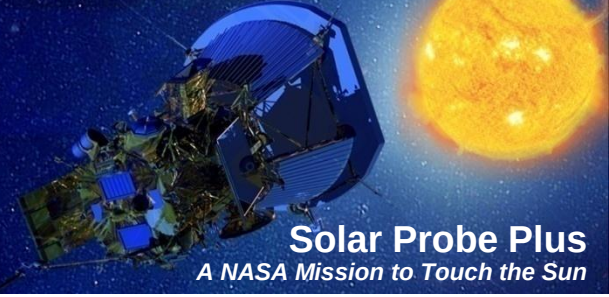
- **Mini Emulator Status**
  - **All Mini Emulators Delivered to Instrument Teams**
  - **GSEOS Software Status**
    - **Several UART/GSEOS Releases as follows:**
    - **UART Version:**
      - **Version: SPP.2.3.008 was released on 7/3/13**
      - **Version: SPP.2.3.012 was released on 7/28/13**
        - **Fix Endian Issues, Update Screens menus, Secondary Header updates**
      - **Version: SPP.3.1.015 was released on 11/16/13**
        - **Fixed Start up problem also includes New ITF Frame and Linux OS update.**
      - **Version: SPP.3.1.019 was limited released on 1/17/14 to FIELDS only**
        - **Fixed GSEOS self test issues.**
        - **Fixed high speed/high load transfers (not seen on SPP Emulators)**
        - **Removed the limit check on setting the UART baud rates. (ie supports 345.6 Kbaud rate)**
        - **Also removes old FPGA bit files, so users do not load in the old FPGA bit files**
    - **SpaceWire Version:**
      - **GSEOS Release Final version by FEB 28, 2014; Basic Spacewire version is available now**
- **Full Emulator Status**
  - **Schematic Done.**
  - **EPL Done for PWA and Box, Box Mechanical PL in work.**
  - **Box Wiring Diagram Done.**
  - **Front/Rear Panel Mech Design –in work.**
  - **Parts Order – in work**
    - **Long Lead parts have been ordered; includes FETS and Aeroflex LVDS parts**

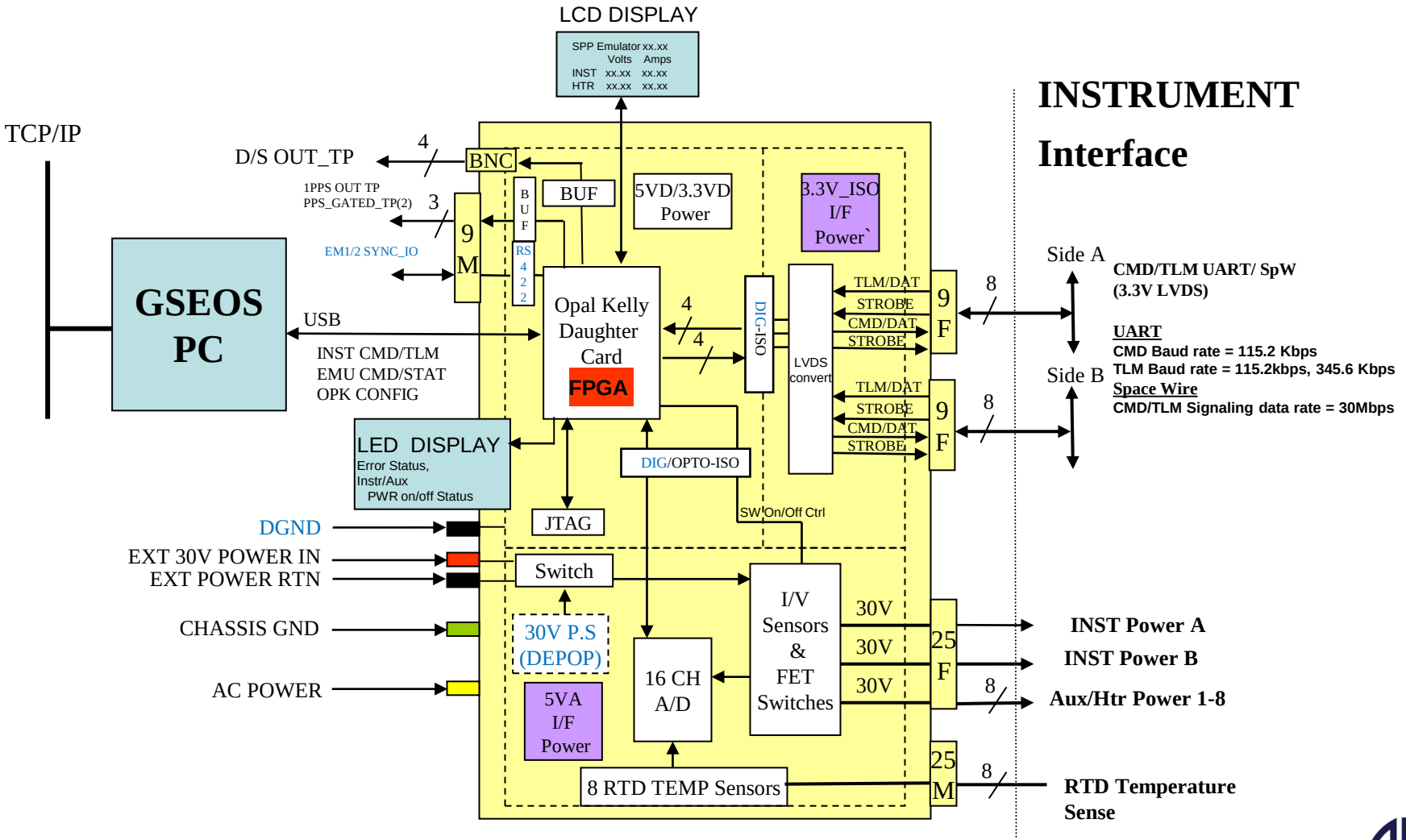
SCE Full-Emulator Overview



- SPP Full Emulator Design is based on the RBSP Full Emulator with modifications
- Provides the following Instrument Interfaces:
  - Instrument Data: UART/Spacewire (A/B)
  - Power Services Outputs (2 Instrument/8 Auxiliary)
  - RTD Temperature Interfaces
    - 8 Total
      - Narrow (-100C to 100C)
      - Wide (-175C to 200C)
        - Temp Range-HW selectable
- Also provides 1PPS and Gated_PPS Test Point EGSE Interfaces
  - Also provide Emulator Sync between 2 Emulators (for FIELDS1/2)
- GSEOS Interface is fully compliant
- Designed for use with Flight hardware
  - Requires External 30V Bus Power Supply for Power Services
    - 30V Internal Supply No longer Provided

REF: RBSP Full Emulator

Full-Emulator Block Diagram



SCE Full-Emulator Block Diagram

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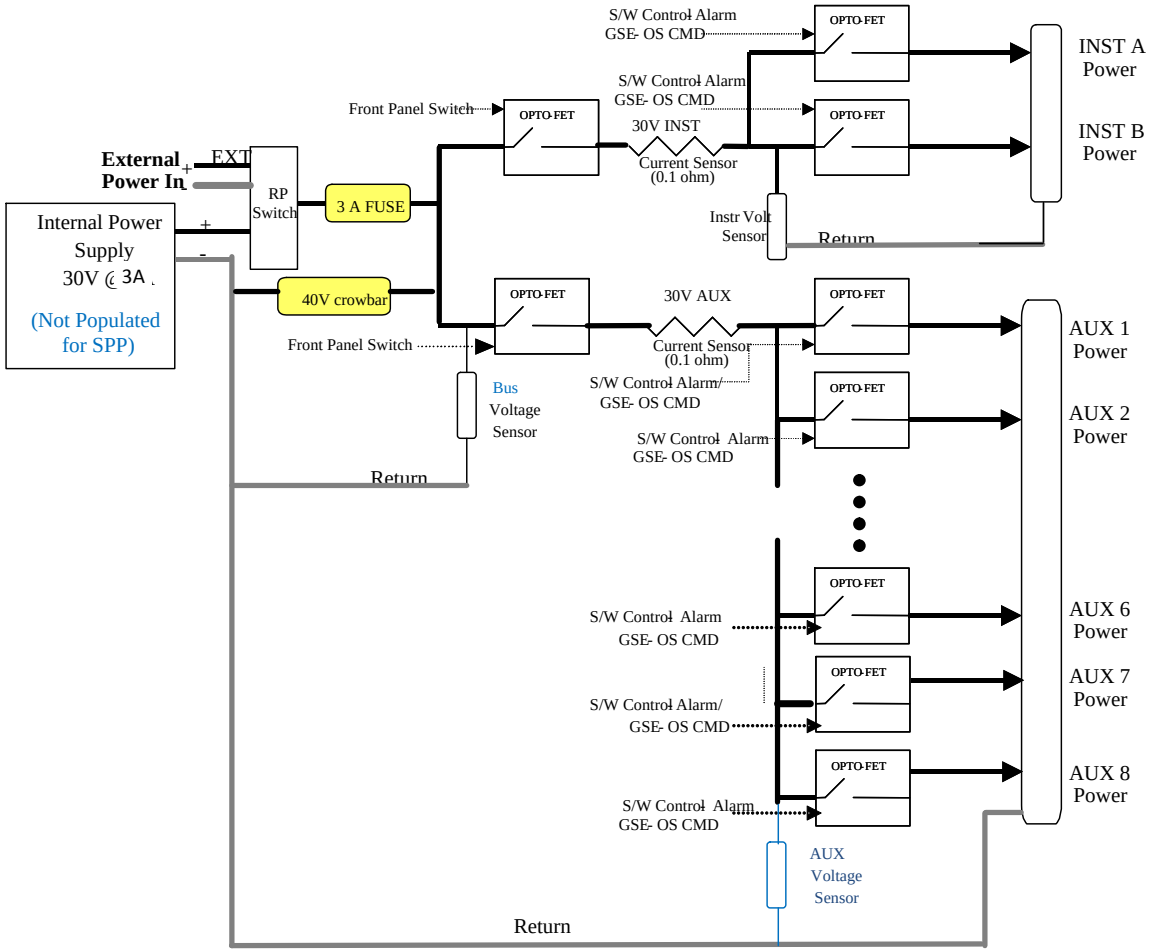
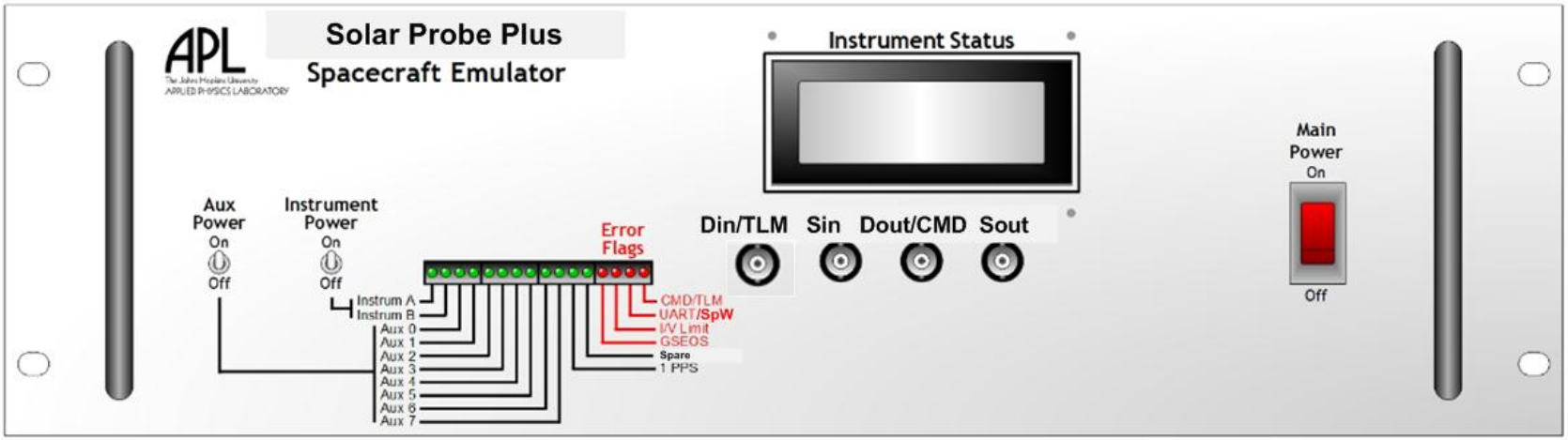
- **Full Emulator Instrument Power Interfaces (Detailed Block Diagram)**



SCE Full-Emulator

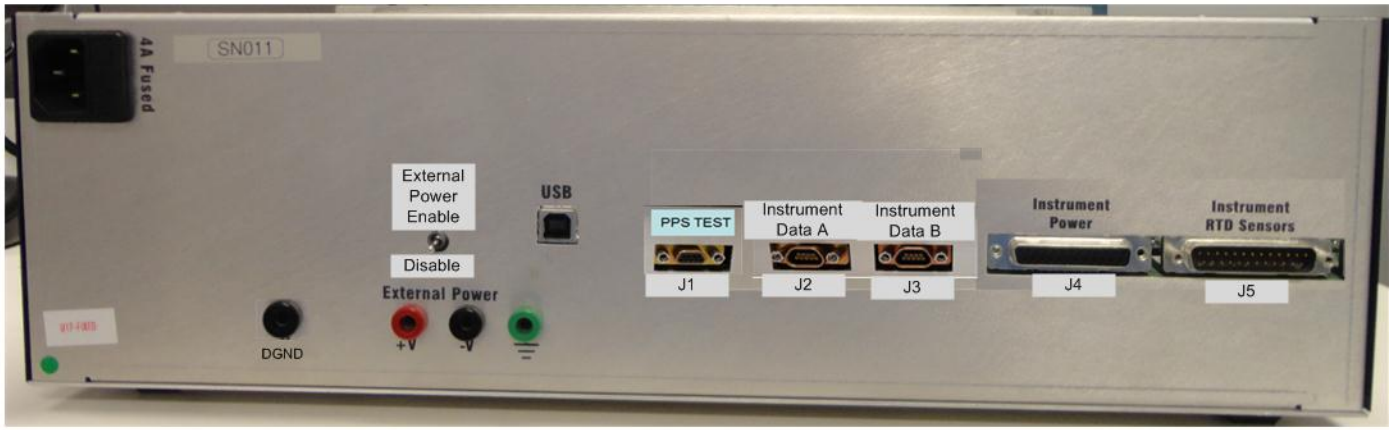
- **Full Emulator Front Panel LED/LCD Interface/BNC TP Interface**



- **Note: The 2 switches above enable the Aux and Instrument Power Buses. Individual Instrument and Aux power outputs are Software controlled on/off.**
  - **Front Panel D/S Test points: BNC**

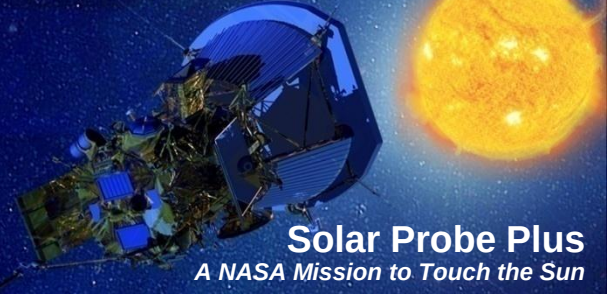
SCE Full-Emulator

- **Full Emulator Rear Panel Interface**



- **Note: The switch above enables the External Power input.**
  - **Data connectors are female MDMs (9F)**
  - **PPS/Emulator Sync test connector is male MDM (9M)**
  - **Instrument Power connector is female DSUB 20AWG (25F)**
  - **Instrument RTD connector is male DSUB 20AWG (25M)**
  - **External Power Supply IF: Banana Jacks**

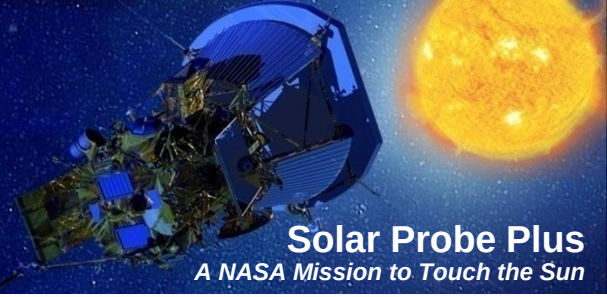
SPP SC Emulator Updates from RBSP



Note: SC Emulator Requirements are documented in 7434-7001

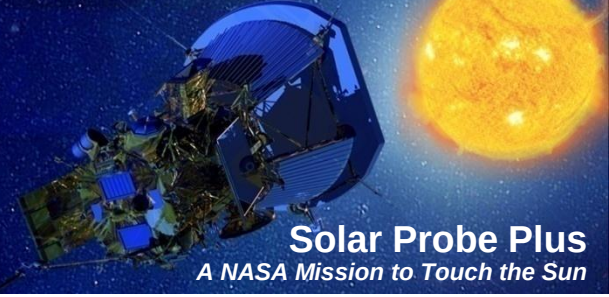
- Update Requirements to SPP General Instrument ICD and SpW ICD for WISPR DPU
  - Provide A/B UART interfaces (115.2K BAUD)
    - Also support 345.6K BAUD Telemetry link from FIELDS and SWEAP
    - Support Virtual PPS (no distinct 1PPS line)
  - Provide A/B SpW link (30 MHz Signaling rate) with configurable SpW bus schedule
    - RBSP only provided non-redundant UART (<345.6K Baud) interface
- GSEOS version 7 will be used for SPP
- Full-Emulators will have 2 gated-PPS test outputs with GSEOS command for arm/disarm/one-shot with programmable pulse width and delay from PPS. In addition to 1 PPS output. (RBSP only provided 1PPS TP)
- Full-Emulators will have Sync Capability to Synchronize virtual 1 PPS timing between 2 Emulators (for FIELDS1/2 Emulators)
- Full Emulators RTD Temp Interface will provide Narrow/Wide RTD Compatibility (RBSP only provided Narrow RTD Compatibility)
- SCE data connectors will be female MDMs, PPS/Sync Test Connector will be Male MDM.

SPP SC Emulator
Updates from RBSP

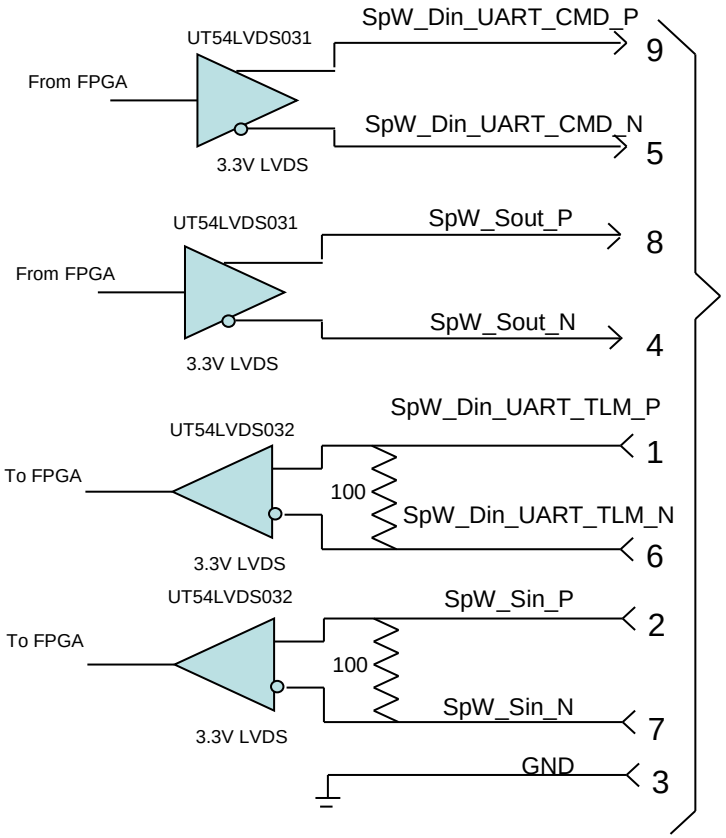


- 5V Power no loner supplied thru USB interface. Internal 5V supply used for Full.
- GSEOS SW verified compatibility with GPIB Drivers, but requires Ext HW supplied by Instrument Team (eg USB/GPIB converter)
- Spacewire RMAP (Remote Memory Access Protocol) will be Implemented in Embedded SW
- GSEOS compatible with Linux in addition to Windows-7 (Recently added)
- Removed 30V Internal Power Supply, since not compatible for flight testing. Users will provide External Power supply input.
- LVDS
  - Use nonflight (flight like) Aeroflex LVDS Parts (vs Fairchild commerical parts)-Program office Risk Decision.
  - Provide Separate LVDS IC packages for Side A and Side B interfaces in order to control Tri-state/off condition of inactive side.

SPP SC FULL Emulator
First Circuit Interfaces



First Circuit Interface (UART/Spacewire)



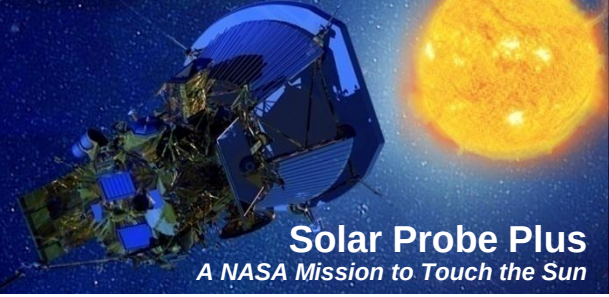
INSTRUMENT INTERFACE

MDM9-FEMALE (J2, J3)
(Separate Connectors for Side A & Side B)
(mating connector is male)

Note: * = SpaceWire Strobe Signals
(Sin/Sout are not used for UART Interfaces)

Connector PN: M83513-13-A01CP (Right Angle)
(Glenair/Mouser)

SPP SC FULL Emulator
First Circuit Interfaces



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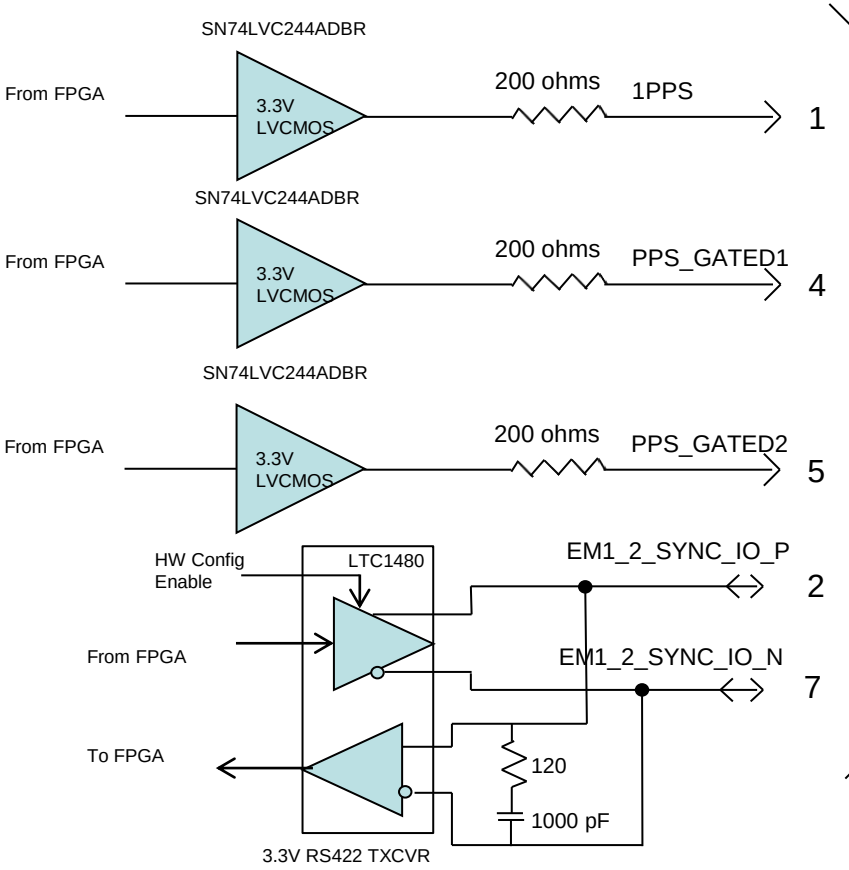
First Circuit Interface (PPS TEST/EM_SYNC -EGSE I/F)



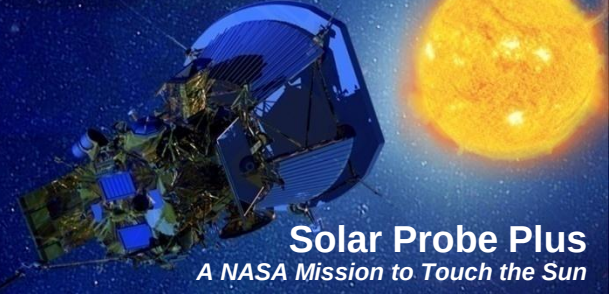
INSTRUMENT EGSE INTERFACE

MDM9-MALE (J1)
(mating connector is female)
Connector PN: M83513-10-A01CP (Right Angle)
(Glenair/Mouser)

Pins:3,6,8,9: Ground

For FIELDS1/2 ONLY:
For FIELDS 1: SYNC = OUTPUT
For FIELDS 2: SYNC = INPUT

SPP SC FULL Emulator
First Circuit Interfaces



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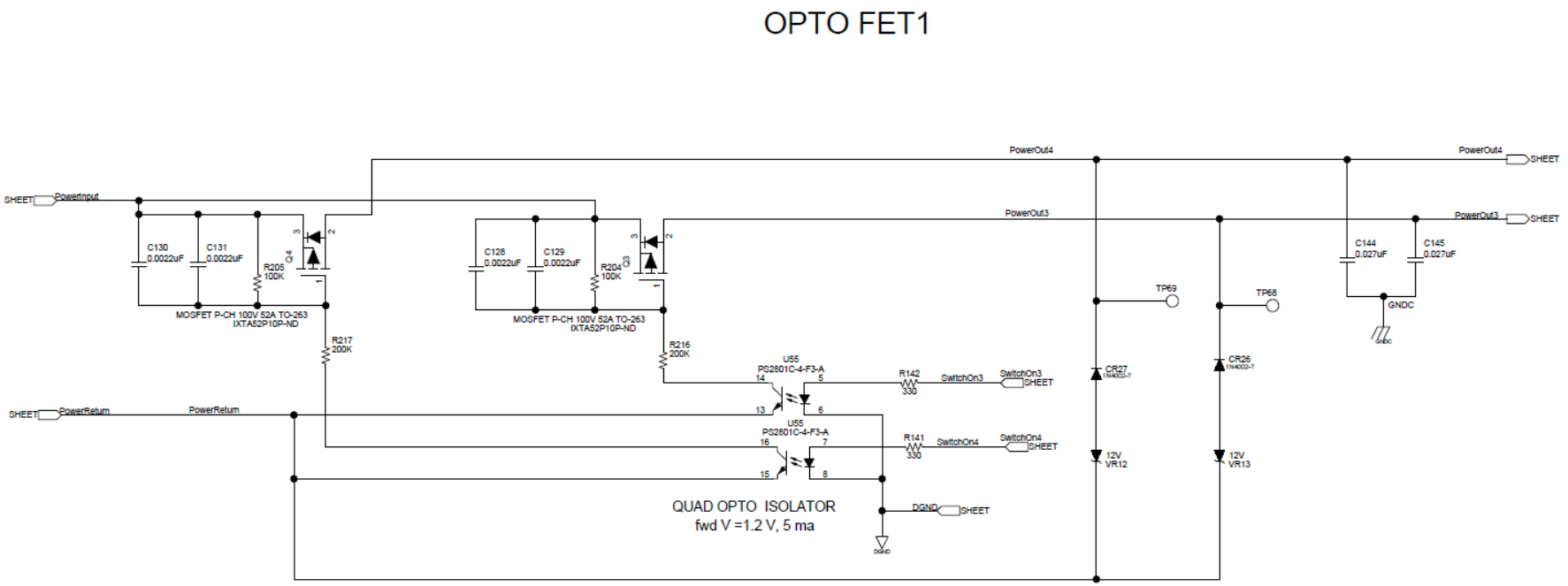
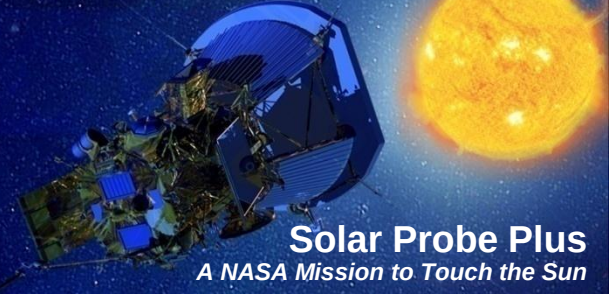
First Circuit Interface (Instr/Aux Power Outputs)



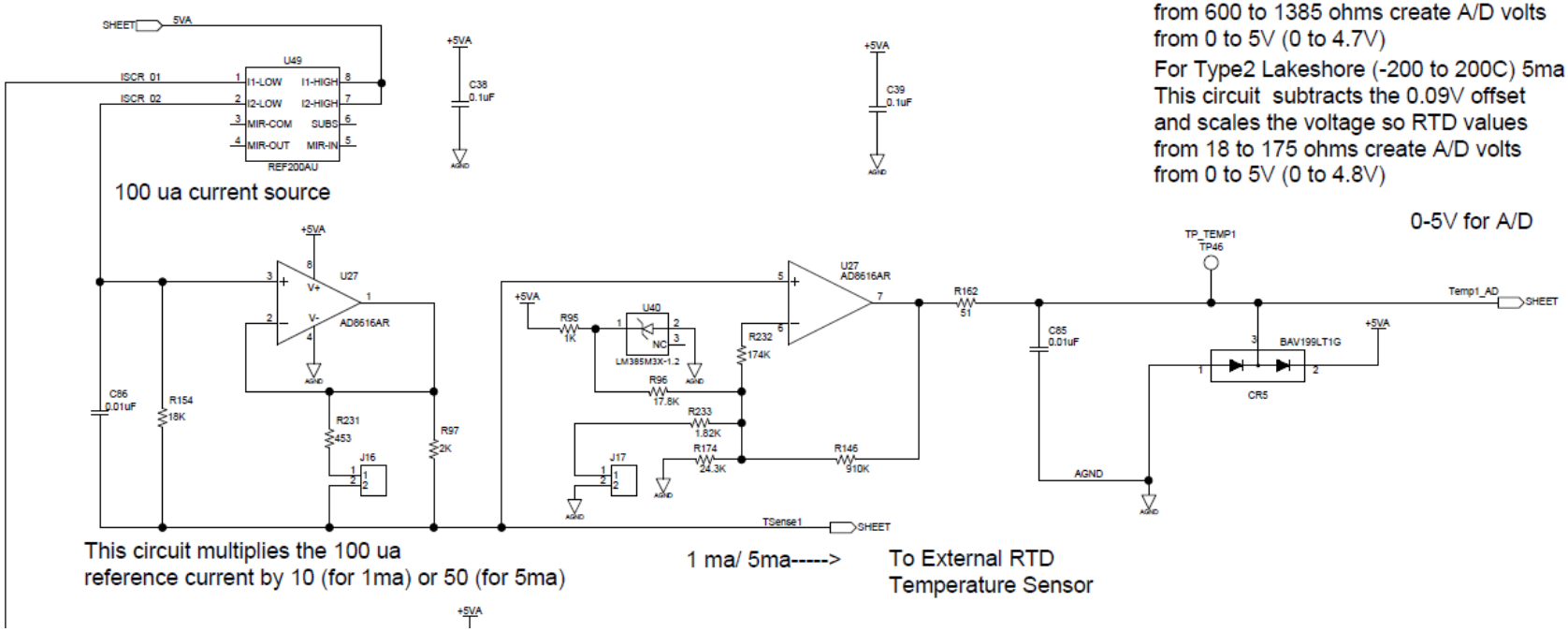
SPP SC FULL Emulator
First Circuit Interfaces



First Circuit Interface (RTD Temp)

RTD SENSE 0

Precision 100 uA Current Source



For Type1 Minco (-100C to 100C) 1ma Case:
This circuit subtracts the 0.6V offset
and scales the voltage so RTD values
from 600 to 1385 ohms create A/D volts
from 0 to 5V (0 to 4.7V)

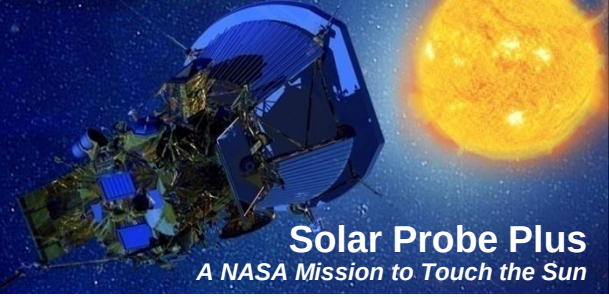
For Type2 Lakeshore (-200 to 200C) 5ma Case:
This circuit subtracts the 0.09V offset
and scales the voltage so RTD values
from 18 to 175 ohms create A/D volts
from 0 to 5V (0 to 4.8V)

0-5V for A/D

This circuit multiplies the 100 ua
reference current by 10 (for 1ma) or 50 (for 5ma)

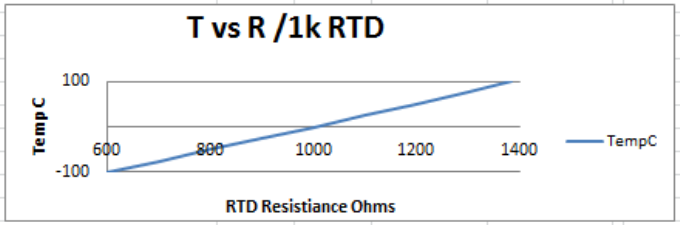
1 ma/ 5ma-----> To External RTD
Temperature Sensor

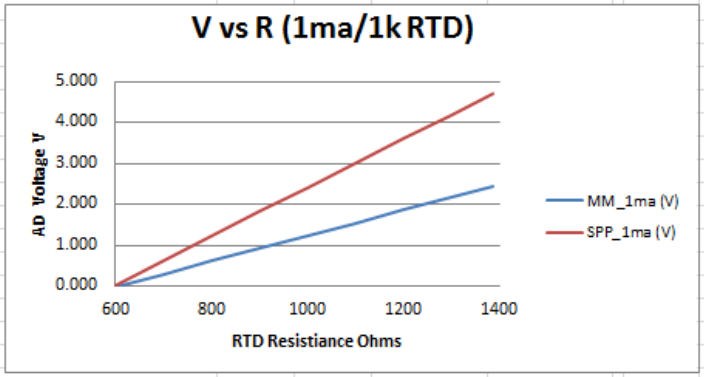
SPP SC FULL Emulator
First Circuit Interfaces



Preliminary RTD PSPICE Simulation Results:

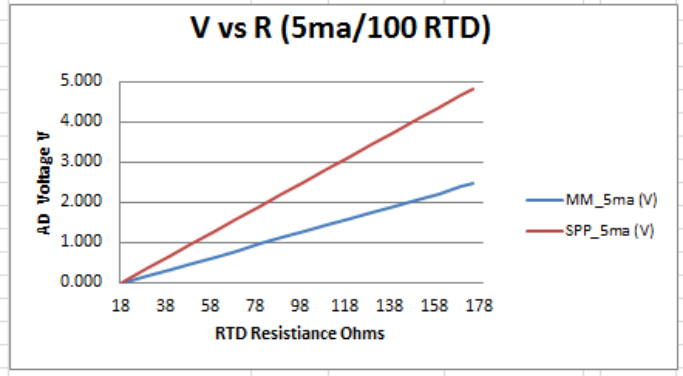
Temp RTD MarK Martin vs SPP			1ma Current Source/1k RTD		
	R(ohms)	TempC	MM_1ma (V)	SPP_1ma (V)	=SPP/2
RTD Resistance 1K nom	600	-100	0.001	0.042	0.021
RTD Resistance 1K nom	700	-75	0.306	0.636	0.318
RTD Resistance 1K nom	800	-50	0.618	1.230	0.615
RTD Resistance 1K nom	900	-25	0.931	1.824	0.912
RTD Resistance 1K nom	1000	0	1.243	2.418	1.209
RTD Resistance 1K nom	1100	25	1.555	3.011	1.5055
RTD Resistance 1K nom	1200	52	1.867	3.605	1.8025
RTD Resistance 1K nom	1300	77	2.180	4.195	2.0975
RTD Resistance 1K nom	1385	100	2.445	4.704	2.352



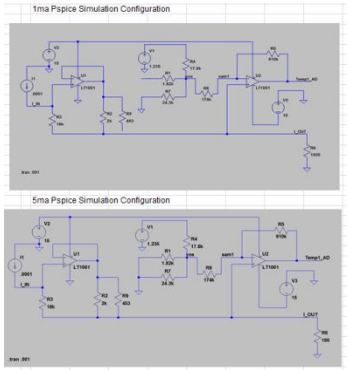


Nominal current: 1mA (+/-.2%)

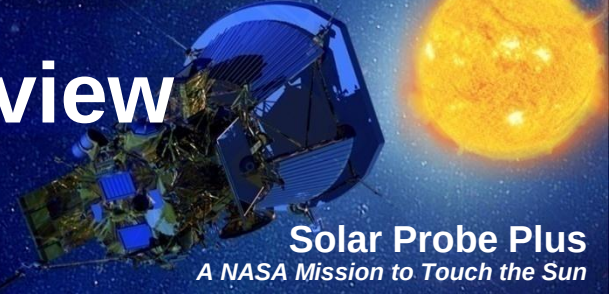
			5ma Current Source/ 100 RTD		
	R(ohms)	MM_5ma (V)	SPP_5ma (V)	=SPP/2	
RTD Resistance 100 nom	18	0.001	0.000	0.0002	
RTD Resistance 100 nom	20	0.031	0.059	0.0295	
RTD Resistance 100 nom	30	0.189	0.366	0.183	
RTD Resistance 100 nom	40	0.347	0.674	0.337	
RTD Resistance 100 nom	50	0.504	0.981	0.4905	
RTD Resistance 100 nom	60	0.662	1.289	0.6445	
RTD Resistance 100 nom	70	0.819	1.596	0.798	
RTD Resistance 100 nom	80	0.977	1.904	0.952	
RTD Resistance 100 nom	90	1.135	2.211	1.1055	
RTD Resistance 100 nom	100	1.292	2.519	1.2595	
RTD Resistance 100 nom	110	1.450	2.826	1.413	
RTD Resistance 100 nom	120	1.607	3.134	1.567	
RTD Resistance 100 nom	130	1.765	3.442	1.721	
RTD Resistance 100 nom	140	1.922	3.749	1.8745	
RTD Resistance 100 nom	150	2.080	4.057	2.0285	
RTD Resistance 100 nom	160	2.237	4.364	2.182	
RTD Resistance 100 nom	170	2.395	4.672	2.336	
RTD Resistance 100 nom	175	2.473	4.820	2.41	



Nominal current: 4.973mA (+/-.2%) (-0.54%)



SC Emulator Requirements Review
Action Item Review



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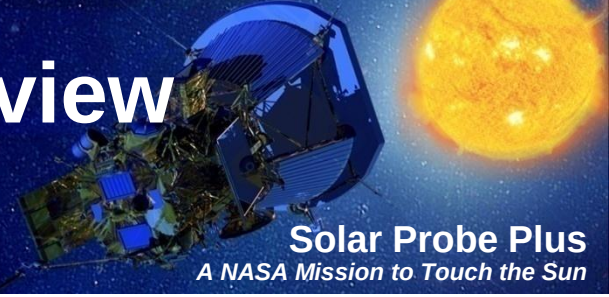
8 Action Items: 4 closed, 4 in work (3 non HW related issues).

Number	Title	Originator	Assignee	Due Date	Response
1	Opto-Isolator may not preserve SpaceWire signal wave shape at 30 MHz. 1. Test signal quality at 30Mbit/sec 2. Determine Margin 3. Consider elimination of Opto Isolation (Pg 18: Sec 2.9, Fig 13)	D. Stott	S. Sawada	Full Emulator Board EDR	**12/5/13: Will use Digital Isolator which is good for signals up to 150 Mbps.— Issue Closed.**
2	Consider adding RMAP protocol errors: 1. Invalid Protocol ID 2. Invalid Key 3. Invalid Header CRC (Pg 16: Sec 2.6)	A. Harris	H. Eaton S. Sawada	7/31/13	Status 7/18/13: Per Harry, he will consider adding. 10/10/13: Harry presently working on basic R/W function. Will add error checking next. Thomas will need to add the error checking counts in GSEOS. **12/5/13: Harry was going to add a single catch all error that reports when errors occurred, but Thomas recommend to add separate counters. Harry agreed to add 6 separate counters to capture RMAP errors. Will make error block larger.** **1/16/14: Done, Design has been updated. Need to update the Req Doc (Action: Harry)**

SC Emulator Requirements Review
Action Item Review



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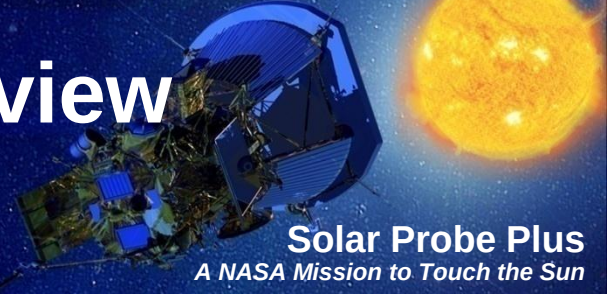
Number	Title	Originator	Assignee	Due Date	Response
3	Side Switching from one REM to the other should be supported/tested. Both REMs may be powered, one connected and the other in "auto start" mode, sending NULLs. The Emulator should have two SpW nodes (or equivalent) to allow simulation/test of this. REM A / REM B • Powered/Connected / Unpowered ↓ ↓ • Powered/Connected / Powered/Autostart ↓ ↓ • Powered/Disconnected / Powered/Connected ↓ ↓ • Unpowered / Powered/Connected (Pg 8: Sec 2.1.6.1 & Pg 16: Sec 2.5)	A. Mick	D. Wenstrand	7/31/13	Status 7/18/13: Per Harry, Doug checking to see if 2 SpW Nodes will fit in FPGA.
4	Moved to Comment number 29	NA	NA	NA	
5	Active vs Inactive SpW Interface • There are several valid SpW REM A vs B configurations (powered, connected, etc) that the spacecraft may present to the instrument. Please ensure that all valid conditions/states between the two sides may be emulated. • In particular, the unused node may be powered on and sending NULLs, waiting for the other side to respond. This is the "autostart" mode, and is specified in the SpW ICD under the router configuration. (Pg 8: Sec 2.1.6.1)	A. Mick	D. Wenstrand H. Eaton S. Sawada	7/31/13	Status 7/18/13: Can support this if Action item 3 can be implemented.

SC Emulator Requirements Review
Action Item Review



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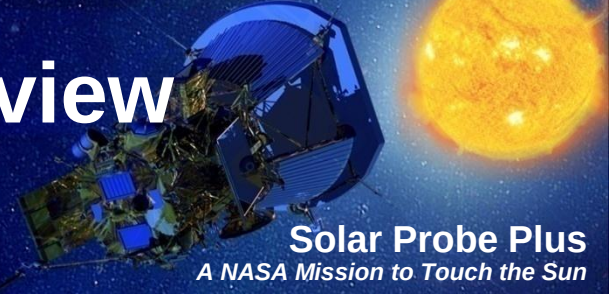
Number	Title	Originator	Assignee	Due Date	Response
6	Determine whether the Fairchild (Commercial) LVDS part is electrically equivalent to the Aeroflex (Flight) part or else use Aeroflex part on Full emulator. (Pg 3: Sec 2.1.1)	T. Green	S. Sawada	Full Emulator Board EDR	Status 9/25/13: Program decision that all GSE interfaces to flight should use the Aeroflex nonflight part. @ $500/per IC. This will cost: 4device/Full EMx12 Full emulators = 48 + 2 Spares = 50x$500 = $25,000 Issue closed.
7	FIELDS 1 and 2 commanding 1 PPS need to be synchronized since the SC will synchronize the interfaces. Make Sure two emulators can be synched to provide a realistic SC interface for FIELDS 1 and 2. (Pg 3: Sec 2.1)	A. Mick	D. Wenstrand H. Eaton S. Sawada	7/31/13	Status 7/18/13: Will test this out on Mini Emulator using CMOS interface. For flight will use RS422 interface, Sync In/Out Signal Direction will be fixed by jumper on the board. For GSEOS, this means capability to run with 1 PC and 3 GSEOS applications running, 1 Master and 2 slaves, Also GSEOS needs to program 2 FPGAs in 2 Emulators.

SC Emulator Requirements Review
Action Item Review



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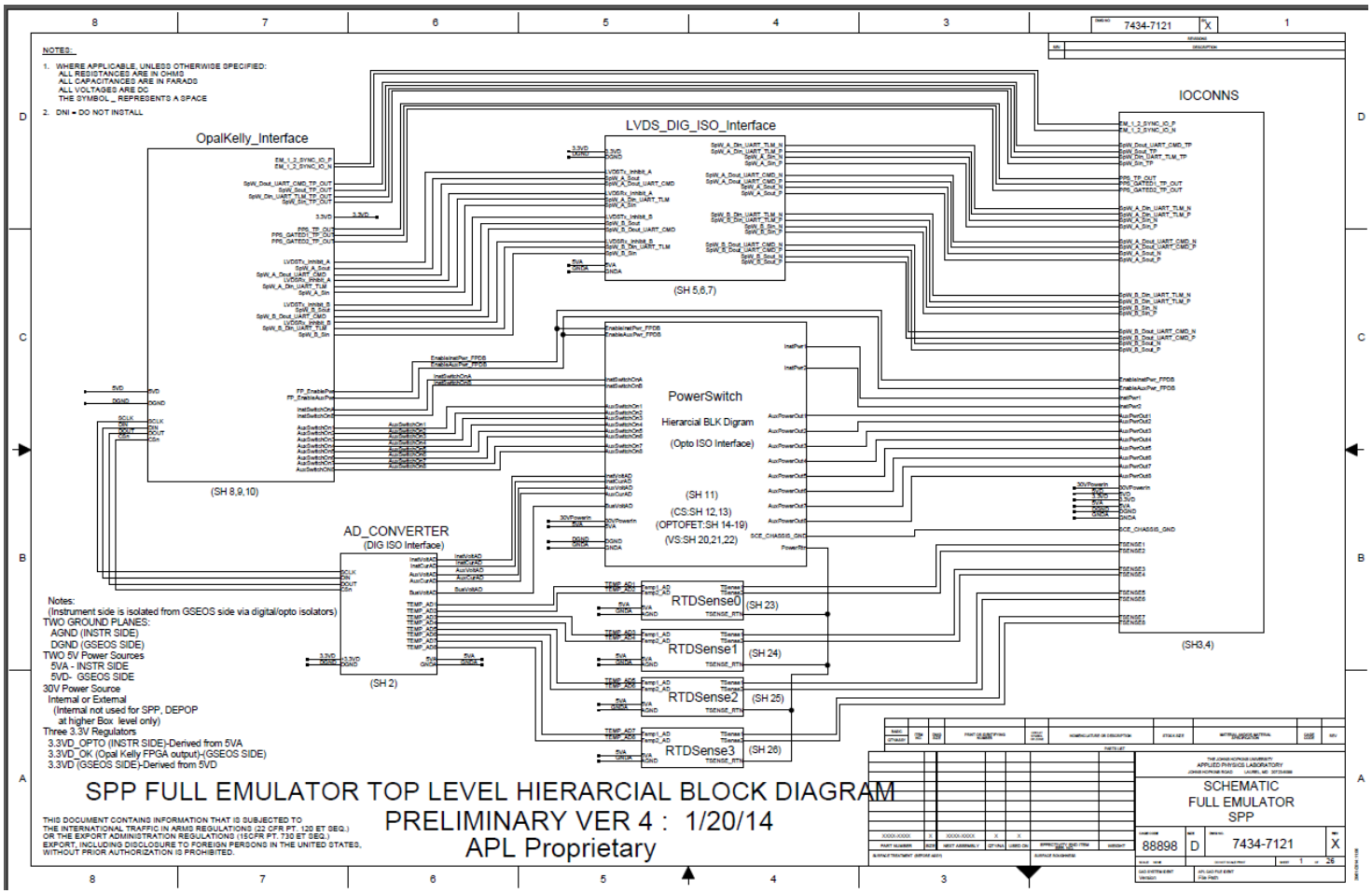
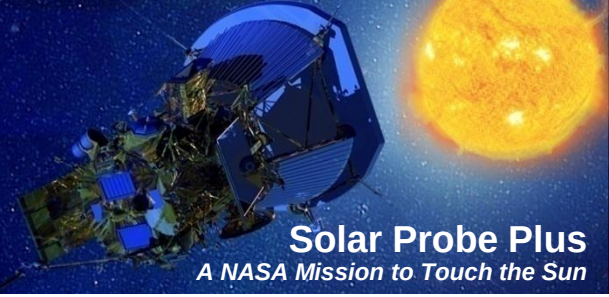
Number	Title	Originator	Assignee	Due Date	Response
8	Consider tying secondary (DGND) or GSEOS side to Chassis for proper grounding. Add single point chassis tie on outside of emulator box. (Pg 18: Figure 13)	T. Green	S. Sawada J. Sheehi	Full Emulator Board EDR	121713: Will add another Banana jack to bring out DGND. See attached diagram. Issue closed.
9	Emulator Command FIFO Size: "shall provide 512 words x 16 FIFO" is too small to guarantee more than 1 second buffering. Change to 2048x16 FIFO. (Pg 13: Sec 2.2.1)	H. Eaton	D. Wenstrand S. Sawada	7/31/13	Status 7/18/13: Per Harry, he Doug will update. Per Thomas OK Bios may help resolve this issue also. Note: This was not included in GSEOS ver12. To be included in next update. 12/5/13: The FPGA bit file has been updated, Thomas to release in next GSEOS version update. Issue closed.

Schematic Review

- **See separate hand out for Full Emulator Schematic/BOM**



RBSP Full Emulator PWA Layout (REF)



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Rear Panel

Instr Data/RTD/PWR Connectors

Test Connector

OK USB CONN

EXT PS SEL SW

RTD1-8

1PPS, CMD,TLM LVDS

3.3VD_ISO/ 3.3VD REGs & BNC TPs

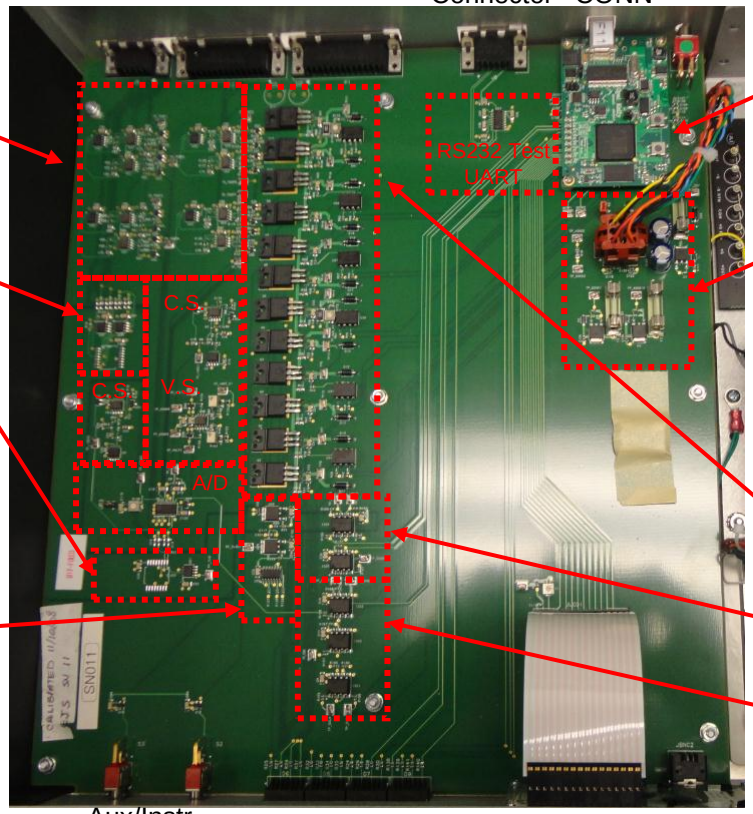
Opal Kelly FPGA Daughter Card

5VD, 5VA, 30V Overvoltage Protection

12 FETs/ OPTO-ISOs

PPS/CMD/TLM OPTO-ISOs

A/D CNTRL OPTO-ISOs



Aux/Instr Switches

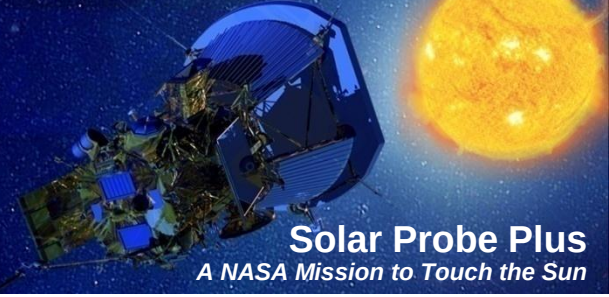
LEDs

LCD Display/BNCTPs(3)

Front Panel

APL

SPP Full Emulator PWA Layout



Solar Probe Plus
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Rear Panel

RTD/PWR Connectors

InstA,InstrB,Test Connector

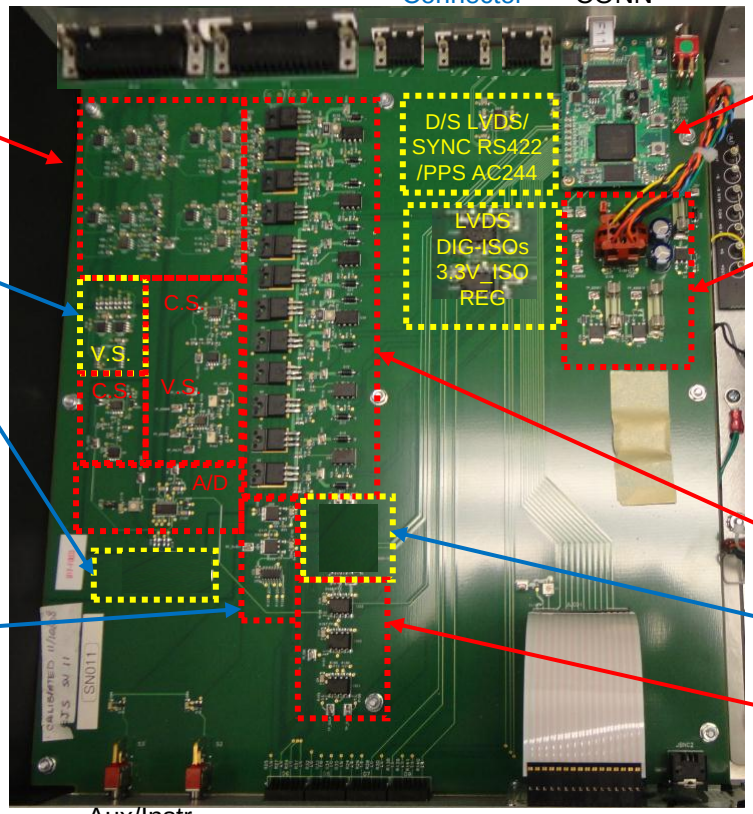
OK USB CONN

EXT PS EN SW

RTD1-8

1PPS, CMD,TLM LVDS (MOVE)

3.3VD_ISO (Move)/ 3.3VD REGs & BNC TPs



Opal Kelly FPGA Daughter Card

5VD, 5VA, 30V Overvoltage Protection

12 FETs/ OPTO-ISOs

PPS/CMD/TLM OPTOs (DEL/Move)

A/D CNTRL DIG_ISOs

Aux/Instr Switches

LEDs

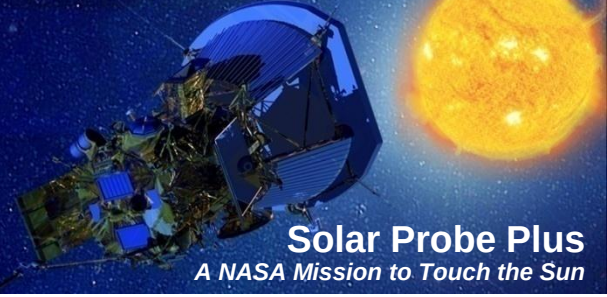
LCD Display/ BNC TPs(4)

Note: SPP Layout Changes shown in Blue Yellow

Front Panel

APL

SPP Full Emulator
5VD Power Supply



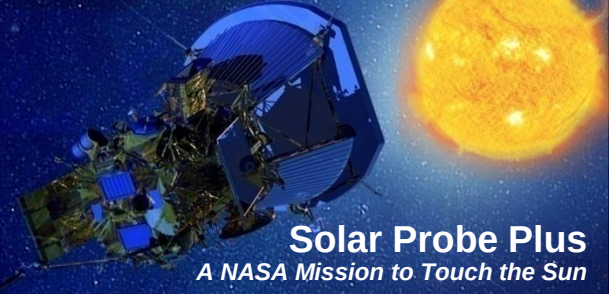
- **5VD requires highest Power, 5VA power is minimal**
- **The Opal Kelly Requires approx 580ma > 500 mamp Max provided by the RBSP Acopican 5EB50 power Supply, Change to 5EB100 (1 Amp supply for SPP). Note: RBSP Used USB 5V power, for SPP the Emulator Power Supply will now power the Opal Kelly.**
- **Below shows Mini Emulator Measured power.**

SPP Mini Emulator 5.1V Power Measurments 080113						
			SN1(ma)	SN1(mW)	SN12(ma)	SN12(mW)
1		At applicaton of 5V power	119	606.9	115	586.5
2		Load HW Test Code	179	912.9	176	897.6
3		SpW at 30 MHz Signal rate- Connected	192	979.2	191	974.1
4		SpW at 30 MHz Signal rate-pass data traffic	193	984.3	191	974.1
5		SpW at 30Mhz(Tx)200 MHz (Rx) Signal rate-pass data traffic	202	1030.2	200	1020
6		Load GSEOS ver 12	490	2499	485	2473.5
7		Load GSEOS ver 12, Side A Internal loopback	492	2509.2	485	2473.5
8		Load GSEOS ver 12, Side B Internal loopback	492	2509.2	485	2473.5

1v to 9v Models

Nominal Output Voltage	Output Current Amps.	Regulation Load +/- %	Regulation Line +/- %	Ripple mV RMS	Model	Order/Quote	Case Size	Price $
1	0.5	0.4	0.05	1	1EB50	Order/Quote	EB-10	99.00
1.5	0.5	0.3	0.05	1	1.5EB50	Order/Quote	EB-10	99.00
1.5	1	0.5	0.05	1	1.5EB100	Order/Quote	EB-13	132.00
1.5	2.5	0.6	0.05	1	1.5EB250	Order/Quote	EB-20	178.00
2	0.4	0.25	0.05	1	2EB40	Order/Quote	EB-10	99.00
3	0.5	0.25	0.05	1	3EB50	Order/Quote	EB-10	99.00
3.3	0.5	0.15	0.05	1	3.3EB50	Order/Quote	EB-10	99.00
3.3	1	0.4	0.05	1	3.3EB100	Order/Quote	EB-13	132.00
3.3	2	0.4	0.05	1	3.3EB200	Order/Quote	EB-20	158.00
4	0.4	0.15	0.05	1	4EB40	Order/Quote	EB-10	99.00
5	0.5	0.15	0.05	1	5EB50	Order/Quote	EB-10	99.00
5	1	0.25	0.05	1	5EB100	Order/Quote	EB-13	120.00
5	1.5	0.25	0.05	1	5EB150	Order/Quote	EB-13	139.00
5	2	0.25	0.05	1	5EB200	Order/Quote	EB-20	158.00
5	2.5	0.25	0.05	1	5EB250	Order/Quote	EB-20	178.00

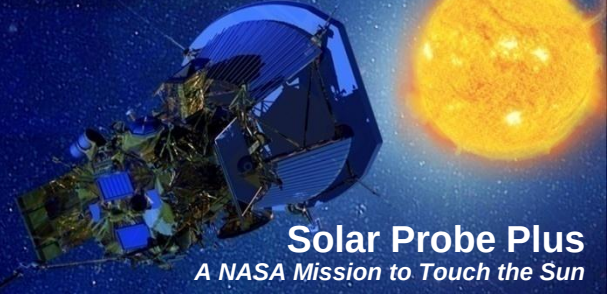
SPP Full Emulator
Parts Change Summary



- **Following List of New parts for SPP Emulator**
  1. **Opal Kelley Daughter Card (later version of OK card)**
     - **Is: XEM6010-LX45 (Was: XEM3010)**
  2. **Digital Isolators (Higher bit rate fro SpW)**
     - **Is: IL711-3E (NVE-2CH) (Was: OPTO ISO HCPL2630-2CH)**
  3. **Opto Isolators-obsolete (2Ch to 4ch)**

     Is: PS2801C (Was: OPTO ISO PS2501-2)
  4. **RS422 Transceiver-LTC1480 (For EM Sync, Not used on RBSP)**
  5. **LVDS –Aeroflex**
     - **Is: UT54LVDS031/32 (was Fairchild FIN1031/32 for Mini Emulator)**
  6. **FETs –**
     - **Is: IXTA52P10P (IXYS) (Was: IRF19540)**
  7. **5V Acopian Power Supply (is 1 A (5EB100): Was .5A(5EB50))**
  8. **Buffer (74VL08-74LVC244)**

Conclusion

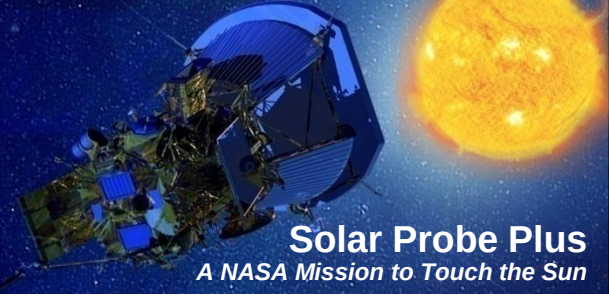


- **Action Items, Comments**
- **Questions**
- **Authorization to Proceed to Fab and Assembly Phase?**

Backup Slides

Backup slides

Schedule



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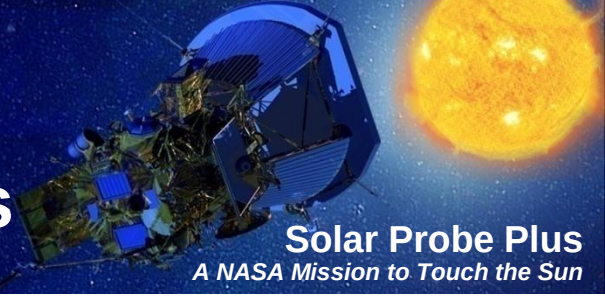
Task Name	% Complete	Physical % Complete	Duration	Start	Finish	Baseline Start	Baseline Finish	Re
Spacecraft Emulator (SCE) Hardware & Firmware	**59%**	**0%**	**515 d**	**Thu 11/29/1**	**Tue 12/23/14**	**Thu 1/17/13**	**Wed 12/21/16**	
SCE: Hire Lead Emulator Engineer/CAM	100%	100%	45 d	Thu 11/29/1	Fri 2/8/13	NA	NA	
SCE: Develop and Review Draft Emulator Requirements Document	100%	100%	91 d	Thu 1/17/13	Thu 5/23/13	Thu 1/17/13	Wed 5/8/13	
SCE: Hold Emulator Requirements Review and Mini-Emulator Schematic Peer Re	100%	100%	35 d	Thu 5/9/13	Thu 6/27/13	Thu 5/9/13	Wed 5/15/13	
SCE: Revise FPGA/SW and Layout Mini-Emulator PWB	91%	75%	130 d	Thu 5/16/13	Mon 11/18/13	Thu 5/16/13	Mon 6/17/13	
SCE: Fab/Assemble/Test Mini-Emulator First Article	100%	100%	11 d	Thu 5/16/13	Fri 5/31/13	Thu 5/16/13	Mon 6/17/13	
SCE: Assemble and Test Mini-Emulators 2-13	100%	100%	46 d	Mon 6/3/13	Tue 8/6/13	Tue 6/18/13	Thu 8/15/13	
Mini-Emulator Deliveries	**100%**	**0%**	**33 d**	**Thu 6/20/13**	**Tue 8/6/13**	**Tue 6/18/13**	**Wed 8/21/13**	
SCE: Support Mini-Emulator Deliveries	95%	80%	98 d	Fri 6/21/13	Thu 11/7/13	Fri 8/16/13	Fri 9/27/13	
SCE: Maintain Mini-Emulators Lifecycle	0%	0%	4 d	Fri 11/8/13	Wed 11/13/13	Mon 9/30/13	Wed 11/27/13	
SCE: Develop and Peer Review Full Emulator Schematic	0%	0%	32 d	Thu 11/14/1	Thu 1/9/14	Mon 12/2/13	Thu 1/9/14	
Procure Materials	42%	7%	125 d	Tue 8/20/13	Mon 2/24/14	NA	NA	
SCE: Layout Full Emulator PWB, Perform Design Analysis	0%	0%	32 d	Fri 1/10/14	Mon 2/24/14	Fri 1/10/14	Mon 2/24/14	
SCE: Prep and Hold Emulator Design Review	0%	0%	9 d	Tue 2/25/14	Fri 3/7/14	Tue 2/25/14	Mon 3/10/14	
Emulators PDR	0%	0%	1 d	Mon 3/10/1	Mon 3/10/14	NA	NA	
SCE: Fab/Assemble/Test Full Emulator First Article	0%	0%	23 d	Tue 3/11/14	Thu 4/10/14	Tue 3/11/14	Thu 4/10/14	
SCE: Assemble and Test Full-Emulators 1-11	0%	0%	25 d	Fri 4/11/14	Thu 5/15/14	Fri 4/11/14	Thu 5/15/14	
Full Emulator Deliveries	**0%**	**0%**	**30 d**	**Fri 4/11/14**	**Thu 5/22/14**	**Fri 4/11/14**	**Thu 5/22/14**	
SCE: Deliver S/C Full Emulator 1 (DPU)	0%	0%	3 d	Fri 4/11/14	Tue 4/15/14	Fri 4/11/14	Tue 4/15/14	
SCE: Deliver S/C Full Emulator 2 (SWEAP)	0%	0%	3 d	Wed 4/16/1	Fri 4/18/14	Wed 4/16/14	Fri 4/18/14	
SCE: Deliver S/C Full Emulator 3 (ISIS)	0%	0%	3 d	Mon 4/21/1	Wed 4/23/14	Mon 4/21/14	Wed 4/23/14	
SCE: Deliver S/C Full Emulator 4 (FIELDS)	0%	0%	3 d	Thu 4/24/14	Mon 4/28/14	Thu 4/24/14	Mon 4/28/14	
SCE: Deliver S/C Full Emulator 5 (DPU)	0%	0%	3 d	Tue 4/29/14	Thu 5/1/14	Tue 4/29/14	Thu 5/1/14	
SCE: Deliver S/C Full Emulator 6 (ISIS)	0%	0%	3 d	Fri 5/2/14	Tue 5/6/14	Fri 5/2/14	Tue 5/6/14	
SCE: Deliver S/C Full Emulator 7 (SWEAP)	0%	0%	3 d	Wed 5/7/14	Fri 5/9/14	Wed 5/7/14	Fri 5/9/14	
SCE: Deliver S/C Full Emulator 8 (ISIS)	0%	0%	3 d	Mon 5/12/1	Wed 5/14/14	Mon 5/12/14	Wed 5/14/14	
SCE: Deliver S/C Full Emulator 9 (SPARE)	0%	0%	3 d	Thu 5/15/14	Mon 5/19/14	Thu 5/15/14	Mon 5/19/14	
SCE: Deliver S/C Full Emulator 10 (SPARE)	0%	0%	3 d	Tue 5/20/14	Thu 5/22/14	Tue 5/20/14	Thu 5/22/14	
SCE: Support Full Emulator Deliveries	0%	0%	154 d	Thu 5/15/14	Tue 12/23/14	Thu 5/15/14	Wed 12/21/16	
SCE: GSEOS Software	**66%**	**0%**	**324 d**	**Thu 1/17/13**	**Thu 5/1/14**	**Thu 1/17/13**	**Mon 12/23/13**	
SCE: Software Development & Test/GSEOS Customization	**66%**	**0%**	**324 d**	**Thu 1/17/13**	**Thu 5/1/14**	**Thu 1/17/13**	**Mon 12/23/13**	
SCE: Interface Software Development/GSEOS Customization (Build 0): Min	94%	90%	215 d	Thu 1/17/13	Mon 11/18/13	Thu 1/17/13	Thu 6/13/13	
SCE: Interface Software Development/GSEOS Customization (Build 1): Full	0%	0%	75 d	Tue 11/19/1	Fri 3/14/14	Fri 6/14/13	Mon 9/30/13	
SCE: GSEOS Emulator Support	0%	0%	16 d	Thu 4/10/14	Thu 5/1/14	Mon 12/2/13	Mon 12/23/13	

Differences: Full vs. Mini Emulators



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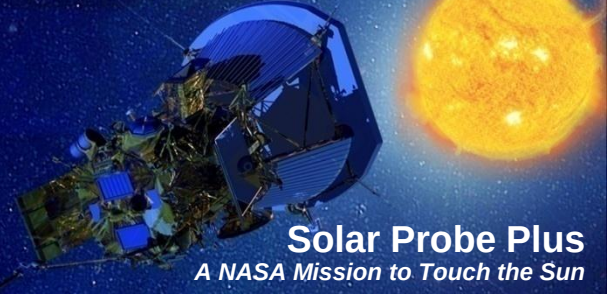
Capability	Full Emulator		Mini-Emulator
Instrument CMD/TLM (UART/SpW) (A/B) Interface	YES		YES
1PPS/PPS_Gated Interface (Instr EGSE IF)	YES		YES
USB Interface to PC (Opal-Kelly) (Note: USB Power not used)	YES		YES
External 5V Input for Internal Emulator Logic	NO		YES
External AC Input for Internal Emulator Logic (AC/DC converters)	YES		NO
Optical/Digital Isolation	YES		NO
30V Power OUTPUTS (10)	YES		NO
Temperatures (8)/Voltage/Current Sensors	YES		NO
EXT 30V SC BUS Power Supply Input Only/ (No Internal 30V SC BUS Power Supply)	YES		NO
Emulator 1 to 2 Sync Capability (FIELDS only)	YES		NO
Rack Mount	YES (5”H x 19”W x 14”D		NO (1”H x 5”W x 7”D)

Power Services List by Instrument



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Subsystem	Power Service	Service Type	used to show compliance with 7434-9040, section 4.10; N/A for pulsed services	Maximum Pulse Current; N/A for switched and unswitched services
EPI-Hi	EPI-Hi Main Power (LVPS)	Switched	0.5 AN	N/A
	EPI-Hi Operational Heater	Switched	0.25 AN	N/A
	EPI-Hi Survival and Warm-up Heater	Switched	0.5 AN	N/A
EPI-LO	EPI-Lo Operational Power	Switched	0.5 AN	N/A
	EPI-Lo Survival, Warm-up and LP Op Heater	Switched	0.5 AN	N/A
FIELDS1	FIELDS1 Operational Power	Switched	1.0 AN	N/A
	FIELDS1 Operationaland Survival Heater	Switched	0.5 AN	N/A
	FIELDS-1 Mech Pre-deployment Warm-up Heaters	Switched	0.25 AN	N/A
FIELDS2	FIELDS2 Operational Power	Switched	1.0 AN	N/A
	FIELDS2 Operationaland Survival Heater	Switched	0.5 AN	N/A
	WISPR & FIELDS-2 Mech Pre-deployment Warm-up Heaters	Switched	0.25 AN	N/A
FIELDS	FIELDS Antenna Deploy Whip Cage 1-2A	Pulsed	N/A	3.0 A
	FIELDS Antenna Deploy Whip Cage 3-4A	Pulsed	N/A	3.0 A
	FIELDS Antenna Deploy Whip Cage 1-2B	Pulsed	N/A	3.0 A
	FIELDS Antenna Deploy Whip Cage 3-4B	Pulsed	N/A	3.0 A
	FIELDS Antenna Deploy Hinge 1A	Pulsed	N/A	2.0 A
	FIELDS Antenna Deploy Hinge 2A	Pulsed	N/A	2.0 A
	FIELDS Antenna Deploy Hinge 3&4A	Pulsed	N/A	3.0 A
	FIELDS Antenna Deploy Hinge 1B	Pulsed	N/A	2.0 A
	FIELDS Antenna Deploy Hinge 2B	Pulsed	N/A	2.0 A
	FIELDS Antenna Deploy Hinge 3&4B	Pulsed	N/A	3.0 A
SWEAP	SWEAP Operational Power	Switched	1.0 AN	N/A
	SPAN A&B Survival Survival Heater	Switched	1.0 AN	N/A
	SPC & WISPR Survival Heater	Switched	1.0 AN	N/A
WISPR	WISPR Main Power	Switched	1.0 AN	N/A
	WISPR Door Deploy Power A	Pulsed	N/A	4.0 A
	WISPR Door Deploy Power B	Pulsed	N/A	4.0 A
	WISPR Operational Heaters	Switched	0.25 AN	N/A

1. **Summary**
2. **Instrument**

Instrument	INSTR QTY	AUX QTY
EPI HI	1	2
EPI LO	1	1
FIELDS1	NA	NA
FIELDS2	NA	NA
SWEAP	1	2
WISPR	1	3

- **FIELDS/WISPR Door Deploy will not use Power Switching functions in Emulator**

RTD Temp Sensor List by Instrument

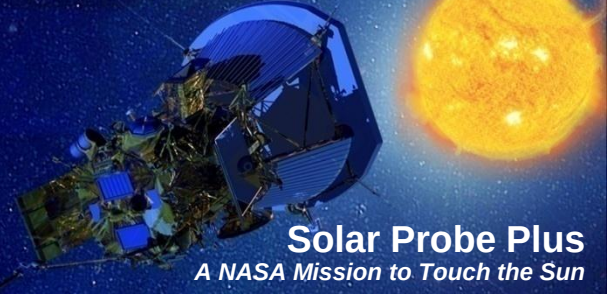


Table 12. Temperature Sensors (1 of 3)

RIU String	Subsystem	Location	Temp Range	
A	Inst	FIELDS MEP (on box)	-100	100
A	Inst	FIELDS/Magnetometer/Flux Gate 1	-175	200
B	Inst	FIELDS/Magnetometer/Flux Gate 2	-175	200
A	Inst	FIELDS/Magnetometer/Search Coil	-175	200
A	Inst	FIELDS/Plasma Wave Pre-amp 1	-175	200
B	Inst	FIELDS/Plasma Wave Pre-amp 2	-175	200
A	Inst	FIELDS/Plasma Wave Pre-amp 3	-175	200
B	Inst	FIELDS/Plasma Wave Pre-amp 4	-175	200
A	Inst	ISIS EPI-Hi 1	-100	100
B	Inst	ISIS EPI-Hi 2	-100	100
A	Inst	ISIS EPI-Hi 3	-100	100
B	Inst	ISIS EPI-Hi 4	-100	100
B	Inst	ISIS EPI-Hi 5	-100	100
A	Inst	ISIS EPI-Lo 1	-100	100
B	Inst	ISIS EPI-Lo 2	-100	100
B	Inst	ISIS EPI-Lo 3	-100	100
A	Inst	SWEAP/SPAN-A+ 1	-100	100
B	Inst	SWEAP/SPAN-A+ 2	-100	100
B	Inst	SWEAP/SPAN-A+ 3	-100	100
A	Inst	SWEAP/SPAN-B 1	-100	100
B	Inst	SWEAP/SPAN-B 2	-100	100
A	Inst	SWEAP/SPAN-B 3	-100	100
A	Inst	SWEAP/SPC Pre-amp	-175	200
B	Inst	SWEAP/SWEM	-100	100
A	Inst	WISPR DPU	-100	100
A	Inst	WISPR/Hemispheric Imager 1	-100	100
B	Inst	WISPR/Hemispheric Imager 2	-100	100
A	Inst	WISPR/Hemispheric Imager 3	-100	100
B	Inst	WISPR/Hemispheric Imager 4	-100	100

1. **Summary (From SC EICD)**
2.

Instrument	Type 1 100C	Type2 200C
▪ FIELDS	1	7
▪ EPI HI	5	
▪ EPI LO	3	
▪ SWEAP	7	1
▪ WISPR	5	

1. **Below Items Not Included, since only needed at system level not subsystem level**

A	Inst Accm	Mag boom deployment mechanism #1	-100	100
B	Inst Accm	Mag boom deployment mechanism #2	-100	100
A	Inst Accm	PWI whip mechanism 1	-100	100
B	Inst Accm	PWI whip mechanism 2	-100	100
A	Inst Accm	PWI whip mechanism 3	-100	100
B	Inst Accm	PWI whip mechanism 4	-100	100
A	Inst Accm	PWI whip mechanism 5	-100	100
B	Inst Accm	PWI whip mechanism 6	-100	100
A	Inst Accm	PWI whip mechanism 7	-100	100
B	Inst Accm	PWI whip mechanism 8	-100	100
A	Inst Accm	WISPR door mechanism 1	-100	100
B	Inst Accm	WISPR door mechanism 2	-100	100

SPP SC Emulator Updates

- **1PPS & GATED PPS Timing (To Instrument EGSE)**

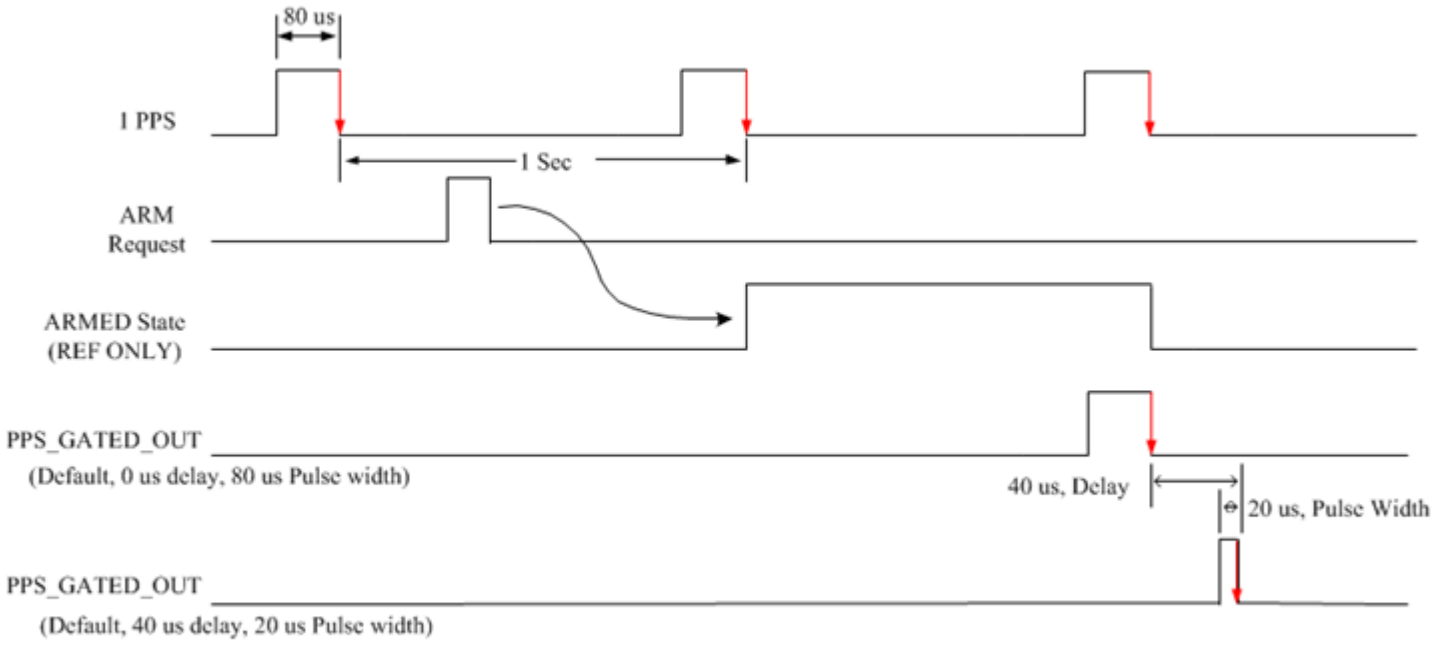
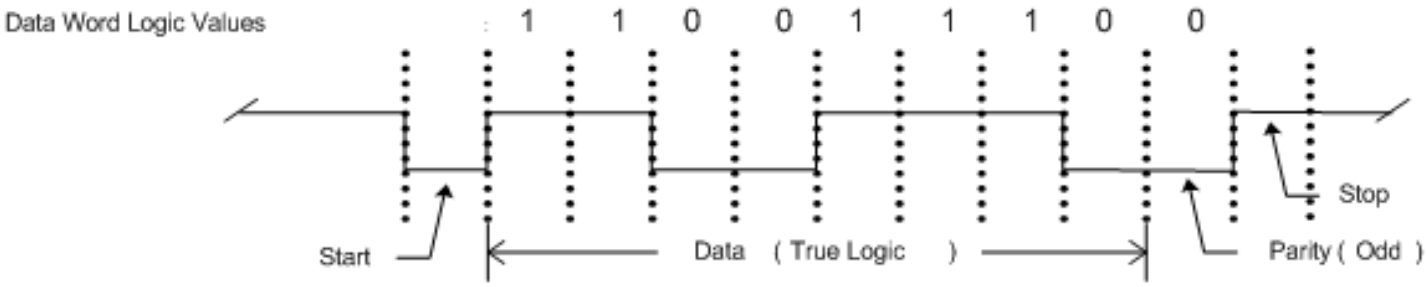


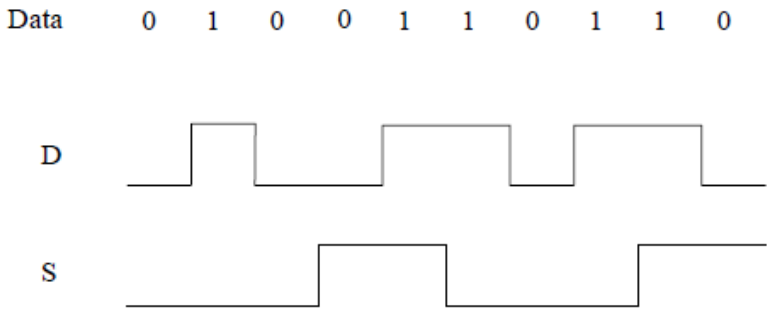
Figure 9. PPS_Gated1 (2) Timing

SPP SC Emulator Updates

- **UART Timing**

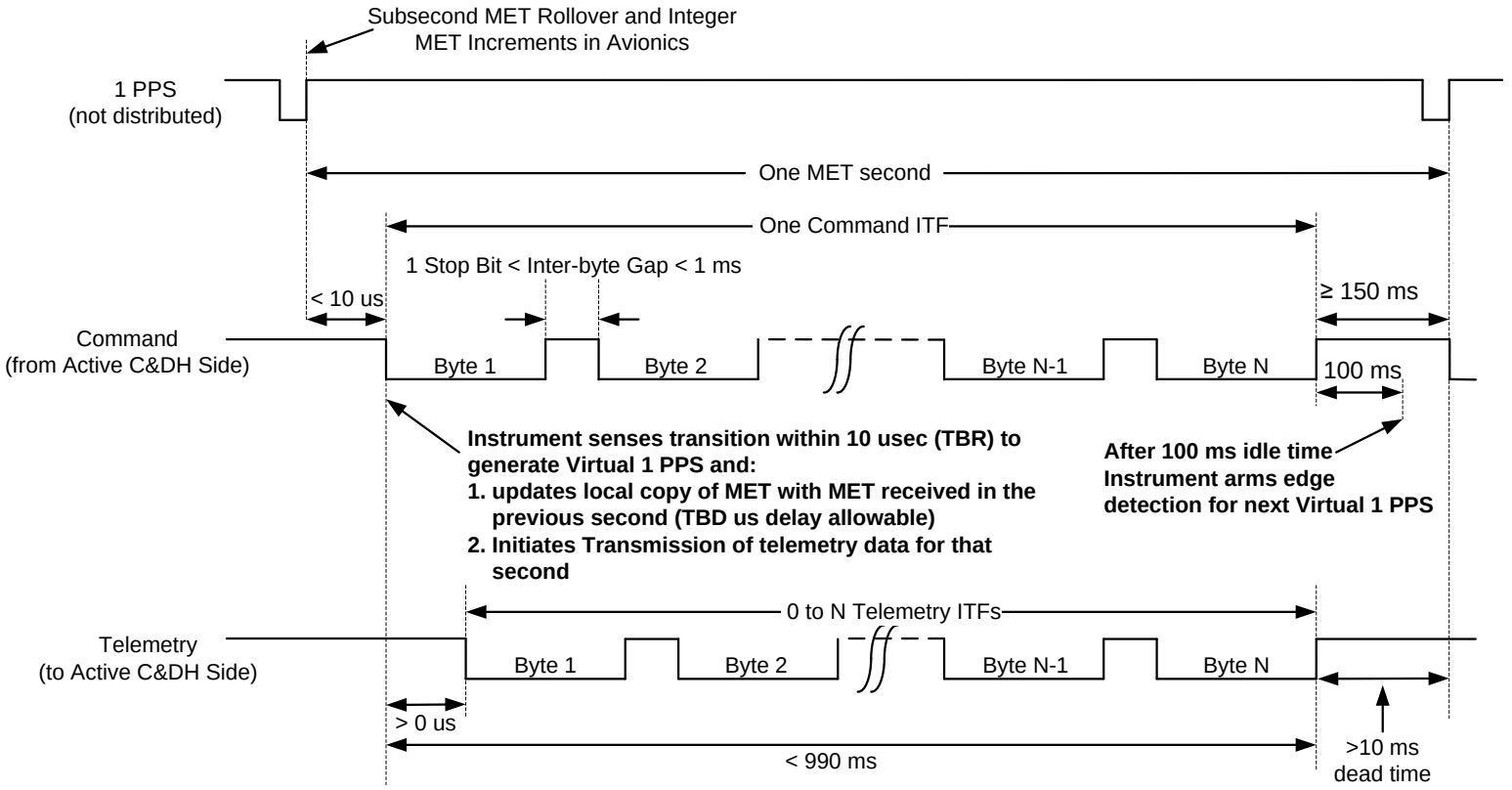


- **SpaceWire Data/Strobe Timing**

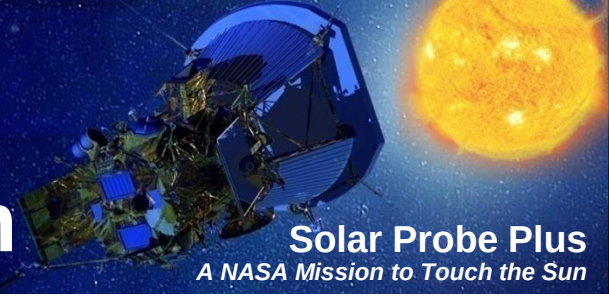


SPP SC Emulator Updates

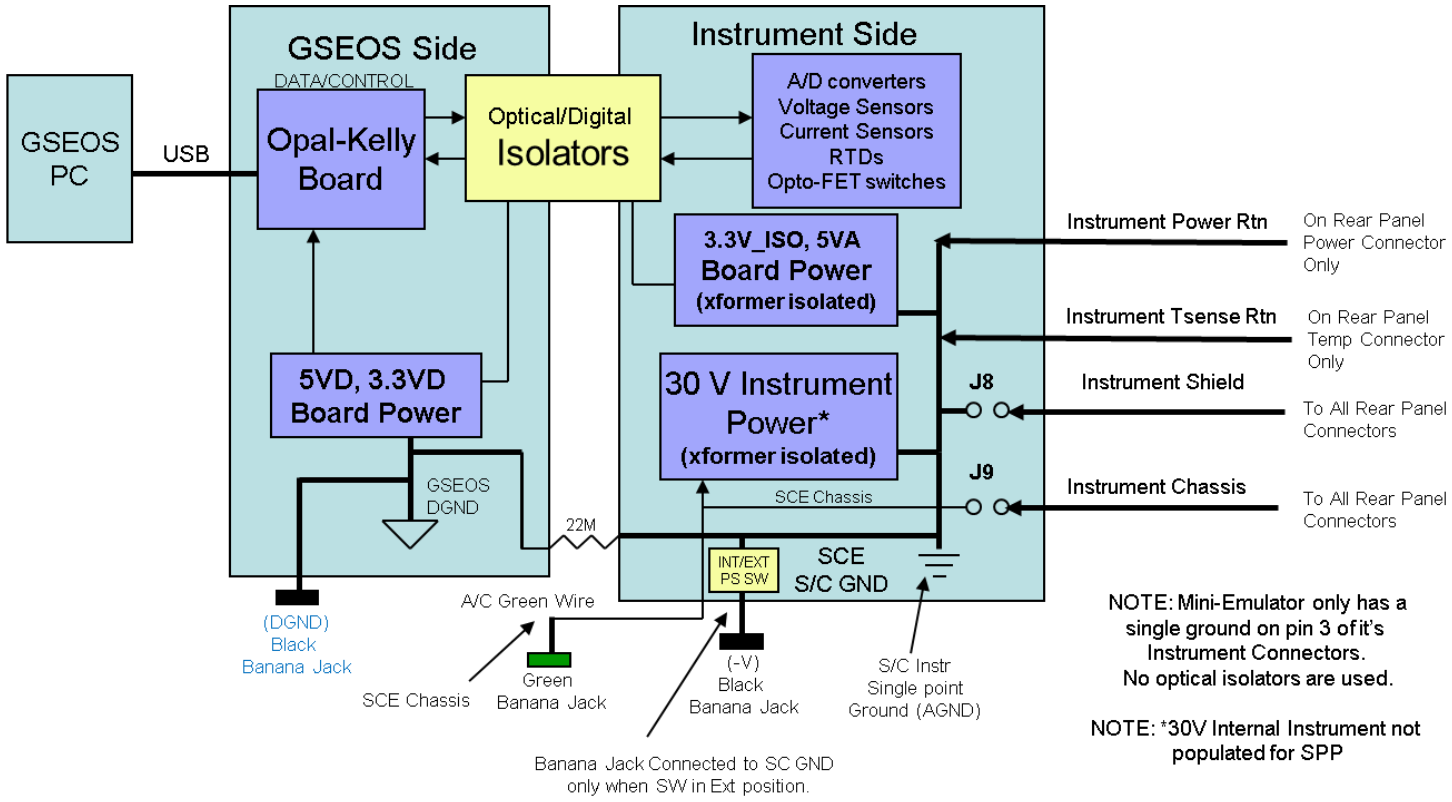
- **Command/Telemetry Timing (UART)**



SPP Full Emulator Grounding Diagram



Solar Probe Plus
A NASA Mission to Touch the Sun



NOTE: Mini-Emulator only has a single ground on pin 3 of it's Instrument Connectors.
No optical isolators are used.

NOTE: *30V Internal Instrument not populated for SPP

SPP Full Emulator Box Wiring Diagram

Solar Probe Plus
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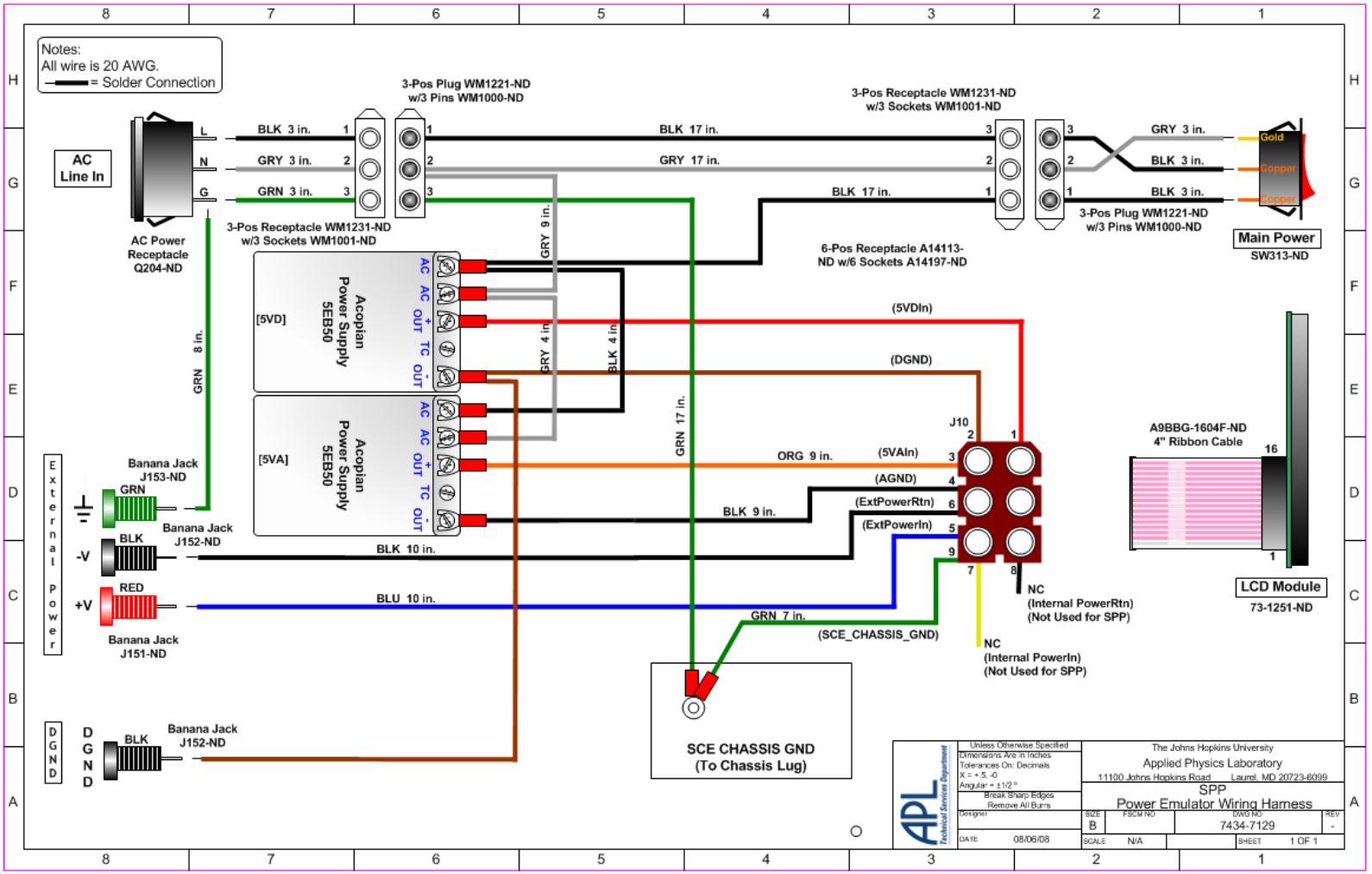
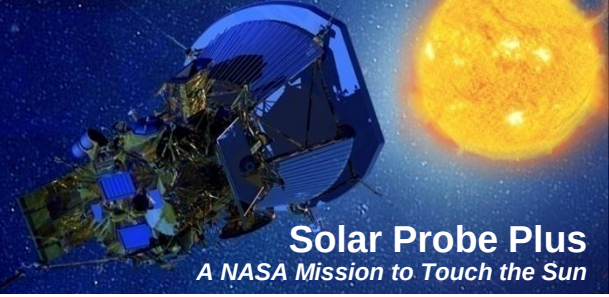


SCE Staffing



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- **Harry Eaton, Embedded SW**
- **Doug Wenstrand, FPGA Design**
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    - **Alan Mick (SPP Data Systems Engineering)**
    - **John Hayes (SPP WISPR DPU/ISIS-EPI-Lo)**
- **CAD/Manufacturing**
    - **Darryl Zawada, Katrina Roarty, Chris Britt, Karen Moore**