SPP SPACECRAFT EMULATOR REQUIREMENTS

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VERSION 2.2-DRAFT

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JHU/APL PROJECT APPROVALS

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REVISION HISTORY

Version	Date	Comments
1.0	April 26, 2013	Initial Revision
2.0	May 31, 2013	Update per 052313 Emulator Team Review Meeting Comments
2.1	June 5, 2013	Update clarification to 2.0, fix typos found
2.2	June 11, 2013	Added section 1 2: Drawing Numbers; Updated sections: 2.1.1.2-updated; Figure 9, 22.6.1, 2.2.7.1, (remove arm status); 2.5 SpW Error Detection –updated; Appendix A/B: fix typos in part numbers; Appendix C-updated.

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1. OVERVIEW

The SPP Spacecraft Emulator shall provide a “spacecraft like” interface between the instrument and a personal computer (PC) running GSEOS. There are two versions of the SPP Emulator, the full function Emulator (referred to as the *Emulator*) and the *Mini-Emulator*. Block diagrams for both versions are shown in Figures 1 and 2.

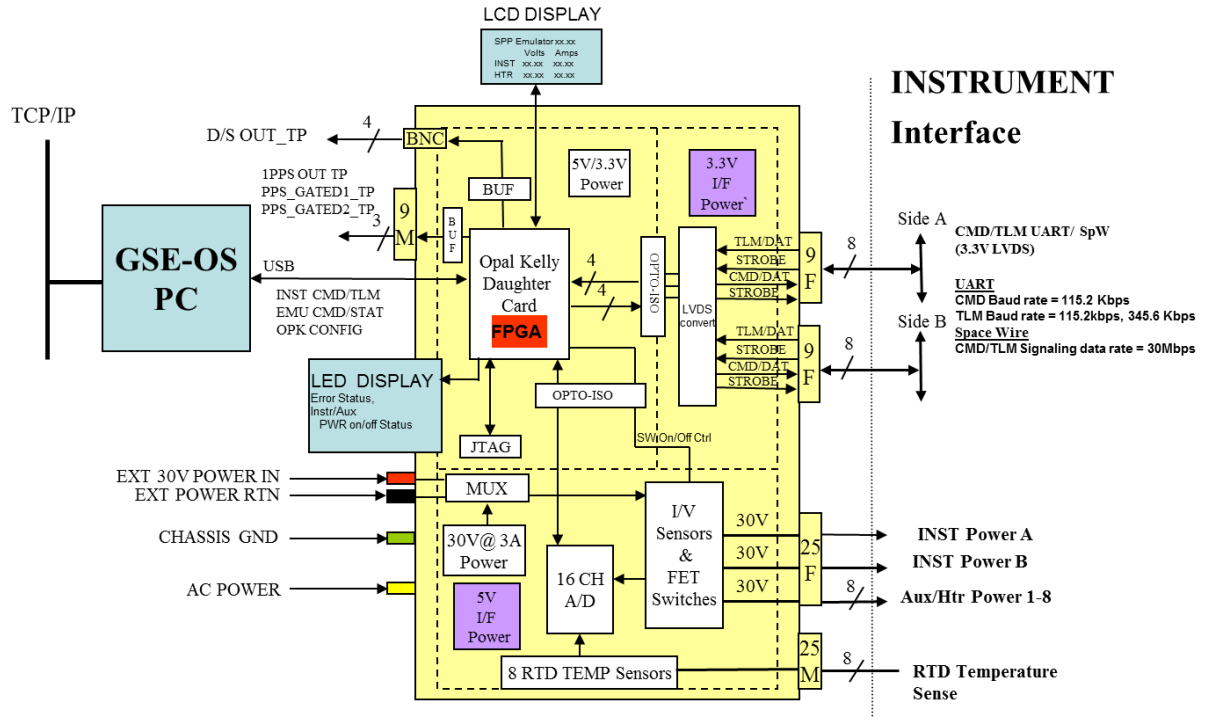


Figure 1 SPP Emulator

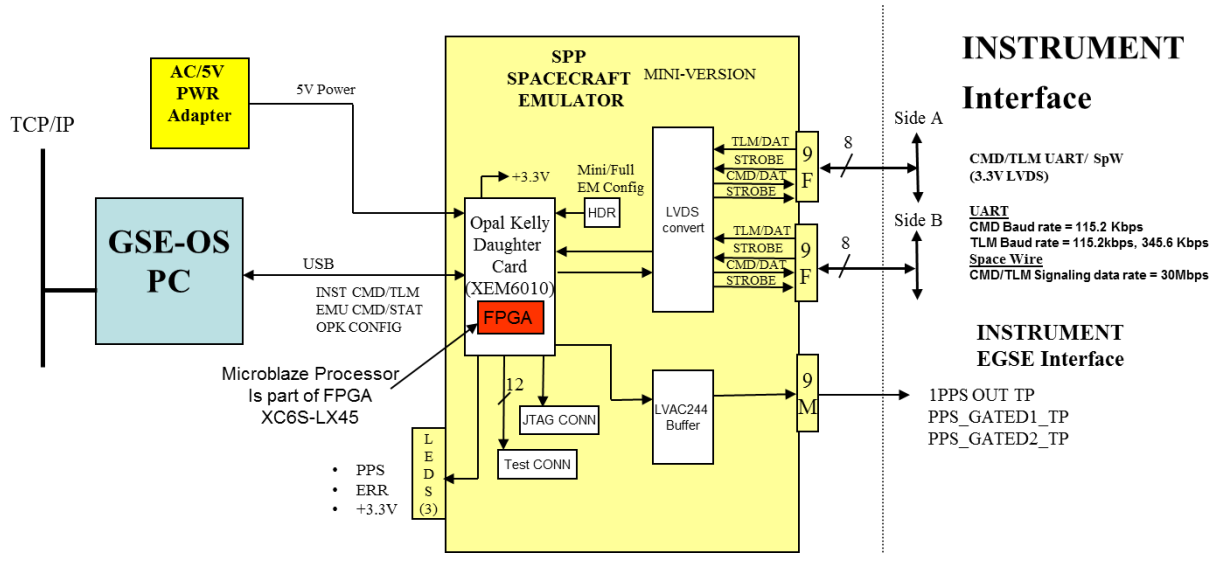


Figure 2 SPP Mini-Emulator

1.1 Reference Documents

1. TBD, General Instrument ICD (GII)
    1 File: GIS_Electrical_Sections,_Draft_SPP_01.18.13.doc), (V. Bailey, APL)
    2 File: SPP GIS Instrument ICD CDH Revision V10 2013-06-03.docx (packet info)
2. 7434-9075, SPP SpaceWire ICD V16 2013-03-25

3. SPP Emulator ICD (SPP BIOS); GSE Software Inc.

4. ECSS-E-ST-50-12C, Space engineering – SpaceWire – SpaceWire links, nodes, routers and networks. 31 July 2008.
5. ECSS-E-ST-50-52C, Space engineering – SpaceWire – Remote memory access protocol http://www.ecss.nl/forums/ecss/dispatch.cgi/standards/showFile/100770/d20100209121656/No/ECSS-E-ST-50-52C(5February2010).pdf
6. ECSS-E-ST-50-11, Space engineering – SpaceWire – Remote memory access protocol Draft F, 12/4/2005

7. 561-SPEC-001, Rev 2.2f, SpaceWire RAMP Target Core Specification (Goddard, 11/23/11)
8. 561-SPEC-002, Rev D, SpaceWire RAMP Core Specification (Goddard, 11/29/11)
9. 561-SPEC-003, Rev Draft 2, SpaceWire Router Specification (Goddard, 11/29/10)

1.2 Reference Drawing Numbers

1. 7434-7110 Mini Emulator Top Level
2. 7434-7100 Mini Emulator PWA
3. 7434-7101 Mini Emulator Schematic
4. 7434-7102 Mini Emulator EPL

5. 7434-7xxx Full Emulator Top Level
6. 7434-7xxx Full Emulator PWA
7. 7434-7xxx Full Emulator Schematic
8. 7434-7xxx Full Emulator EPL

2. SYSTEM DESCRIPTION

The Emulator interfaces can be divided into the following categories:

a) Instrument Data and Timing Interfaces (between Emulator and Instrument)
b) PPS Test Point (TP) Interface (between Emulator and Instrument EGSE)
c) USB Interface (between Emulator and PC)
d) Instrument Power Interfaces (between Emulator and Instrument)
e) Temperature Sensors (between Emulator and Instrument)
f) Miscellaneous Interfaces

The Mini-Emulator only provides interfaces for **a)**, **b) and c)** above and does not have optical isolation. The Mini-Emulator **SHOULD NOT BE CONNECTED TO FLIGHT HARDWARE**.

2.1 Instrument Data and Timing Interfaces

Note: The Emulator will be configurable using GSEOS to provide either UART data interfaces or SpaceWire data interfaces at any one time. (ie., not both simultaneously) The UART and SpaceWire functions shares common LVDS Driver and Receiver interfaces.

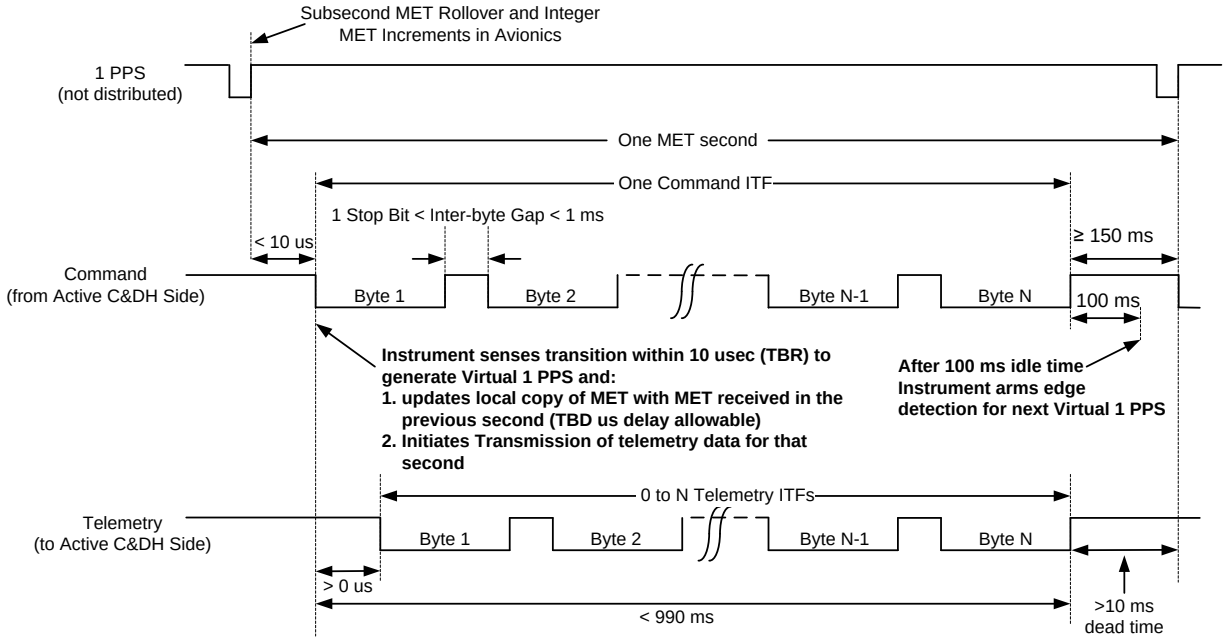
For SPP, the Emulator shall be configured either for UART or SpaceWire data interfaces for the following SPP instruments:

- FIELDS, SWEAP, ISIS (EPI-HI, EPI-LO) : UART
- WISPR: SpaceWire

2.1.1 UART Commands to Instrument

The Emulator shall send commands to the instrument using two serial UART like data streams (Side A, Side B), at any point in time only one of the two Command UARTS will be active. In each interval between Virtual 1 PPS pulses, the active Command UART will send *INSTRUMENT* data as defined in the Instrument Transfer Frame (ITF) protocol described in the GII (General Instrument ICD). The command interface window for transmission of complete data words is from the Virtual 1PPS up to 150 msecs prior to the next Virtual 1 PPS as shown in Figure 3. The Inter-byte Gap time shall be configurable with a resolution of 1 us.

The data rate shall be configurable from GSEOS. The nominal/default command data rate is 115.2 Kbps. A capability shall also exist to inject errors into the command UART data stream (see section 2.3). The command signals shall be at 3.3V LVDS levels. The electrical interface is shown in Figure 4. The optical isolators are only present in the full Emulator. The LVDS driver shall be electrically equivalent to the flight part.



Note: Active C&DH Side =Active Emulator Side

Figure 3. UART Command & Telemetry Frame Timing

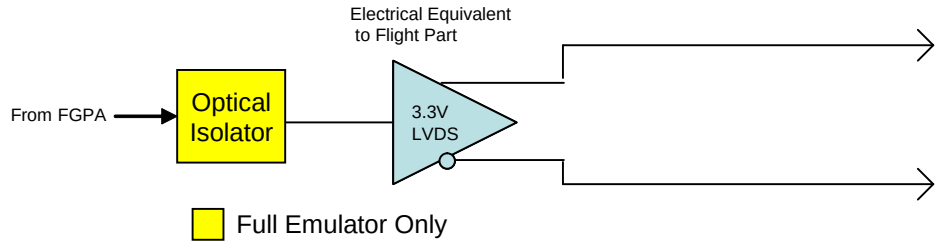


Figure 4. Command UART/SpaceWire(D/S) Output Electrical Interface

2.1.1.1 Command UART Interface and Virtual 1 PPS Timing

The Emulator Command protocol timing is shown in Figure 3. The Virtual 1 PPS is aligned with the leading edge of the first command byte.

Note: The *Instrument* **will** detect the leading edge of the first command byte within 10 microseconds TBR by implementing an Idle Timer on the link. When the link is inactive for 100 milliseconds it shall enable detection of the next falling edge on the interface. This detected edge is defined as the Virtual 1 PPS. The Virtual 1 PPS will be used for instrument timekeeping.

2.1.1.2 Instrument use of Active Command UART Interface

The Emulator shall only put one of the two Command UART interfaces in the active state at a time. Active means that Command messages are sent per the time in Figure 3. The other Command UART shall be inactive, with inactive defined as powered on and output disabled (ie., Tri-stated) for Full Emulators and powered on and driven high (ie., to simulate Tri-stated condition) for Mini Emulators (which is the link idle state).

Note: The *Instrument* **will** be capable of using the active Command UART at any time, with no advanced warning of a switchover. (The Emulator is not required to switch A/B sides in the middle of a command.)

2.1.1.3 Transfer Layer

The Emulator shall transmit one Instrument Transfer Frames (ITF) between Virtual 1PPS pulses as documented in the GII (General Instrument ICD).

2.1.2 UART Telemetry from Instrument

The Emulator receives two UART like telemetry data streams from the instrument (Side A, Side B). The Instrument will transmit data on the same interface as it received the Virtual 1 PPS. The Instrument will disable the LVDS transmitter on the inactive telemetry interface. The Emulator shall provide capability to monitor/detect erroneous traffic on the inactive side. (See section 2.4)

Note: The telemetry interface window for transmission of complete data words is from the Virtual 1PPS up to 10 msec prior to the next Virtual 1PPS as shown in the Figure 3.

Note: When the *Instrument* detects the Virtual 1 PPS on the Command UART interface, it can immediately begin transmission of telemetry data per Figure 3. The *Instrument* will cease transmission of telemetry data 990 milliseconds after detection of the Virtual 1 PPS or sooner.

Note: The *Instrument* may transmit one or multiple Instrument Transfer Frames (ITF) between Virtual 1 PPS pulses.

The data rate shall be configurable to 115.2 Kbps and to 345.6 Kbps using GSEOS. The nominal Telemetry UART data rate shall be 115.2 Kbps. The data rates for Command and Telemetry UART shall be selected independently. The telemetry signals shall be at 3.3V LVDS electrical levels. Figure 5 shows the first circuit interface for the telemetry data stream. Optical isolators shall only be used in the full Emulator. The LVDS receiver shall be electrically equivalent to the flight part.

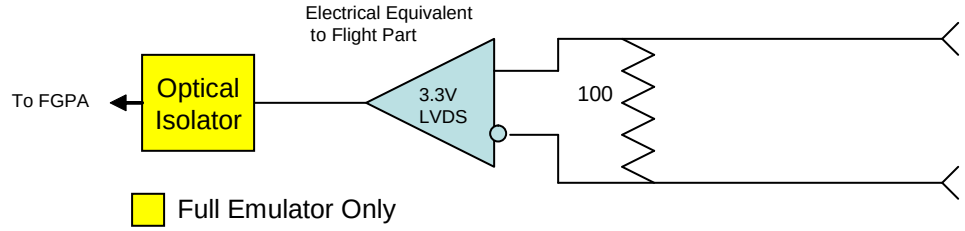


Figure 5.Telemetry UART/SpaceWire(D/S) Input Electrical Interface

2.1.3 UART Parameters and Polarity

The command and telemetry words consist of 1 start bit, 8 data bits, odd parity and 1 stop bit. Within the data byte, the least significant bit is transmitted first. For multi-byte values, “big endian” format shall be used where the most significant byte is sent first.

As stated above, the command UART data rate is nominally[1] 115.2 Kbps with an accuracy of +/- 1.5%. The Telemetry UART data rate is nominally 115.2 Kbps with an accuracy of +/- 1.5

[1] Although the nominal rate is 115.2 Kbps, CMD and TLM rates from 19.2 Kbps to 345.6 Kbps are programmable via GSEOS. The rates can also be different for CMD and TLM but by default the rates will be set to 115.2Kbps and only changeable by editing a GSEOS configuration file.

%. Data bit values are true logic (not inverted) at the input to the driver, the "+" output of the driver, and the output to the receiver. At the output of the driver, a logic one means the "+" output is high and the "-"output is low. For a logic zero, the "+" output is low and the "-"output is high. The idle condition for the line is a high input to the driver. This polarity is shown in Figure 6.

Note 1: The Command Baud rate (clock period) can be set to within 10ns.

Note 2: The Telemetry Baud rate is determined by the following equation: Telemetry Baud Rate = (100Mhz/16)/(N) where N is an integer. Therefore, for a desired Baud Rate, calculate the value of N using the equation. Round N to the nearest integer, then recalculate the actual configurable Baud rate using N in the equation. The accuracy is determined by difference between the desired and actual configurable baud rates. (Example, for a desired 345.6 KHz Baud rate, N=18.08. The configurable baud rate, using N = 18, is 347.222 KHz. The resultant accuracy is +0.47%.)

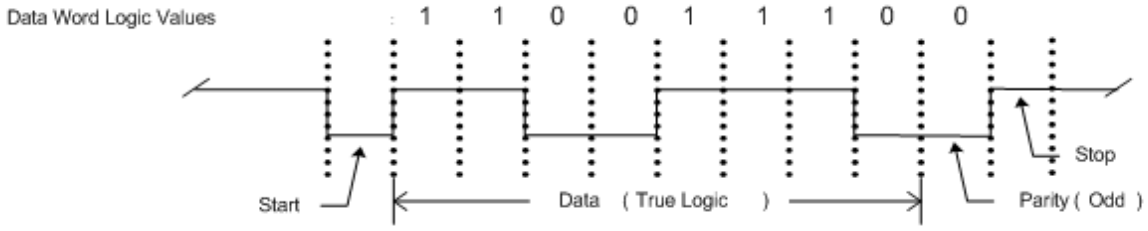


Figure 6. UART Polarity

2.1.4 1PPS Signal to Instrument EGSE

The Emulator shall send a 1PPS pulse to the instrument EGSE. The electrical level for this 1PPS pulse shall be 3.3V LVCMOS. The electrical interface is shown in Figure 7. The Emulators shall not have optical isolators for this interface, since it interfaces to Instrument EGSE equipment. The 1PPS timing shall have an accuracy of 100 ppm and the 1PPS pulse width shall be 80 u-seconds as shown in Figure 8.

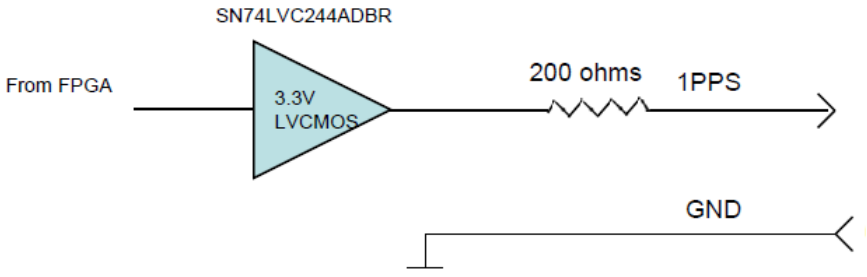


Figure 7. 1 PPS/PPS_Gated1/ PPS_Gated2 Electrical Interface

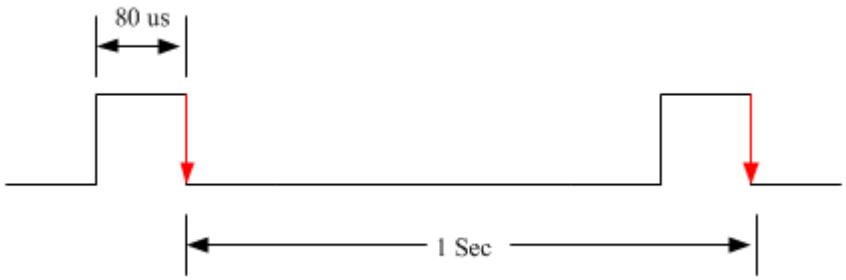


Figure 8. 1 PPS Timing

2.1.5 PPS_GATED1 and PPS_GATED2 Signals to Instrument EGSE

The Emulator shall send two PPS GATED pulse signals (PPS GATED1, PPS GATED2) to the instrument EGSE. The electrical level for these signals shall be 3.3V LVCMOS. The electrical interface is shown in Figure 7. The Emulators shall not have optical isolators for this interface, since it interfaces to Instrument EGSE equipment. The PPS_Gated timing shall have an accuracy of 100 ppm as shown in Figure 9. The pulse width (default: 80 u-seconds) and positioning of the gated pulse (delay (default: 0 u-seconds)) with respect to the 1PPS pulse shall be controlled by GSEOS (see SPP BIOS ICD).

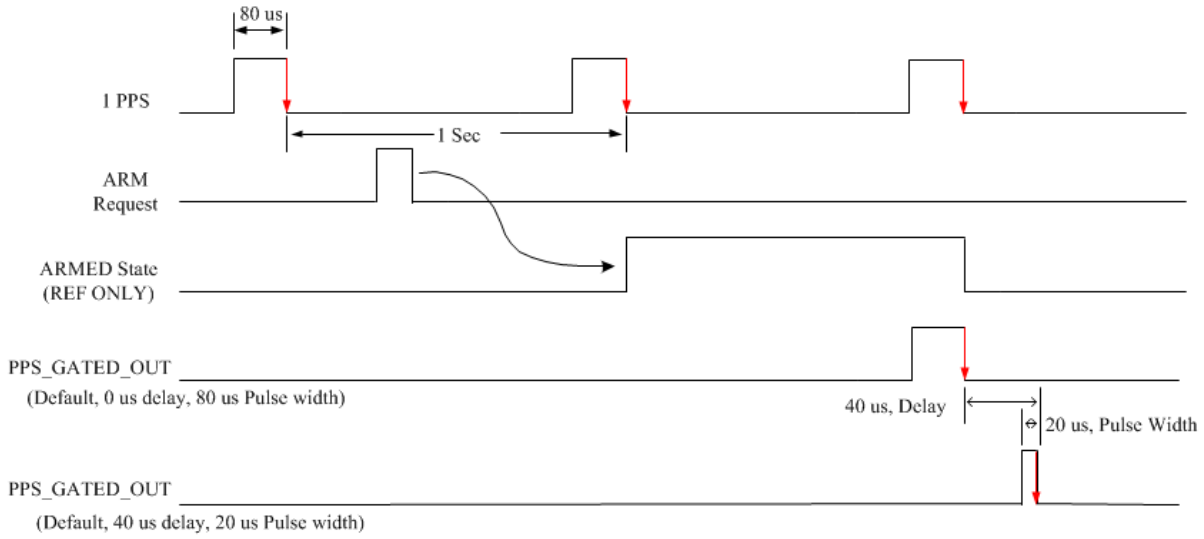


Figure 9. PPS_Gated1 (2) Timing

2.1.6 SpaceWire Commands to Instrument

The Emulator shall send commands to the instrument using two serial SpaceWire data streams (Side A, Side B), at any point in time only one of the two Command SpaceWire interfaces will be active. In a minor frame interval, the active Command SpaceWire interface will send

INSTRUMENT data as defined in the Instrument Transfer Frame (ITF) protocol described in the GII (General Instrument ICD). The command interface window for transmission of complete data words is within the same minor frame.

The Command SpaceWire signaling data rate (ie., raw bit rate) shall be 30 Mbps. A capability shall also exist to inject errors into the command SpaceWire data stream (see section 2.5). The command signals shall be at 3.3V LVDS levels. The electrical interface is shown in Figure 4. The optical isolators are only present in the full Emulator. The LVDS driver shall be electrically equivalent to the flight part.

*2.1.6.1 **Instrument use of Active Command SpaceWire Interface***

The Emulator shall only put one of the two Command SpaceWire interfaces in the active state at a time. The other Command SpaceWire shall be inactive, with inactive defined as powered on and output disabled (ie., Tri-stated) for Full Emulators and powered on and driven high (ie., to simulate Tri-stated condition) for Mini Emulators.

PR Mode for primary and redundant SpW links should use “00” Always primary port or “01” Always redundant port, per GSFC SpW Node Spec, 561-SPEC-002, Rev D, Section 4.2
(Note: The emulator will not provide automatic switchover capability for failed SpaceWire A/B links.)

*2.1.6.2 **Transfer Layer***

The Emulator shall be able to transmit one Command Instrument Transfer Frames (ITF) per major frame per the desired bus schedule as defined by the GII. (Note: Typically the instrument command ITF shall be sent during MNF49.)

*2.1.6.3 **Spacecraft Time Synchronization***

The Emulator shall generate Time Codes using the SpaceWire Standard Time-code mode. (Note: The 3 GSFC defined Time Code modes are not used for SPP.)

Spacecraft time (MET) is distributed and synchronized through the SpaceWire network. Standard SpaceWire time codes are transmitted to each SpaceWire node at a 50 Hz / 20 ms cadence. The SpaceWire nodes use the 50 Hz time code interrupt to derive a 1 Hz / 1 PPS signal if needed.

*2.1.6.4 **Spacecraft Time Definition***

- Minor Frame: A 50 Hz / 20 ms interval delineated by the time codes distributed over the SpaceWire network.
- Major Frame: A 1 Hz / 1 PPS interval made up of 50 minor frames.

The Emulator shall provide capability to configure the Minor Frame and Major Frame rates.

2.1.7 SpaceWire Telemetry from Instrument

The Emulator receives two SpaceWire telemetry data streams from the instrument (Side A, Side B).

The Instrument will only send telemetry data when it is queried to do so. The emulator will send a request for telemetry to the instrument to which the instrument responds with the telemetry requested. The Instrument will disable the LVDS transmitter on the inactive telemetry interface. The Emulator shall provide capability to monitor/detect erroneous traffic on the inactive side. (See section 2.5)

The Telemetry SpaceWire signaling data rate (ie., raw bit rate) is 30 Mbps. The maximum data rate for WISPR Image data is 350Kbps.The telemetry signals shall be at 3.3V LVDS electrical levels. Figure 5 shows the first circuit interface for the telemetry data stream. Optical isolators shall only be used in the full Emulator. The LVDS receiver shall be electrically equivalent to the flight part.

The Emulator FPGA shall add clock recovery circuitry to avoid use of PHY chips.

2.1.8 SpaceWire Parameters and Polarity

SpaceWire uses Data-Strobe (DS) encoding. This is a coding scheme which encodes the transmission clock with the data into Data and Strobe so that the clock can be recovered by simply XORing the Data and Strobe lines together. The data values are transmitted directly and the strobe signal changes state whenever the data remains constant from one data bit interval to the next. This coding scheme is illustrated in Figure 10. The reason for using DS encoding is to improve the skew tolerance to almost 1-bit time, compared to 0.5 bit time for simple data and clock encoding.

A SpaceWire link comprises two pairs of differential signals, one pair transmitting the D and S signals in one direction (Command) and the other pair transmitting D and S in the opposite direction (Telemetry). That is a total of eight wires for each bidirectional link.

Data bit values are true logic (not inverted) at the input to the driver, the “+” output of the driver, and the output to the receiver.

At the output of the driver, a logic one means the “+” output is high and the “-“output is low. For a logic zero, the “+” output is low and the “-“output is high. This polarity is shown in Figure 10.

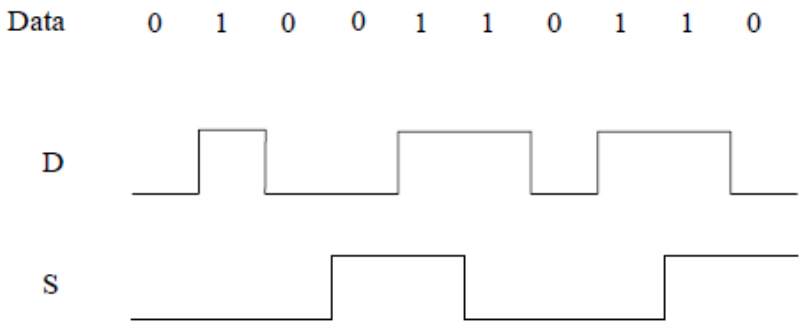


Figure 10. SpaceWire Data-Strobe Encoding

2.1.9 SpaceWire Character level Protocol

There are two types of characters:

- Data characters, which hold an eight-bit data value, are transmitted least significant bit first. Each data character contains a parity bit, a data-control flag and the eight bits of data. The parity bit covers the previous eight bits of a data character or two bits of a control character, the current parity bit and the current data-control flag. It is set to produce odd parity so that the total number of 1's in the field covered is an odd number. The data-control flag is set to zero to indicate that the current character is a data character.
- Control characters which hold two control bits. Each control character is formed from a parity bit, a data-control flag and two control bits. The data-control flag is set to one to indicate that the current character is a control character. Parity coverage is similar to that for a data character. One of the four possible control characters is the escape code (ESC). This can be used to form control codes. Two control codes are specified and valid which are the NULL code and the Time-Code.
    - NULL is formed from ESC followed by the flow control token (FCT). NULL is transmitted whenever a link is not sending data or control tokens, to keep the link active and to support link disconnect detection.
    - The Time-Code is used to support the distribution of system time across a network. A Time-Code is formed by ESC followed by a single data-character. The data and control characters are illustrated in Figure 11.

Note: See ECSS-E-ST-50-12C, for Exchange level and Packet Level and Network Level protocols.

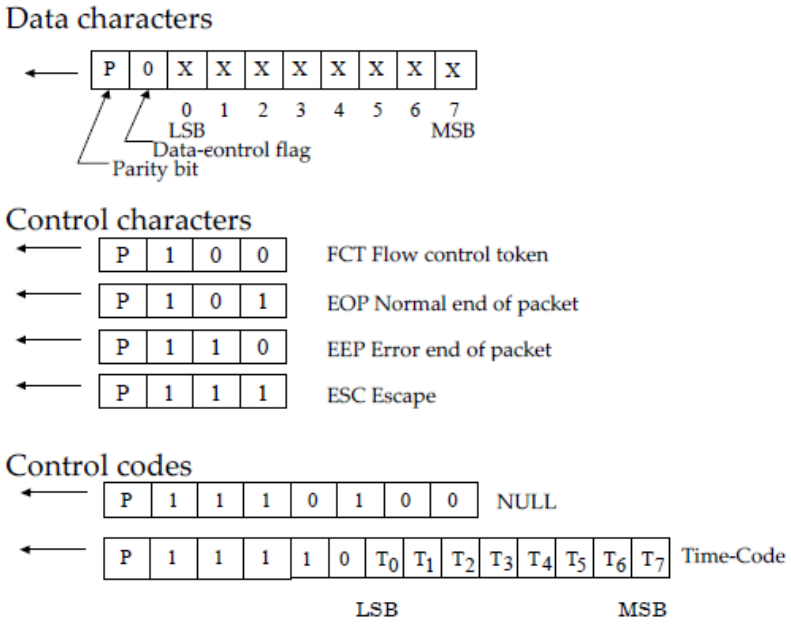


Figure 11. SpaceWire Data and Control Characters

2.1.10 SpaceWire RMAP Protocol

The Emulator shall provide Remote Access Memory Protocol (RMAP) for SpaceWire which is a standard method of reading and writing to registers and memory within a SpaceWire unit by sending a command and where appropriate receiving a reply.

The Emulator shall implement RMAP in embedded software.

The Emulator shall provide RMAP error detection capability. (See section 2.5)

*2.1.10.1 **RMAP Write Sequence***

The Emulator shall provide the command interfaces (as defined in 2.1.9.3) to the WISPR DPU in accordance with the requirements of the RMAP write sequence as defined in section 3.1.1 of the SPP SpaceWire ICD, 7434-9075.

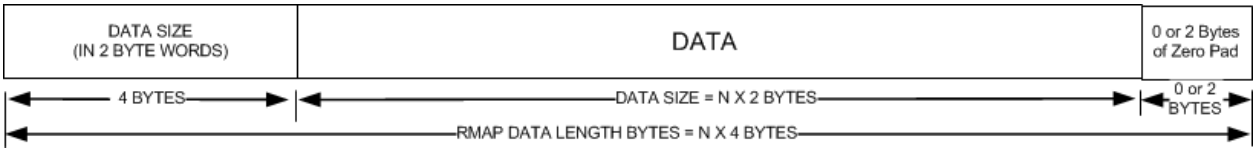
*2.1.10.2 **RMAP Read Sequence***

The Emulator shall provide the telemetry interfaces (as defined in 2.1.9.4 and 2.1.9.5) to the WISPR DPU in accordance with the requirements of the RMAP write sequence as defined in section 3.1.2 of the SPP SpaceWire ICD, 7434-9075.

*2.1.10.3 **RMAP Command Interface Data Structure***

The RMAP Command Interface definition for the WISPR DPU is as follows:

- A command buffer starting with a 32-bit size value. The size and data are contiguous.
- The size value indicates the number of 16-bit words of valid data that follow.
- The size value does not include the (optional) Zero Pad bytes.
- The command buffer (DATA) must be an integer number of 16-bit words and include space for an optional 2 bytes of zero pad so that RMAP transfers may be padded to modulo 32-bit words.



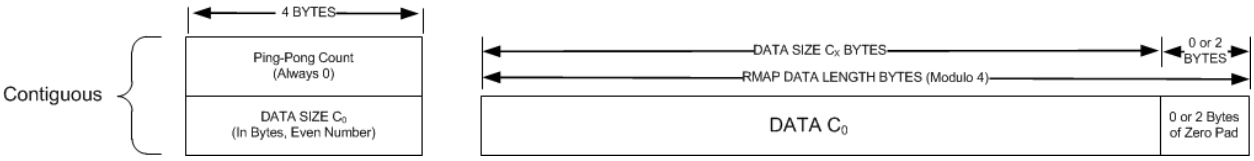
*2.1.10.4 **RMAP Low Speed Housekeeping Telemetry Interface Data Structure***

The RMAP Housekeeping Low Speed Telemetry Interface definition for the WISPR DPU is as follows:

- A data buffer with an associated size and ping-pong value. However, the ping-pong value is always zero.

- Emulator uses one base address and WISPR resolves it to either the ping or pong buffer.

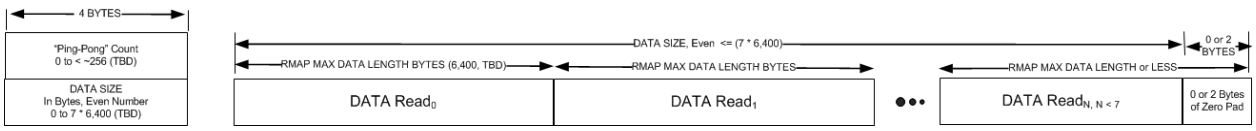
- The Emulator will read the size and then use that information to read the data buffer.
- The data buffer does not have to be contiguous with the size value, but may be.
- The data buffer must be an integer number of 32-bit words with two bytes of zero padding after the data, if necessary. This is an RMAP implementation restriction.
- The data (the ITFs) shall be an integral number of 16-bit words.



*2.1.10.5 **RMAP High Speed Image Telemetry Interface Data Structure***

The RMAP High Speed Image Telemetry Interface definition for the WISPR DPU is as follows:

- An image buffer may be much larger than the amount of data that can be transferred in one major frame. Only 350 * 2^10 bits of image data may be transferred in one major frame.
- The Emulator will read a maximum of 6,400 bytes (50 * 2^10 bits) at a time (TBD). To read 350 * 2^10 bits in one major frame, 7 RMAP reads (TBD) will be used.
- A so-called “ping-pong counter” will keep track of the major frames of image data.
- The image buffer will have a base address known to the Emulator. The base address and the “ping-pong count” will be used at start of a major frame to calculate the base address for the reads during that frame.
- The Emulator will advance the calculated base address up to 7 times (TBD) during the major frame in order to read up to 325 * 2^10 bits of data.
- The Emulator will not read more data than indicated by the size value.



2.2 USB Interface

The USB interface has two purposes. During initialization it downloads the FPGA configuration file into the Opal-Kelly daughter card. After initialization, the USB interface is used to transfer four data streams between the Emulator and the GSEOS PC:

1) Commands to instrument (115.2 Kbps)
2) Telemetry from Instrument (115.2 Kbps to 345.6 Kbps)
3) Command and Control data to Emulator (rate only needs to average 19.2 Kbps)
4) Status from Emulator (rate only needs to average 19.2 Kbps)

2.2.1 Instrument Commands (USB)

GSEOS shall send instrument commands using the Opal-Kelly PIPEIN mechanism (PIPE 80). The Emulator shall provide a 512x16 FIFO for storing commands sent from GSEOS. The space (words) in this FIFO can be read by GSEOS using WIREOUT(20).

Instrument commands are formatted into SPP ITF packets by GSEOS but the Emulator has no knowledge of ITF and does not parse ITF packets. Instead, the command data sent from GSEOS is embedded into a separate packet protocol called FTF (FIFO Transfer Frame). Header and control words in this packet specify the amount of ITF data in the packet and the time to send the ITF packet to the instrument. Using this mechanism, GSEOS shall have the ability to set the command data output times within 10 milliseconds (TBR) in each virtual 1PPS frame. Also, the Emulator registers an error if the command output fails to complete prior to 100 milliseconds before the end of the 1 PPS period.

A raw command output mode shall ALSO be provided where command data is transferred directly from GSEOS to the instrument without any ITF packet layering. For details about the data content and the ITF format see the GII. For details about the FTF format see the SPP Bios Manual (part of the GSEOS download).

Note: The SPP Command ITF contains CCSDS Command packets.

2.2.2 Instrument Telemetry (USB)

Telemetry data from the instrument shall be sent to GSEOS using the Opal-Kelly PIPEOUT A0. A 2K x 16 word FIFO shall be provided for storing telemetry words associated with PIPE A0. The WIREOUT 23 status bits shall indicate to GSEOS the words available in this FIFO. GSEOS reads the words as they are available. Telemetry data received from the instrument is in the SPP ITF format but the Emulator has no knowledge of ITF packets. Instead, the Emulator inserts the ITF data into FTF (FIFO Transfer Frame) packets. There is no restriction on the amount of ITF data within an FTF packet but nominally, the Emulator shall build FTF packets each 100 ms.

The Emulator shall report the arrival time of the first byte of Telemetry data in each 1PPS frame. Nominally, complete telemetry packets are received in 1PPS frames. The Emulator shall report an error condition if telemetry data continues beyond the 990 milliseconds point within a virtual 1PPS frame.

For details about the FTF packet format see the SPP Bios manual. For details about the Telemetry ITF format, see the GII.

Note: The SPP Telemetry ITF contains CCSDS Telemetry packets.

2.2.3 Emulator Status (USB)

Status data from the Emulator shall be sent to GSEOS using the Opal-Kelly PIPEOUT A1. A 512 x 16 word FIFO shall be provided for storing status words associated with PIPE A1. The WIREOUT 24 status bits shall indicate to GSEOS the words available in this FIFO.

Emulator status packets are divided into two major categories, *FPGA status* and *Analog status*. *FPGA status* shall provide information specific to activities in the Opal Kelly FPGA, such as progress of the command frame decoding, arrival times of the telemetry packets, UART commanded baud rates, CMD packet decoding status etc. The FTF status packets are described in the SPP Bios Manual.

Analog status packets (only functional in the FULL Emulator) provide instrument currents, voltages, temperatures and power switch on/off settings. See the SPP Bios Manual for details about the format of the FTF Status packets.

2.2.4 Emulator Commands/Control (USB)

GSEOS shall send Emulator commands using the Opal-Kelly PIPEIN mechanism (PIPE 81). The Emulator shall provide a 512x16 FIFO for storing Emulator commands sent from GSEOS. The space (words) in this FIFO can be read by GSEOS using WIREOUT(21). All Emulator command packets shall be in the FTF format.

Emulator commands can be divided into two categories, FPGA configuration and Analog configuration. FPGA type packets control the operation of the FPGA by setting data multiplexers, data input enables, 1PPS enables, UART data rates and major/minor frame sizes. The FPGA packet shall provide the controls necessary for forcing error conditions. (See Section 2.3)

The Analog control packets are only functional on the FULL emulator and are used to open/close power switches, set current/voltage limits and control the sampling of the analog sensors. For details about the Emulator commands see the SPP Bios Manual.

2.2.5 1PPS EGSE Test Interface Output Control

*2.2.5.1 **1PPS Control***

The 1PPS Gated pulse shall be controlled using an Emulator Command (FPGA type command). The enable/disable state shall be controllable from GSEOS.

2.2.6 PPS Gated1 EGSE Test Interface Output Control

*2.2.6.1 **PPS_GATED1 Control***

The PPS_Gated1 pulse shall be controlled using an Emulator Command (FPGA type command). The arm/disarm state, pulse width and delay (0 to 1 second) of the pulse relative to 1PPS shall be controllable from GSEOS. The programmable pulse width resolution shall also be 1 microsecond. The programmable delay resolution shall be 1 microsecond.

The PPS_Gated1 pulse shall be output only after the arm state has been commanded. The PPS_Gated1 pulse shall be output on the subsequent (next) 1 PPS cycle from when the arm

command was received (not the current 1 PPS cycle). The arm state shall be armed for just 1 PPS cycle then automatically transition to the disarm state. The arm state must then be re-armed from GSEOS to generate the next output.

2.2.7 PPS Gated2 EGSE Test Interface Output Control

*2.2.7.1 **PPS_GATED2 Control***

The PPS_Gated2 pulse shall be controlled using an Emulator Command (FPGA type command). The arm/disarm state, pulse width and delay (0 to 1 second) of the pulse relative to 1PPS shall be controllable from GSEOS. The programmable pulse width resolution shall also be 1 microsecond. The programmable delay resolution shall be 1 microsecond.

The PPS_Gated2 pulse shall be output only after the arm state has been commanded. The PPS_Gated2 pulse shall be output on the subsequent (next) 1 PPS cycle from when the arm command was received (not the current 1 PPS cycle). The arm state shall be armed for just 1 PPS cycle then automatically transition to the disarm state. The arm state must then be re-armed from GSEOS to generate the next output.

2.3 Forced Error Conditions for UART Interfaces

The Emulator shall have the ability to force the following errors. The UART errors only apply to the CMD UART, not the TLM UART.

a) Off Frequency UART data rates: The Emulator's CMD TX UART data rate is programmable from GSEOS. Data rates from 38.4 Kbps to 345.6 Kbps are programmable with a resolution of 0.2 % from GSEOS. Using this mechanism, the off-frequency or erroneous UART data rates can be simulated.

b) UART Parity Errors (force parity error): GSEOS shall have the ability to set the CMD UART parity level. Parity errors shall be simulated by setting an incorrect level for parity.

c) UART Framing Errors: The STOP bit polarity can be selected from GSEOS. This is how framing errors shall be simulated.

d) 1PPS Test Output disappearance: Since GSEOS can enable/disable the 1PPS output, this error can simulated by disabling 1PPS.

e) Virtual 1PPS Output disappearance: Since GSEOS can control the UART command output; this error can be simulated by not sending a command.

f) ITF command packet errors and out of sequence counts shall be forced within GSEOS without interaction from the Emulator hardware. This feature can be implemented by building a raw command with purposeful ITF errors. A feature shall be provided where the user can construct an entire block (either ITF of ITF-CCSDS) with errors embedded into the block.

2.4 Error Detection for UART Interfaces

The Emulator shall provide error detection capability as follows. The UART error detection features only apply to the TLM UART, not the CMD UART.

a) The Emulator shall provide capability to monitor/detect erroneous UART traffic on the inactive side. Activity detection will consists of a simple check to detect erroneous signal transitions. (ie., there should be none.)

2.5 SpaceWire/RMAP Error Detection

The Emulator shall provide SpaceWire error detection capability as follows.

1. Link Disconnected : Flag if at any time during the 1pps the link disconnected
2. SpaceWire Error : This is a flag that is set if there was a parity error or flow control error any time during the 1pps interval
3. Timecode Error : This is a flag that is set if an out of sequence time code was received during the 1pps interval
   The Emulator shall provide capability to monitor/detect erroneous SpaceWire traffic on the inactive side. Activity detection will consists of a simple check to detect erroneous signal transitions. (ie., there should be none.)

The Emulator shall provide RMAP error detection capability as follows:

1. The Emulator shall monitor for incoming activity to verify the WISPR DPU isn't sending non-RMAP traffic.
2. RMAP Error: (TBR)
3. More detection capability to be added (TBR)

2.6 SpaceWire/RMAP Error Injection

The Emulator shall have the ability to force the following SpaceWire errors.

a) Valid SpW Read with invalid (i.e. out-of-bounds) WISPR DPU Memory Address
b) Valid SpW Read with invalid data length field (not a multiple of 4 Bytes)
c) Valid SpW Write with invalid WISPR DPU Memory Address
d) Valid SpW Write with invalid length (not a multiple of 4 Bytes)
e) SpW Read Retransmission requests (per user configurable schedule or automatic retries for failed receipt at Emulator)
f) Transmit Parity Error Inject, GSFC SpW Node Spec, 561-SPEC-002, Rev D, Section 3.2.21
g) Out of Sequence Time-Code -> Verify WISPR DPU doesn't propagate the time-code; per GSFC SpW Node Spec, 561-SPEC-002, Rev D, Section 3.8.2. SCE detection via GSFC SpW Node Spec, 561-SPEC-002, Rev D, Section 3.8.4

2.7 Command Retries

For UART, the Emulator shall not support command failure retries. For SpaceWire, the Emulator shall provide capability to retry failed commands. Retried commands must complete in the minor frame that it was sent.

2.8 Instrument Power Interfaces (Full Emulator only)

Figure 12 shows the power circuits implemented in the SPP Emulator. The 30 Volt power source for the instrument and auxiliary power shall be derived from a single 30V@3A power supply. There shall be two current sensors, one for instrument power and one for auxiliary power. Similarly, there are two voltage sensors, one for instrument power and one for heater/auxiliary power. All decisions about automatic shutoff of the power FETS are based on these two pairs of sensors.

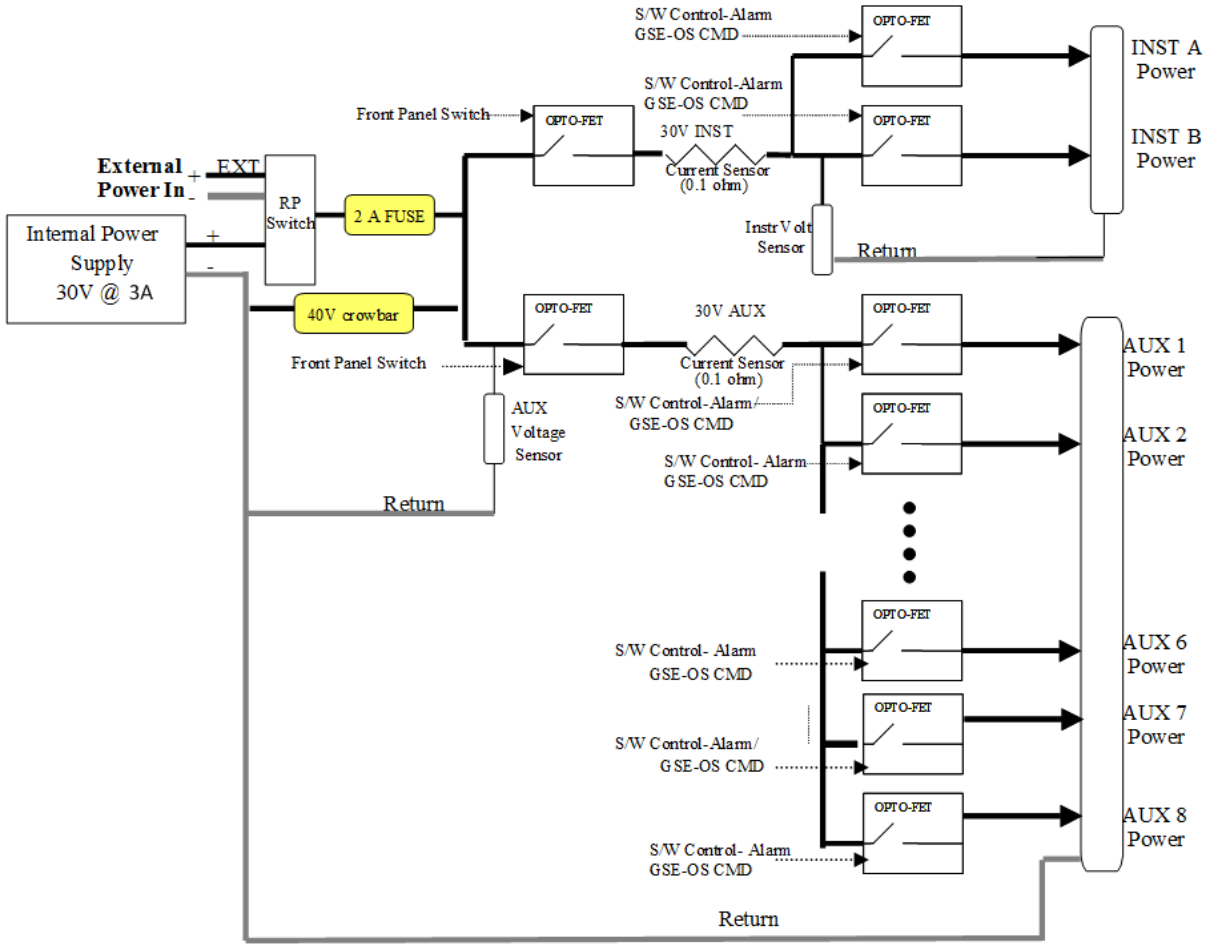


Figure 12. SpaceWire Data and Control Characters

A series of opto-FETs are used to switch power in response to either over/under current or voltage, front panel switch position or a GSEOS command from user. A single "analog packet" sent over the Emulator Command/Control path (pipe81) shall configure voltage/current limits and on/off switch settings. The status of these switch positions and status of the current/voltage trip conditions shall be reported via status packets (analog status packets) sent over the Emulator Status pipeA1. One packet shall be sent each second reporting the nominal status of current/voltage, current/voltage limits and switch settings. When a trip condition occurs, a special error packet shall be sent indicating the reason for the voltage/current trip. The Emulator shall respond to an out-of-limit current/voltage condition within 1 millisecond. The over and under current limit levels are programmable from GSEOS to within 10 ma / 10 mv.

2.9 Emulator Grounding

The Emulator grounding scheme is shown in Figure 13. The grounding scheme follows that described in 7434-9039 (SPP EMECP - Electromagnetic Environment Control Plan). All of the instrument side electronics, i.e. power switches, A/D converters, current sensors, voltage sensors shall be powered from a separate set of transformer coupled power supplies. The only link between the GSEOS side electronics (DGND) and the Instrument side electronics (AGND) shall be thru optical isolators. A 20M resistor connects to two grounds to insure that any large capacitive voltage differentials can be dissipated. Two banana jacks exposed to the rear panel shall allow connecting the GSEOS ground (CHASSIS GND) to the Instrument ground for cases where this is desirable.

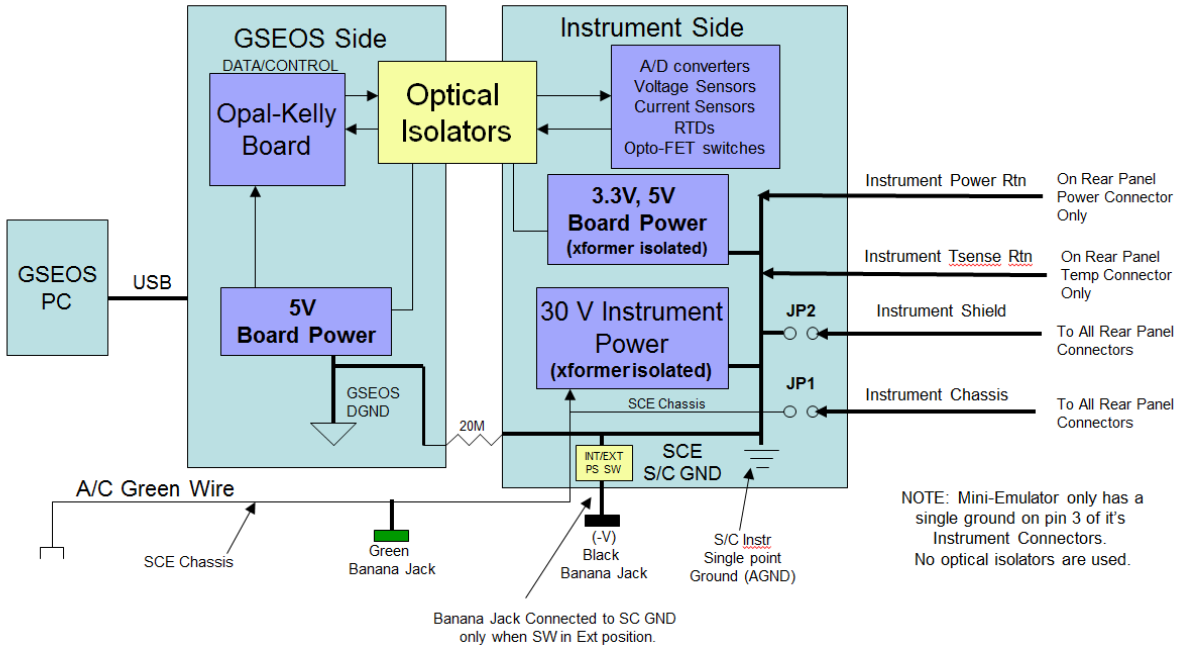


Figure 13 Emulator Grounding/Isolation Scheme

2.10 Overcurrent and Overvoltage Protection

2.10.1 Current Protection

The Emulator PCB shall provide a resettable fuse that limits the current supplied by the 30V instrument power supply to 2 amps. The internal 5V supply shall be current limited to 1 amp.

2.10.2 Overvoltage Protection

The 30V volt power supply (both internal and external) shall be crowbar limited to 35 Volts. The 5V supplies (both Instrument side and Opal-Kelly side) shall be crowbar limited to 6 Volts. The 3.3V volt supplies (derived from 5V supply) shall be Zener diode limited to 3.6V (TBR).

2.11 RTD Temperature Sensors (Full Emulator only)

The SPP Emulator shall provide eight interfaces to the instrument RTDs (Resistive Temperature Detectors). A precision current source shall be used to measure the resistance of the RTD. The resulting voltage produced by the RTD shall be measured by a 12 bit A/D converter. The raw count to resistance scaling factor shall be TBD counts/ohm. The maximum resistance will be TBD ohms. The temperature sensors are sampled/updated once per second and are included in the analog status packet sent to GSEOS.

2.12 Miscellaneous Interfaces

2.12.1 Full Emulator Front Panel

*2.12.1.1 **LCD Display***

The full Emulator shall have a front panel LCD display (20 x 4). Four values shall be displayed in real-time, Instrument Current, Instrument Voltage, Auxiliary Current, Auxiliary Voltage. Asterisks shall blink at the top of the display if an out of limit condition has occurred.

*2.12.1.2 **LED indicators***

The full Emulator front panel shall have 16 LED indicators. They show the enable/disable status of the two Instrument power outputs (GREEN) and eight Auxiliary power outputs (GREEN). A 1PPS led shall flash for approximately 100 milliseconds on each output edge of the 1PPS signal (GREEN). A Spare Indicator (GREEN) shall be provided. Four RED error LEDs shall be provided that indicates an error condition exists. Includes the following errors: GSEOS error, an out of limit current/voltage error, a UART/SpaceWire data transfer timing error (overflow, underflow, command timing overlap, telemetry timing overlap), and a CMD/TLM error.

LED Indicator Summary List

1. Instrument A PWR Status (Green)
2. Instrument B PWR Status (Green)
3. Aux 0-7 PWR Status (Green) (Total 8)

4. 1PPS (Green)
5. Spare (Green)
6. GSEOS Error, I/V Limit Error, UART/SpaceWire Error, CMD/TLM Error (RED) (Total 4)

*2.12.1.3 **Power Switches***

The full Emulator shall have two front panel power enable switches, one for Instrument power and one for Auxiliary power. These switches are in series with the GSEOS controlled power switches and provide the user with a way to disable power without using GSEOS. There shall also be a single A/C power ON/OFF switch on the Emulator front panel.

*2.12.1.4 **Instrument Data Interface Test Points***

The full Emulator shall provide UART/SpaceWire Data and Strobe Test Points as follows:

a) Din/TLM data BNC (LVTTL version of Data/TLM input data signal, buffered and at 3.3V levels).

b) Sin BNC (TTL version of Strobe input signal, buffered and at 3.3V levels).

c) Dout/CMD data BNC (LVTTL version of CMD output data signal, buffered and at 3.3V levels).

d) Sout BNC (LVTTL version of Strobe output signal, buffered and at 3.3V levels).

Note: Above signals will correspond to either the Instrument A or B interface, whichever is configured at the time.

2.12.2 Full Emulator Rear Panel

The full Emulator rear panel shall have the following connectors:

a) Instrument Data Interface A: This connector (MicroD-9F) shall provide the CMD and TLM (UART/SpaceWire) LVDS signal interface to the side A instrument. A signal ground shall also be included on this interface connector.

b) Instrument Data Interface B: This connector (MicroD-9F) shall provide the CMD and TLM (UART/SpaceWire) LVDS signal interface to the side B instrument. A signal ground shall also be included on this interface connector.

c) 1PPS, PPS_GATED1, PPS_GATED2 test point outputs, MicroD-9M (LVTTL, buffered and at 3.3V levels). Multiple signal ground pins shall also be included on this interface connector.

d) Instrument A/B and Heater/AUX Power: This connector (DSUB25F) provides two switchable 30V Instrument power outputs (with returns) and eight 30V switchable Aux power outputs (with returns). A chassis ground shall also be included on this interface connector.

e) RTD Sensors 1-8: This connector (DSUB25M) provides eight RTD sense pairs. A chassis ground shall also be included on this interface connector.

f) USB connector for connection to GSEOS PC (standard USB peripheral connector).

g) External 30V Power Input Connector: Two banana jacks (Plus (RED), Minus (BLACK)).

h) External/Internal 30V Power Supply Select Switch

i) S/C Instrument Ground: Banana jack that exposes the S/C ground for measurements or for optionally connecting to Emulator Chassis/Earth ground. (Note: This banana jack is common with External 30V Minus banana jack, and is only connected to SC ground when external power supply select switch is selected to External Power Supply)

j) GSEOS chassis / Earth Ground: Banana jack (Green) that exposes the Emulator Chassis / Earth ground.

k) AC Power Input.

2.12.3 Mini Emulator Front Panel

2.12.3.1 ***LED indicators***

The Mini Emulator front panel shall provide 3 RED LED indicators.

A +3.3V LED shall illuminate when 5V power is supplied to the mini emulator.

A 1PPS led shall flash for approximately 100 milliseconds on each output edge of the virtual 1PPS signal.

An Error LED shall indicate that a data transfer timing error (overflow, underflow, command timing overlap, telemetry timing overlap, UART error, SpaceWire error) has occurred.

2.12.3.2 ***Power Interface***

The Mini Emulator shall provide a 5V power input. Power will be received from an AC to 5V adapter cord. (The adapter cord is supplied with the Mini Emulator delivery.)

2.12.3.3 ***PC Interface***

The Mini Emulator shall provide a USB connector for connection to GSEOS PC (standard USB peripheral connector).

2.12.4 Mini Emulator Rear Panel

The Mini Emulator rear panel shall have the following connectors:

a) Instrument Data Interface A: This connector (MicroD-9F) shall provide the CMD and TLM (UART/SpaceWire) LVDS signal interface to the Side A instrument. A signal ground shall also be included on this interface connector.

b) Instrument Data Interface B: This connector (MicroD-9F) shall provide the CMD and TLM (UART/SpaceWire) LVDS signal interface to the Side B instrument. A signal ground shall also be included on this interface connector.

c) 1PPS, PPS_GATED1, PPS_GATED2 test point outputs, MicroD-9M (LVTTL, buffered and at 3.3V levels). Multiple signal ground pins shall also be included on this interface connector.

d) GSEOS Signal Ground: Barrel Connector that exposes the Emulator Signal ground.

3. APPENDIX A

3.1 Pin Out List – Mini Emulator

3.1.1 Mini Emulator (J1- Instrument A Interface)

			MINI EMULATOR PN: 7434-7110	CONNECTOR REF DES: J1 PN: M83513/13-A01CP CONN D MICRO RCPT R/A 9 SOCKET
Pin #	I/O	SIGNAL TYPE	DESCRIPTION	COMMENTS
1	I	LVDS	SpW_A_Din_UART_TLM_P	
2	I	LVDS	SpW_A_Sin _P	Not used for UART Interfaces
3		GND	GND	
4	O	LVDS	SpW_A_Sout _N	Not used for UART Interfaces
5	O	LVDS	SpW_A_Dout_UART_CMD_N	
6	I	LVDS	SpW_A_Din_UART_TLM_N	
7	I	LVDS	SpW_A_Sin _N	Not used for UART Interfaces
8	O	LVDS	SpW_A_Sout _P	Not used for UART Interfaces
9	O	LVDS	SpW_A_Dout_UART_CMD _P	

3.1.2 Mini Emulator (J2- Instrument B Interface)

			MINI EMULATOR PN: 7434-7110	CONNECTOR REF DES: J2 PN: M83513/13-A01CP CONN D MICRO RCPT R/A 9 SOCKET
Pin #	I/O	SIGNAL TYPE	DESCRIPTION	COMMENTS
1	I	LVDS	SpW_B_Din_UART_TLM_P	
2	I	LVDS	SpW_B_Sin _P	Not used for UART Interfaces
3		GND	GND	
4	O	LVDS	SpW_B_Sout _N	Not used for UART Interfaces
5	O	LVDS	SpW_B_Dout_UART_CMD_N	
6	I	LVDS	SpW_B_Din_UART_TLM_N	
7	I	LVDS	SpW_B_Sin _N	Not used for UART Interfaces
8	O	LVDS	SpW_B_Sout _P	Not used for UART Interfaces
9	O	LVDS	SpW_B_Dout_UART_CMD _P	

3.1.3 Mini Emulator (J3- EGSE PPS Test Interface)

			MINI EMULATOR PN: 7434-7110	CONNECTOR REF DES: J3 PN: M83513/10-A01CP CONN D-SUB MDM PIN R/A 9PINS
Pin #	I/O	SIGNAL TYPE	DESCRIPTION	COMMENTS
1	O	3.3V LVTTL	1PPS_TP_OUT	
2		GND	GND	
3		GND	GND	
4	O	3.3V LVTTL	PPS_GATED1_TP_OUT	(AKA: SPARE1_TP_OUT)
5	O	3.3V LVTTL	PPS_GATED2_TP_OUT	(AKA: SPARE2_TP_OUT)
6		GND	GND	
7		GND	GND	
8		GND	GND	
9		GND	GND	

3.1.4 Mini Emulator (J4- GROUND)

			MINI EMULATOR PN: 7434-7110	CONNECTOR REF DES: J4 PN: SJ1-3544N CONN BARREL- RCPT R/A
Pin #	I/O	SIGNAL TYPE	DESCRIPTION	COMMENTS
		GND	GND	All Barrel connections = ground

4. APPENDIX B

4.1 Pin Out List – Full Emulator

Note: J1, J2 are internal connectors. J4 is not used.

4.1.1 Full Emulator (J5- Instrument A Interface)

			FULL EMULATOR PN: 7434-7xxx	CONNECTOR REF DES: J5 PN: M83513/13-A01CP CONN D MICRO RCPT R/A 9 SOCKET
Pin #	I/O	SIGNAL TYPE	DESCRIPTION	COMMENTS
1	I	LVDS	SpW_A_Din_UART_TLM_P	
2	I	LVDS	SpW_A_Sin _P	Not used for UART Interfaces
3		GND	GND	
4	O	LVDS	SpW_A_Sout _N	Not used for UART Interfaces
5	O	LVDS	SpW_A_Dout_UART_CMD_N	
6	I	LVDS	SpW_A_Din_UART_TLM_N	
7	I	LVDS	SpW_A_Sin _N	Not used for UART Interfaces
8	O	LVDS	SpW_A_Sout _P	Not used for UART Interfaces
9	O	LVDS	SpW_A_Dout_UART_CMD _P	

4.1.2 Full Emulator (J6- Instrument B Interface)

			Full EMULATOR PN: 7434-7xxx	CONNECTOR REF DES: J6 PN: M83513/13-A01CP CONN D MICRO RCPT R/A 9 SOCKET
Pin #	I/O	SIGNAL TYPE	DESCRIPTION	COMMENTS
1	I	LVDS	SpW_B_Din_UART_TLM_P	
2	I	LVDS	SpW_B_Sin _P	Not used for UART Interfaces
3		GND	GND	
4	O	LVDS	SpW_B_Sout _N	Not used for UART Interfaces
5	O	LVDS	SpW_B_Dout_UART_CMD_N	
6	I	LVDS	SpW_B_Din_UART_TLM_N	
7	I	LVDS	SpW_B_Sin _N	Not used for UART Interfaces
8	O	LVDS	SpW_B_Sout _P	Not used for UART Interfaces
9	O	LVDS	SpW_B_Dout_UART_CMD _P	

4.1.3 Full Emulator (J3- EGSE PPS Test Interface)

			FULL EMULATOR PN: 7434-7xxx	CONNECTOR REF DES: J3 PN: M83513/10-A01CP CONN D-SUB MDM PIN R/A 9PINS
Pin #	I/O	SIGNAL TYPE	DESCRIPTION	COMMENTS
1	O	3.3V LVTTL	1PPS_TP_OUT	
2		GND	GND	
3		GND	GND	
4	O	3.3V LVTTL	PPS_GATED1_TP_OUT	(AKA: SPARE1_TP_OUT)
5	O	3.3V LVTTL	PPS_GATED2_TP_OUT	(AKA: SPARE2_TP_OUT)
6		GND	GND	
7		GND	GND	
8		GND	GND	
9		GND	GND	

4.1.4 Full Emulator (P1 – Instrument Power)

			FULL EMULATOR PN: 7434-7xxx	CONNECTOR REF DES: P1 PN: DSUB25F CONN D-SUB SOCKET R/A 25 SOCKET
Pin #	I/O	SIGNAL TYPE	DESCRIPTION	COMMENTS
1	O	Instr PWR	Instrument Power Out 1	
2	O	Instr RTN	Instrument Power Return	
3	O	Instr RTN	Instrument Power Return	
4	O	Instr PWR	AUX Power Out 1	
5	O	Instr PWR	AUX Power Out 2	
6	O	Instr PWR	AUX Power Out 3	
7	O	Instr PWR	AUX Power Out 4	
8	O	Instr PWR	AUX Power Out 5	
9	O	Instr PWR	AUX Power Out 6	
10	O	Instr PWR	AUX Power Out 7	
11	O	Instr PWR	AUX Power Out 8	
12	O	Instr RTN	Instrument Power Return	
13		Instr Chassis GND	Instrument Chassis Ground	
14	O	Instr RTN	Instrument Power Return	
15	O	Bus PWR	Instrument Power Out 2	
16	O	Instr RTN	Instrument Power Return	
17	O	Instr RTN	Instrument Power Return	
18	O	Instr RTN	Instrument Power Return	
19	O	Instr RTN	Instrument Power Return	
20	O	Instr RTN	Instrument Power Return	
21	O	Instr RTN	Instrument Power Return	
22	O	Instr RTN	Instrument Power Return	
23	O	Instr RTN	Instrument Power Return	
24	O	Instr RTN	Instrument Power Return	
25		Instr Shield GND	Instrument Shield Ground	

4.1.5 Full Emulator (P2 – Instrument RTD Sensors)

			FULL EMULATOR PN: 7434-7xxx	CONNECTOR REF DES: P2 PN: DSUB25M CONN D-SUB PIN R/A 25 PIN
Pin #	I/O	SIGNAL TYPE	DESCRIPTION	COMMENTS
1	I	Temp Sense	Temp Sense 1	
2	I	Temp Sense	Temp Sense 2	
3	I	Temp Sense	Temp Sense 3	
4	I	Temp Sense	Temp Sense 4	
5	I	Temp Sense	Temp Sense 5	
6	I	Temp Sense	Temp Sense 6	
7	I	Temp Sense	Temp Sense 7	
8	I	Temp Sense	Temp Sense 8	
9				
10				
11		Instr Shield GND	Instrument Shield Ground	
12				
13		Instr Chassis GND	Instrument Chassis Ground	
14	I	Temp Sense RTN	Temp Sense Return	
15	I	Temp Sense RTN	Temp Sense Return	
16	I	Temp Sense RTN	Temp Sense Return	
17	I	Temp Sense RTN	Temp Sense Return	
18	I	Temp Sense RTN	Temp Sense Return	
19	I	Temp Sense RTN	Temp Sense Return	
20	I	Temp Sense RTN	Temp Sense Return	
21	I	Temp Sense RTN	Temp Sense Return	
22				
23		Instr Shield GND	Instrument Shield Ground	
24				
25		Instr Chassis GND	Instrument Chassis Ground	

4.1.6 Full Emulator (JBNC1 – DATA IN/TLM TP)

			FULL EMULATOR PN: 7434-7xxx	CONNECTOR REF DES: JBNC1 PN: BNC CONN BNC
Pin #	I/O	SIGNAL TYPE	DESCRIPTION	COMMENTS
1	O	3.3V LVCMOS	Data In/TLM Test Point	Note: Side A/B signal Select by GSEOS
2	O	SIG GND	Signal Ground	

4.1.7 Full Emulator (JBNC2 – STROBE IN TP)

			FULL EMULATOR PN: 7434-7xxx	CONNECTOR REF DES: JBNC2 PN: BNC CONN BNC
Pin #	I/O	SIGNAL TYPE	DESCRIPTION	COMMENTS
1	O	3.3V LVCMOS	Strobe In Test Point	Note: Side A/B signal Select by GSEOS
2	O	SIG GND	Signal Ground	

4.1.8 Full Emulator (JBNC3 – DATA OUT/CMD TP)

			FULL EMULATOR PN: 7434-7xxx	CONNECTOR REF DES: JBNC1 PN: BNC CONN BNC
Pin #	I/O	SIGNAL TYPE	DESCRIPTION	COMMENTS
1	O	3.3V LVCMOS	Data Out/CMD Test Point	Note: Side A/B signal Select by GSEOS
2	O	SIG GND	Signal Ground	

4.1.9 Full Emulator (JBNC4 – STROBE OUT TP)

			FULL EMULATOR PN: 7434-7xxx	CONNECTOR REF DES: JBNC2 PN: BNC CONN BNC
Pin #	I/O	SIGNAL TYPE	DESCRIPTION	COMMENTS
1	O	3.3V LVCMOS	Strobe Out Test Point	Note: Side A/B signal Select by GSEOS
2	O	SIG GND	Signal Ground	

4.1.10 Full Emulator (External 30V Power Supply Input)

			FULL EMULATOR PN: 7434-7xxx	CONNECTOR REF DES: +V/-V/Chassis GND PN: Banana socket CONN Banana Socket
Pin #	I/O	SIGNAL TYPE	DESCRIPTION	COMMENTS
+V	I	30V	External 30 V Power Supply Input	Red Banana Socket
-V	I	30V RTN	External 30 V Power Supply Return	Black Banana Socket
GND		Chassis GND	Chassis Ground	Green Banana Socket

5. APPENDIX C

5.1 TBD List

5.1.1 Instrument Power Interfaces

Table below shows the Instrument Power Interface requirements for each instrument. For Reference only to show that the Emulator provides adequate quantity of power interfaces, will be removed when document is released.

Several Issues/TBDs, need confirmation from Instrument team, as noted below.

SPP Emulator Power Services Requirements

Emulator Baseline Internal Power Services Capability

Service Type	Output I (Max)	QTY
Instrument PWR	3A total Instru+ Aux outputs	2
AUX PWR	3A total Instru+ Aux outputs	8
TEMP	NA	8

(Internal power supply = 30V @3amps)

Instrument Power Services Needs

Main	Instrument	Description	Total QTY	PWR (W)	I (amps)	Emulator Meets Instrument Needs?	Comments
1	WISPR-Instrument	Main	1	15	0.68	Yes	
	WISPR-Aux		4			Yes	
		(WISPR Surv HTR)		3.4	0.10	Yes	per E. Adams 5/10/13
		(OP HTR)		4.6	0.13	Yes	per E. Adams 5/10/13
		(Door Deploy A/B-2)		90	3.00	No	per E. Adams 4/26/13, 3 Amps @ 28 V for 40 ms
2	FIELDS-Instrument	PRI & MAG	1	20	0.91	Yes	
	FIELDS-Aux		7 + 8 TBD			No	
		(MAG and SCM OP & Surv HTR)		?		?	
		(Ant Deploy whips Cage 1-4A)	4 TBD	?		?	5A total?
		(Ant Deploy whips Cage 1-4B)	4 TBD	?		?	5A total?
		(Ant Deploy Hinge 1A) TINI pin puller		43.75	1.25	?	
		(Ant Deploy Hinge 2A)		?		?	
		(Ant Deploy Hinge 3&4A)		?		?	
		(Ant Deploy Hinge 3B) TINI pin puller		43.75	1.25	?	
		(Ant Deploy Hinge 4B)		?		?	
		(Ant Deploy Hinge 1&2B)		?		?	
3	SWEAP-Instrument	Main	1	12	0.55	Yes	
	SWEAP-Aux		2			Yes	
		(Cover Deploy A/B-2)		?		?	
4	ISIS-EPI HI-Instrument	Main	1	6	0.27	Yes	
	ISIS-EPI HI-Aux		2			Yes	
		(Surv & Warm Up HTR)		3.2	0.09	Yes	per E. Adams 5/6/13
		(OP HTR)		0.33	0.01	Yes	per E. Adams 5/6/13
5	ISIS-EPI LO Instrument	Main	1	5	0.23	Yes	
	ISIS-EPI LO -Aux		1			Yes	
		(Surv &Warm Up HTR)		2.5	0.07	Yes	per E. Adams 5/6/13

Note: Current Loads calculated based on Bus Voltage for resistive loads = 35V, Bus Voltage for constant loads = 22V	35
Note: Above requirements based on SPP Power Services file: PDU Services - 1-30-2013.xlsx, Updated per E. Adams	22

5.1.2 Instrument Temp Sensor Interfaces

Table below shows the Instrument Temp Sensor Interface requirements for each instrument. For Reference only to show that the Emulator provides adequate quantity of Temp sensor interfaces, will be removed when document is released.

All quantities confirmed with Instrument Team, Emulator provides adequate number of Temp Sensors.

Instrument RTD Temperature Sensor Needs

Main	Instrument	Description	Total QTY			Emulator Meets Instrument Needs?	Comments
1	WISPR-Instrument	RTD TEMP	6			Yes	per E. Adams 4/23/13
2	FIELDS-Instrument	RTD TEMP	8			Yes	per E. Adams 6/08/13
3	SWEAP-Instrument	RTD TEMP	8			Yes	per E. Adams 6/08/13
4	ISIS-EPI HI-Instrument	RTD TEMP	3			Yes	per E. Adams 4/23/13
5	ISIS-EPI LO Instrument	RTD TEMP	3			Yes	per E. Adams 4/23/13