# 13May22LVPSPeerReview

Wednesday, May 22, 2013
7:19 PM

**LVPS Peer Review**
*Reviewee*: David Do
*Reviewers*: Jim Johnson (SwRI), Samuel Kerem (APL), Uno Carlsson (APL), Steve Jaskulek (APL), Rick Cook (Caltech), Branislav Kecman (Caltech)
*Chair*: John Dickinson, Nigel Angold

*Action item legend:*
@[Actionee] AI ([Requestor]): [Action]

*Actions:*
@Dickinson AI (Jaskulek): Can the redundant primary side power signals from the spacecraft be tied together on the LVPS?
    Where is the isolation protection between side A and B maintained: S/C or instrument?
@Dickinson AI (Jaskulek): Work with Project to determine how Op Heater power is received by instrument
    Is it along with instr. primary power, or is it a separate service
@Do AI (Johnson): Look into freewheeling diodes around the normal mode inductors
    Can reduced conducted emissions in EMI
@Do AI (Kerem): Consider fuses or series diodes across D8/D9 diodes to reduce single point failures
@Do AI (Johnson): Consider thermal analysis and part packaging for Q20
    TO-205 can might not conduct heat adequately compared to the amount dissipated in the component
@Do AI (Johnson): Suggestion: fast-and-soft Shotkey across the switching FET (Q20)
    An RC is another option, but is lossy
@Do AI (Johnson): Suggestion: Ferrite bead/small inductor for differential mode noise rejection on low voltage outputs
    Differential inductance for the LC filter on the output
    Add a freewheeling diode across the ferrite bead
@Do AI (Carlsson): Safety - Perform a short-circuit analysis for safety purposes on low-voltage outputs
    Based on analysis results, possible design implications may be appropriate
@Do AI (Jaskulek): Verify that the resistance/capacitance between primary to secondary is within SPP EMI Spec
@Do AI (Kerem): Fix note "GNDP is tied to GND at U1-**18**"
@Do AI (Kerem/Kecman): Add a page/key that indicates how grounds are connected
@Do AI (everyone): Linear Regulator (U4) is positive feedback; should be negative
@Do AI (Jaskulek): Safety - what happens to other voltages when the a voltage rail is shorted?
    Part of short-circuit analysis
@Do AI: (Johnson) consider Active current limiting on the output of the linear regulators to prevent going to cycle-by-cycle limiting on the switcher
@Do AI (Dickinson): Refine the output loads and provide capability table to EPI-Hi for review
@EPI-Hi AI (Cook): Review min/max voltage and determine where error budget is bookept
    Shouldn't all be kept at the LVPS
@Do AI (Jaskulek): If operational heater is added to primary power bus, do not include

heater power in primary current sense circuit
@Do AI (Kecman): EPI-Hi will supply the a thermistor (made to GSFC spec)
@EPI-Hi AI: Send thermistor datasheet/spec; Do will test the thermistor in board checkout
    EPI-Hi will provide the component; Do will fabricate it (install on board)
@Do AI (EPI-Hi): Requests to do a quick EMI test on EM board
    Conducted emissions is the only practical test
    To be determined whether this is done at APL's or Caltech's facility
@EPI-Hi AI (Jaskulek): Provide mechanical information on LVPS EMI shield
@Dickinson AI (Jaskulek): Ensure Do has a contact for the thermal analysis
    Answer: Greg Dirks at SwRI
@Do AI (EPI-Hi): Perform a follow-up layout review
    Layout will be done in Expedition
@Dickinson AI: When does EPI-Hi need the LVPS in the schedule
    From the LVPS spec: Jan 23, 2014
@Do AI (EPI-Hi): Indicate on schematic which portions should have primary vs. secondary side EMI shielding to leave room on parts placement for gold-plated footprint (to be incorporated by EPI-Hi mechanical engineering)
@Do AI (EPI-Hi, Dean): Suggestion: put electrostatic isolation between the primary and secondary transformer windings
    Determine how/if it should be done
    Meant to clean-up switching noise
    Otherwise, you'll have a hard time meeting the spec for ripple
@Do AI (Johnson): Look at using a reset winding

*Notes:*
Design review focused on EPI-Hi LVPS Design
    EPI-Lo LVPS review was held a few weeks ago
PWM Closed Loop analysis: Results: able to achieve:
    60-70% phase margin
    10dB gain margin
6V load is very steady; 12V varies
    2.5% regulation capability
+6 is regulated on EPI-Hi boards; -6V/+12 is not regulated
All outputs are 0.1V above nominal name (for rails)
What is running off the -6V? only the bias supply, which is always on
    The supply can turned down, but is always a load
Cook: who builds the transformers: APL, maybe outside supplier/vendor
As long as linear regulator circuit works (with the correct polarity), it is fine
    However, Kerem and Johnson could not intuitively verify the operation of the circuit
EPI-Hi requests 2x capability over for max load
    This could lead to design changes
    Decision: Do to determine capability of design and EPI-Hi to respond concerning adequacy
Design employs low side current sense
EPI-Hi ADC system is 0-5V (0-4.5V would be very safe)
    Gain of 10; 5V per 1A