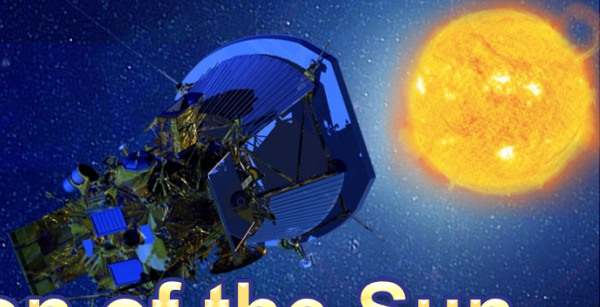
Solar Probe Plus

A NASA Mission to Touch the Sun



Integrated Science Investigation of the Sun
Energetic Particles

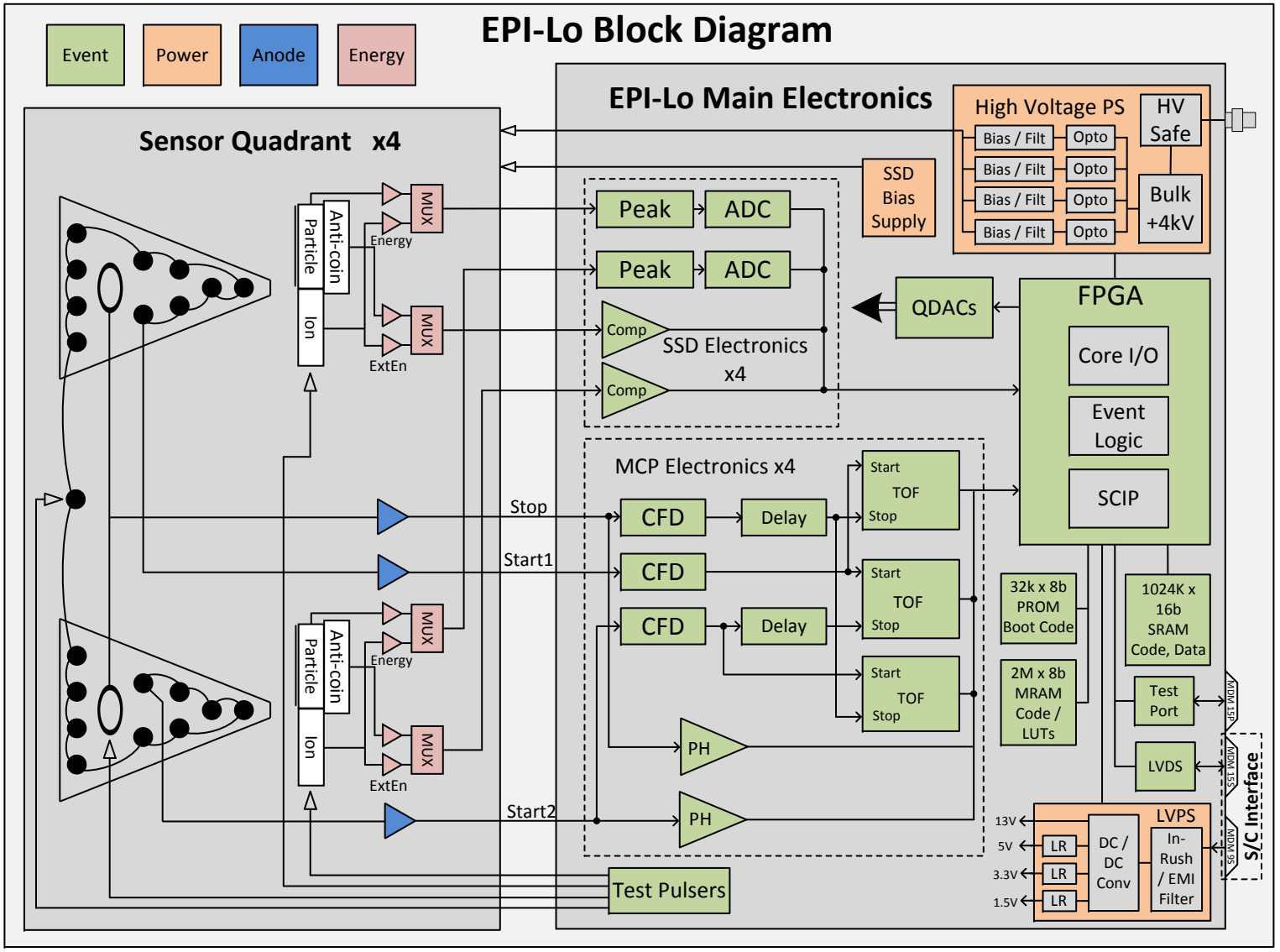
EPI-Lo Event Board FPGA EDR

Marian Stokes
John Hayes

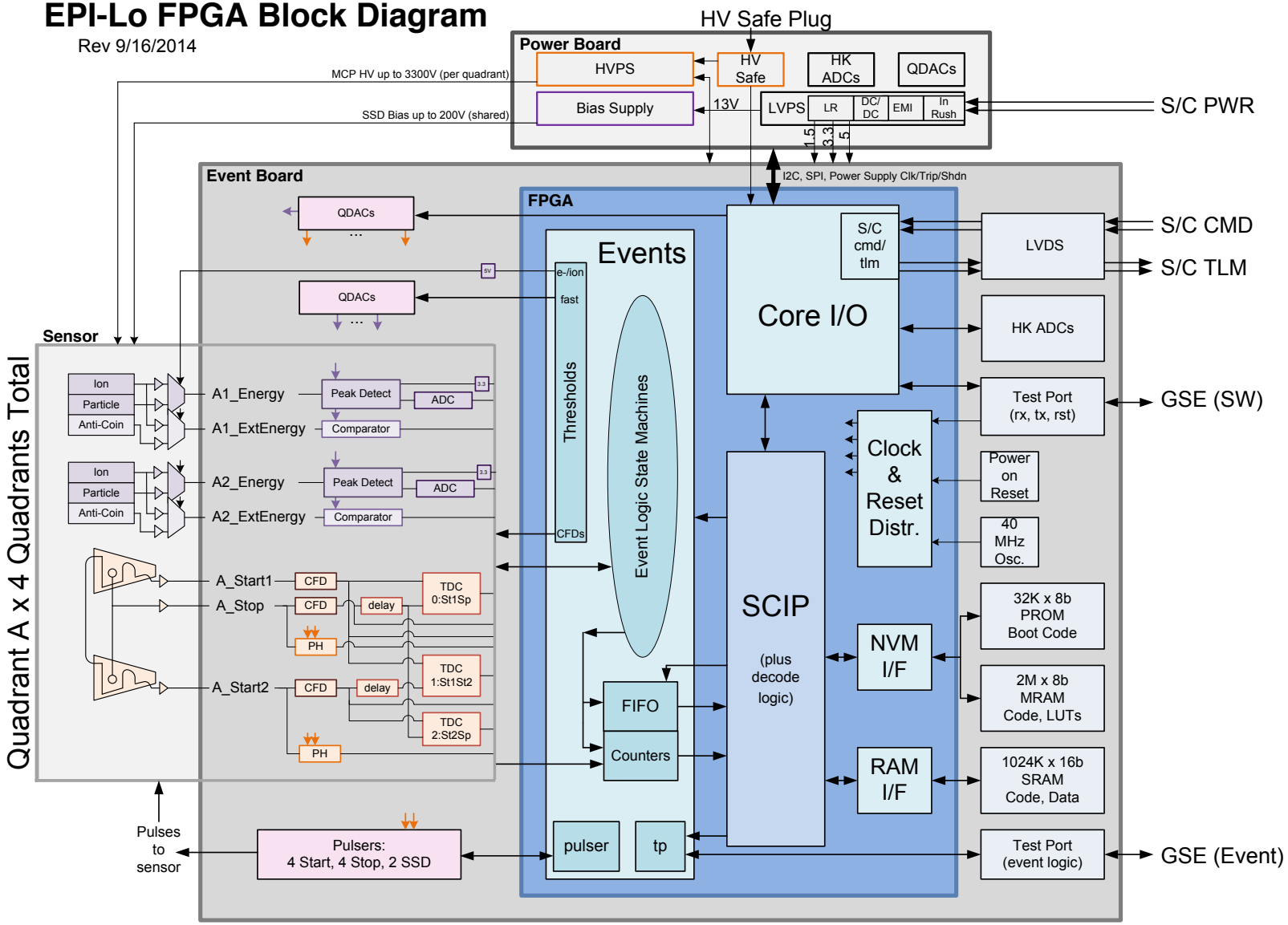
Outline

- Block diagrams
- Requirements
- Development Path
- Resource requirements
- Timing analysis
- Power analysis
- Remaining EM work
- Remaining FM preparation work
- Detailed design description
- Summary

EPI-Lo Block Diagram



FPGA Block Diagram



FPGA Requirements Summary

- FPGA requirements in 7464-4093
- FPGA contains all event processing and event logic
  - SCIP: 16-bit 10 MIPS processor (reused custom embedded processor based on Harris RTX2010 and APL's FRISC)
  - Processor memory interface to PROM, MRAM, SRAM
  - LVDS UART spacecraft communication interface
  - Support I/O
    - Provide power supply clocks, set thresholds, monitor housekeeping, read high voltage safing status, etc.
  - Test Interfaces
    - Processor test port, event logic test port
    - Internal pulser stimulus
  - Event Logic
    - Count sensor basic rates and diagnostic rates
    - Collect and process TDC values to generate start direction and particle TOF
    - Select appropriate SSD channel and record energy deposited (energy and extended energy as appropriate)
    - Detect coincidence, anti-coincidence, and pulse-height over-threshold
    - Send selected valid events to processor event buffer

FPGA Development Path

- Part choices
  - For Flight: Actel RTAX2000SL -1 speed CCGA-624 (common buy)
  - For EM: Reprogrammable A3PE3000 on Aldec adapter
  - Option to use AX2000 on an EM board but not planned
- Design Flow
  - Design files are maintained on SD Unix system
    - VHDL with constraint files and control scripts as needed
    - Reports, programming files, simulation outputs etc
  - Design is targeted to both flight and EM throughout development
  - Design files are backed up to local system with SourceTree for EM change tracking and Doxygen for internal documentation
  - Flight design files will be archived in PLM
  - The software specification serves as the formal documentation and user manual for the whole digital system
- Design Tools
  - Synplify Pro (I-2013.09, Build 545R, Aug 28 2013)
  - Actel Libero (9.1.0.18)
  - ModelSim

FPGA Development Path

- Current Status
  - All functions tested on EM event board
  - Functional simulations on individual components
  - Timing simulations on timing-critical components
  - Design synthesized and routed for flight
  - Static timing analysis complete

- Note: FPGA Design and Development Process controlled by QMS QY3-775-01. Many similar guidelines and requirements as NASA 500-PG-8700.2.7 and 500-PG-8700.2.8

Resource Requirements - Gates

- Actel RTAX2000SL -1 speed CCGA-624 (common buy part)
  - Design is fully implemented for both EM and flight part
  - Flight Usage:
    - SEQUENTIAL (R-cells) Used: 8452 Total: 10752 (78.61%)
    - COMB (C-cells) Used: 17469 Total: 21504 (81.24%)
    - LOGIC (R+C cells) Used: 25921 Total: 32256 (80.36%)
    - RAM/FIFO Used: 3 Total: 64
    - Note: Internal RAM for event FIFO only so soft memory is fine (does include a parity check however)
    - Note: APL guidelines consider moderate reuse designs “red” risk at 80% fill at EDR. This is understood and there are possibilities for reducing fill percentage if necessary.

Resource Requirements – I/O

- Actel RTAX2000SL -1 speed CCGA-624 (common buy part)
  - IO w/Clocks Used: 418 Total: 418
  - Outputs are low slew, 12 mA
  - No I/O left floating
  - APL guidelines consider uncommitted I/O “green”
    - 16 spares (driven low)
  - If even more spares were needed:
    - 2 spares from unneeded/unused 1 PPS inputs
    - 2 test port inputs through Schmitt triggers
    - 5 test port outputs through Schmitt triggers
  - Special pins
    - PRA/B/C/D: open
    - TDI, TDO, TDS: open
    - TCK, TRST: ground
    - VPUMP: 3.3V
    - Flight NC with options for commercial and socket parts (not planned for use but board accommodates possibility)

Resource Requirements - Power

- 1.5 V Core Voltage, 3.3 V I/O supply voltage
  - +/-5% voltage tolerance
  - Supplies can be powered up or powered down in any sequence as long as some app note details are considered
  - I/O are tri-stated during power-up
- SmartPower analysis (tends to be too high in my opinion)
  - Best Case: 417 mW
  - Worst Case: 966 mW
- Power Spreadsheet analysis
  - Best Case: 250mW (19mA at 3.0V + 130mA at 1.425V)
  - Best Case without static component: 149mW (2mA, 100mA)
    - Experience shows this is a reasonable typical case for low temperature instruments with low radiation requirements
  - Worst Case: 556mW (47mA at 3.6V + 261mA at 1.575V)
  - RBSPICE comparison (roughly 1/3 of resources and much less running on masterclk)
    - 105mW (6.5mA at 3.3V, 56mA at 1.5V)

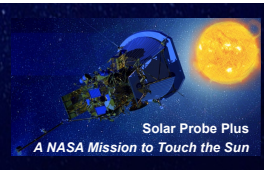
Timing Analysis

- Standard reset and clock handling
  - Appropriate handling of async signals, clock domain crossing etc.
  - HCLOCK for procclk, masterclk, baudclk
  - Routed CLOCK for heavily loaded reset, clr_evt, stretch
- Static timing analysis complete with sufficient margin per APL guidelines
  - Conditions (over-conservative):
    - Radiation Exposure: 100 Krad Temperature: MIL Voltage: MIL
    - Speed Grade: -1 Design State: Post-Layout Data source: Silicon verified
    - Min Operating Condition: BEST Max Operating Condition: WORST
  - Min timing results: No timing violations
  - Max timing results: No timing violations
    - Clock Domain: masterclk
    - Frequency (MHz): 105.009
    - Required Frequency (MHz): 40.000
    - Clock Domain: procclk
    - Frequency (MHz): 16.687
    - Required Frequency (MHz): 10.000

Remaining Work

- Remaining EM Work
  - Address any issues found in integrated testing / calibration
    - Preliminary wedge check and power board check okay
  - Systematically verify requirements on final design
    - Preliminary check has been completed on current design
- Remaining FM Preparation Work
  - Release requirements document
  - Release FPGA design files
  - Prepare FPGA programming request

FPGA Design Structure Overview



- EPI-Lo Top Level
  - Processor – Reused from JEDI/RBSPICE/EIS
  - Clock and reset handling – Reused from JEDI/RBSPICE/EIS
  - Core I/O – Similar to JEDI/RBSPICE/EIS and SO-SIS with some updates (moderate reuse)
  - Event – Similar to JEDI/RBSPICE/EIS and SO-SIS with some updated and unique components (some reuse)
    - Focus of design review

Processor and Memroy

- The SCIP processor is unchanged
- Processor Memory Interface
  - The FPGA shall read from one 32K x 8 PROM.
    - The PROM is used for boot code. When reading 16-bit instructions from PROM, each read requires 4 processor cycles. For simplicity, 8-bit reads also use 4 cycles. Interface details are in the UT28F256LVQLE datasheet.
  - The FPGA shall read from and write to one 2M x 8 MRAM.
    - The MRAM is used for software code, macros, and look-up tables. 16-bit MRAM access requires 4 processor cycles for a read or a write. MRAM interface details are in the UT8MR2M8-40YPC datasheet.
  - The FPGA shall read from and write to one 512K x 32 SRAM organized as 1024K x 16 bits.
    - The SRAM is used for software code, macros, telemetry, science data, and look up tables. SRAM access requires 1 processor cycle for a read or a write. SRAM interface details are in the HLXSR01632 datasheet.

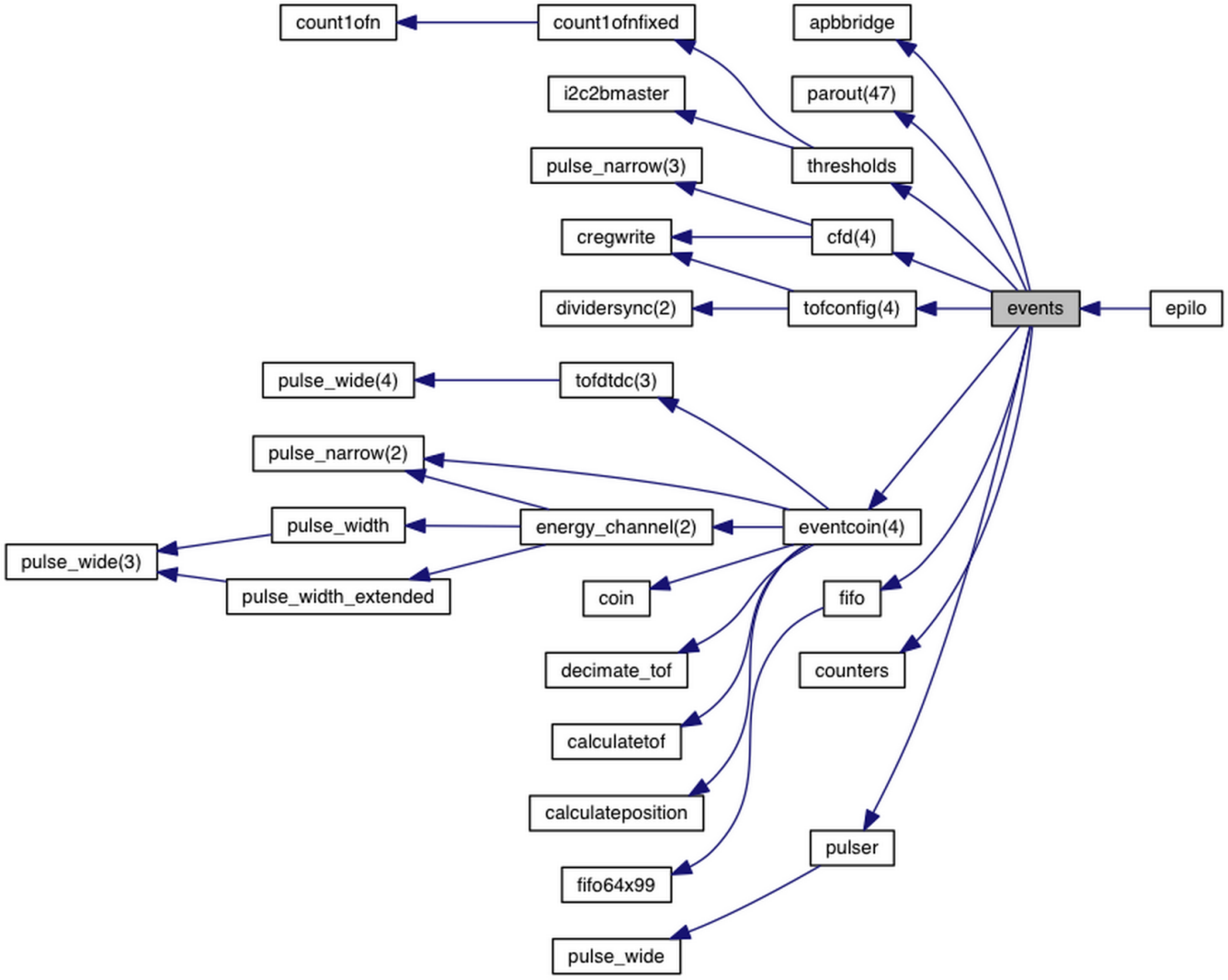
Other Core I/O

- S/C Communication UART
- Housekeeping ADCs (SPI)
- 400 kHz clock for LVPS
  - Runs even during reset
- Programmable HVPS clocks
  - Enabled and disabled by command
- Programmable bias clock
  - Enabled and disabled by command
- Read and report safing plug
- Read MCP over-current trip per quadrant
- Respond to trip with MCP shutdown (when monitoring is enabled)
- MCP shutdown when commanded

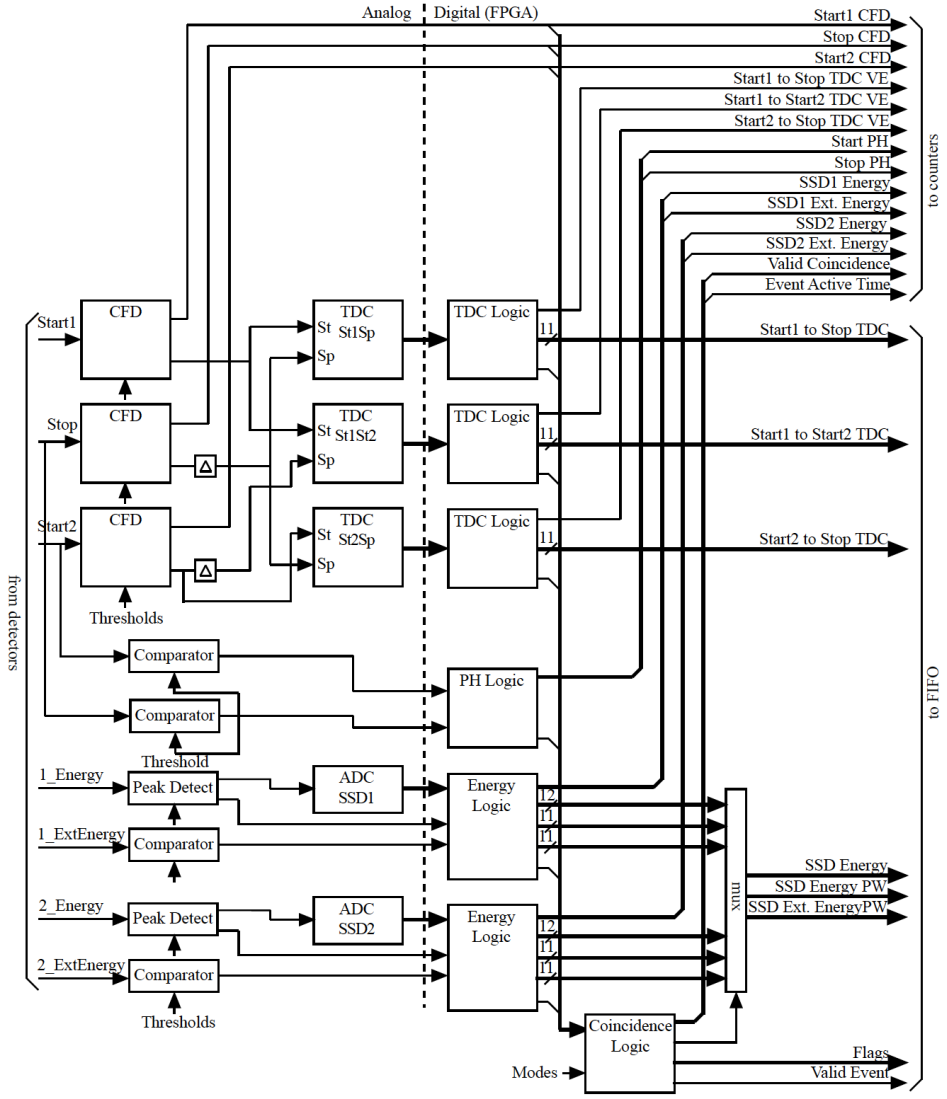
Event Structure – Illusion?

- The software maintains the illusion that there are independent particle and ion electronics
- The software maintains the illusion that there are separate event logic mode processing chains by time-multiplexing between modes
  - Ion Energy
  - Ion Composition
  - Particle Energy
  - Particle Composition
- The FPGA just has one event processing chain
  - Configured by software
  - Sends events to software
- For example, there are commands to set the particle energy threshold and to set the ion energy threshold. The software time-multiplexing loads the actual hardware threshold with either the particle and ion setting depending on the event mode.
- The four quadrants are almost entirely independent but must all be the same mode
  - A one-event-deep holding register per quadrant multiplexes events through one FIFO to the processor

Events Structure – VHDL view



Events Structure – Quadrant View



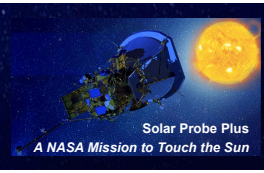
Events - Thresholds

- Event thresholds are on the “fast” I2C bus
  - Energy thresholds
  - Extended energy thresholds
- Other thresholds are on the “slow” I2C bus in core I/O
  - Pulse height thresholds
  - Pulser configurations
  - Power supply configurations

Events – CFD ASICs

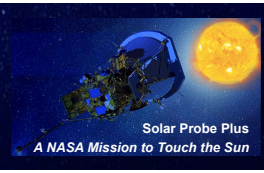
- 3 CFDs per quadrant: Start1, Start2, Stop
- Set each individual threshold (by command/parameter)
- Set each individual autozero (by command/parameter)
- Fixed pulsewidth
- SPI-like control bus for settings

Events – TOF-D ASICs



- One TOF-D per quadrant
- 3 channels of each TOF-D used
  - Start1 to Stop (with stop delay)
  - Start2 to Stop (with stop delay)
  - Start1 to Start2 (with start2 delay)
  - ~73ps LSB to ~150ns max measured TOF
- SPI-like control bus for settings
- Delays are set by parameter, all other settings are fixed
- TDC logic configuration is “digital window”
  - One start followed by one stop within 2047 codes is valid
  - Multiple starts are invalid
  - Multiple stops are invalid
  - Start with stop >2047 codes later is invalid
  - Start without stop is invalid

Events – Energy Measurements



- 2 energy channels per quadrant
- "Three part" energy measurements
  - Linear energy range
    - ~50 keV to ~1.5MeV
    - Measure analog output of peak detect ASICs with ADC
      - 8-Channel ADC but only using 1 channel per part
      - Baseline parameter is also subtracted from this ADC measurement
  - PW or composite energy range
    - ~1MeV to ~20MeV
    - Measure width of LED from peak detect ASIC
    - Roughly 1 us/MeV
    - 25ns steps to ~20us expected (51us max implemented)
  - Extended energy range
    - ~20MeV to ~400MeV with some caveats
    - Measure width of comparator output from extended energy chain
      - In ion modes, this is the low gain channel
    - 25ns steps to 51us max implemented with an inactive 200ns ignored

Events – Baseline Measurements

- Alternatively, all event activity and event logic criteria is ignored and the energy ADC collects energy baseline measurements
- Same FIFO path

Events – Event Modes

- Event mode and event coincidence determine how TDC and Energy measurements are considered

	Event Logic Mode – Are These Events Produced?			
Event Type	**Ion Composition**	**Particle Composition**	**Ion Energy**	**Particle Energy**
Energy-only	No	No	Yes	Yes
TOFxE	As available	As available	As available	As available
TDC-only	As allowed	As allowed	No	No

Events - Settings

	Event Logic Mode – Does the Setting Apply?			
Event Setting	**Ion Composition**	**Particle Composition**	**Ion Energy**	**Particle Energy**
Ignore some energy channels	Yes	Yes	Yes	Yes
Specify if start and energy or stop and energy coincidence is required	No (always required)	No (always required)	Yes	Yes
Specify if extended energy and energy coincidence is required	No (always ignored)	Yes	Yes	Yes
Accept/reject simultaneous energy events	Yes	Yes	Yes	Yes
Specify TDC Valid Criteria	Yes	Yes	No	No
Specify TDC-only acceptance %	Yes	Yes	No (none)	No (none)
Ignore some positions (set width 0)	Yes	Yes	No	No
Ignore/require valid position	Yes	Yes	No	No
Ignore/require position match SSD	Yes	Yes	No	No
Ignore/required TDC measurements match closely	Yes	Yes	No	No

Events - Coincidence

- Coincidence windows are hardcoded
  - One set for energy modes: Timing relative to energy LED
  - One set for composition modes: Timing relative to stop
  - 100ns step sizes
  - Activity required in 1 (and only 1) “1” location
  - Other activity ignored
- Required coincidence is configurable (to some degree – see previous slide)
- Coincidence is also reported for events that match the event logic criteria

Energy

Start1	1	1	1	1	1	1	
Start2	1	1	1	1	1	1	
StartPH	1	1	1	1	1	1	
Stop		1	1	1	1	1	1
StopPH		1	1	1	1	1	1
VE(s)			1	1	1	1	1
SSD	0	0	0	0	0	**1**	0
Anti					1	1	1

Composition

Start1	1	1	1	1			
Start2	1	1	1	1			
StartPH	1	1	1	1			
Stop	0	0	**1**	0	0	0	0
StopPH		1	1	1			
VE(s)	1	1	1	1	1		
SSD		1	1	1	1	1	1
Anti		1	1	1	1	1	1

Events – Calculate Position

- 20 positions per quadrant plus one pulser position per quadrant
  - Each position set with minimum Start1Start2 value
  - Each position set with width per position
  - These values are in TOF units (~73ps/lsb)
- In composition modes:
  - Setting a position width to 0 and requiring a valid position ignores specific positions for further event processing.
  - Option to require the calculated position to be valid for further event processing. That is, require the position be 0 through 19 or pulser position 20.
  - Option to require the calculated position to match the SSD for further event processing. That is, require the position to be 0 through 9 if SSD1 or 10 through 19 if SSD2. The pulser position 20 is considered to match both SSDs.

Events – Calculate TOF

- TOF is the average of Start1Stop and Start2Stop
- In composition modes:
  - Option to require TDC values to match closely for further event processing in composition modes. That is, require Start1Stop - Start2Stop + Delay ~= Start1Start2.
  - Parameters for expected delay and close enough values for each quadrant to evaluate whether the TDC values match closely. These values are in TOF units (~73ps/lsb).

Events – Allow TDC-only

- Option to allow TDC-only or reject TDC-only events for further event processing in composition modes
- Option to decimate TDC-only events for further event processing in composition modes.
  - That is, in addition to the option of enabling all TDC-only events or disabling all TDC-only events, there are options to send some TDC-only events: every 2nd, 4th, 8th, 16th, 32nd, or 64th.

Events - FIFO

- No favoritism between quadrants
- All quadrants merge to a single fifo
- Core generated 64x99 FIFO

	total bits	97
Event word from HW to SW	**Bits**	
TDC St1 to Sp		11
TDC St1 to St2		11
TDC St2 to Sp		11
TDC Valid Flags		3
MCP PH Coin Flags (start, stop)		2
Calculated TOF		11
Calculated Start Position (0-19, pulser 20, invalid 31)		5
SSD Energy		12
SSD Energy Pulsewidth (25ns units)		11
SSD Extended Energy (25ns units)		11
SSD / Anti Coincidence		1
SSD / Start1 Coincidence		1
SSD / Start2 Coincidence		1
SSD / Stop Coincidence		1
SSD / VE Coincidence (all required VEs)		1
SSD ID		2
Quadrant ID (A = 00, B=01, C=10, D=11)		2

Events - Counters

- 21 bits
- Sync.

Name	Description
A Start1 CFD	A CFD pulses
A Start2 CFD	
A Stop CFD	
A Start1 to Stop TDC Valid	A TDC valid events
A Start2 to Stop TDC Valid	
A Start1 to Start2 TDC Valid	
A Start PH	A PH pulses
A Stop PH	
A1 SSD Energy LED	A energy pulses
A1 Extended Energy	
A2 SSD Energy LED	
A2 Extended Energy	
A Valid Coincidence	A valid coincidence events
A Event Active Time	A event analysis activity time
B Start1 CFD	B pulses
...	
B Event Active Time	
C Start1 CFD	C pulses
...	
C Event Active Time	
D Start1 CFD	D pulses
...	
D Event Active Time	
FIFO Write	FIFO writes

Events - Pulser

- Pulses can be injected into front-end circuitry
- Start to each quadrant
- Stop to each quadrant
- Energy test “1” to all quadrants
- Energy test “2” to all quadrants
- Options for start to stop delay
  - These delays are from approximately 0ns to approximately 187.5ns in approximately 12.5ns steps but the exact values are unimportant and any used values will be characterized.
- Options for start to energy delay
  - These delays are from approximately 0ns to approximately 787.5ns in approximately 12.5ns steps but the exact values are unimportant and any used values will be characterized.
- Options for rate
  - These rates are ~300hz, 400hz, 500hz, ~600hz, ~700hz, 800hz, ~900hz, 1khz, 2khz, ~3khz, 4khz, 5khz, ~6khz, ~7khz, 10khz, and 25khz but the exact values are unimportant and any used values will be characterized.
- Option for external enable
  - Test port input 1

Summary

- FPGA is (possibly) complete
  - V3.3 design fits and meets timing
  - But not 100% tested. Need a fully integrated instrument!
- Remaining FPGA Work
  - Release requirements document
  - Help clarify system and software documents as needed
  - Address any issues found in testing / calibration
  - Release FPGA design files
  - Prepare FPGA programming request
  - Flight FPGA test