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EPI-Lo FPGA Requirements Document

FSCM NO.	SIZE	DRAWING NO.	REV.
88898	A	7464-4093	-
SCALE NONE	DO NOT SCALE PRINT	SHEET 1 OF 27	

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Introduction

1.1 Purpose

This document defines the requirements for the FPGA for the Energetic Particle Instrument - Low Energy (EPI-Lo), part of the Integrated Science Investigation of the Sun (ISIS) suite on the Solar Probe Plus spacecraft.

1.2 Instrument Context

ISIS is a two-instrument suite consisting of EPI-Hi and EPI-Lo. Together, their primary objective is to determine in both gradual (shock accelerated) and impulsive (flare accelerated) solar energetic particle (SEP) events: energy spectra, composition (electrons, protons, major heavy elements) timing, and pitch angle distributions. Another objective of the ISIS suite is to measure 3He as a key indicator of impulsive events. ISIS will also provide measurements of other populations (CIRs, ACRs, and GCRs) to provide important new information on the radial dependences of these particles.

EPI-Lo is a high-heritage TOF-based mass spectrometer that measures over 2π steradians the energetic electron (25-500 keV) and ion spectra (~0.02-7 MeV protons & 0.02-2 MeV/nuc heavier ions). EPI-Lo resolves all major heavy ion species and 3He and 4He over much of this energy range in multiple directions. EPI-Lo covers the critical energy range from suprathermal energies (~20 keV/nuc) up to the lower portion of EPI-Hi energy range with a single instrument.

EPI-Lo is comprised of two subsystems, the sensor and the main electronics. The sensor consists of eight identical wedges, each having 10 apertures and look directions. The electronics are separated into two boards, the event board and the power supply board. The sensor head and main electronics are mechanically integrated together and mounted as a single unit to the spacecraft via an ISIS-provided bracket. Each sensor wedge includes a time-of-flight (TOF) section feeding a solid-state silicon detector (SSD). The SSD and its associated preamps connected to the event board measures particle energy. Secondary electrons, generated by ions passing through the entry and exit foils, are detected by the timing anodes and their associated preamps to measure ion TOF. Event energy and TOF measurements are combined to derive ion mass and to identify particle species.

EPI-Lo has one FPGA with an embedded processor (there is no other processor in the instrument). This document describes the requirements for the FPGA.

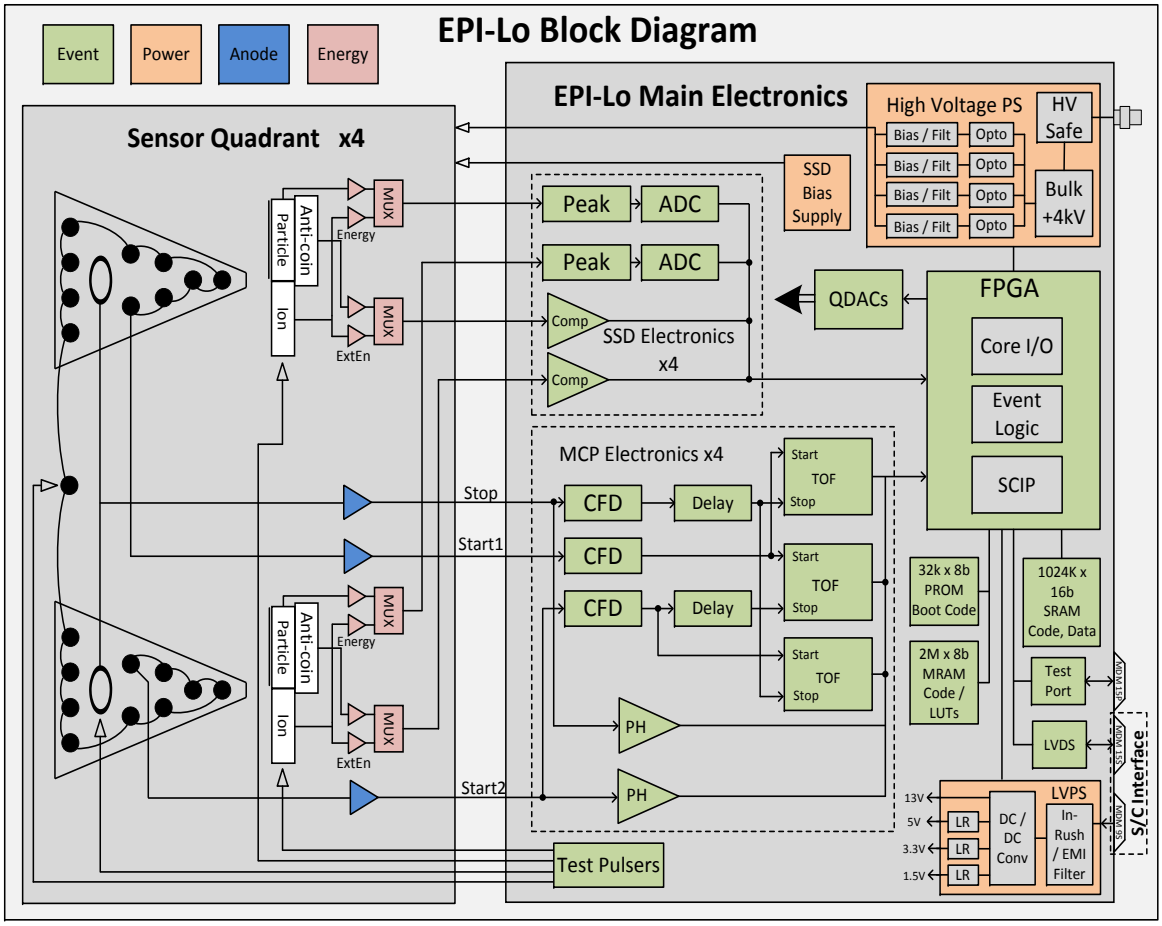

Figure 1: EPI-Lo Block Diagram

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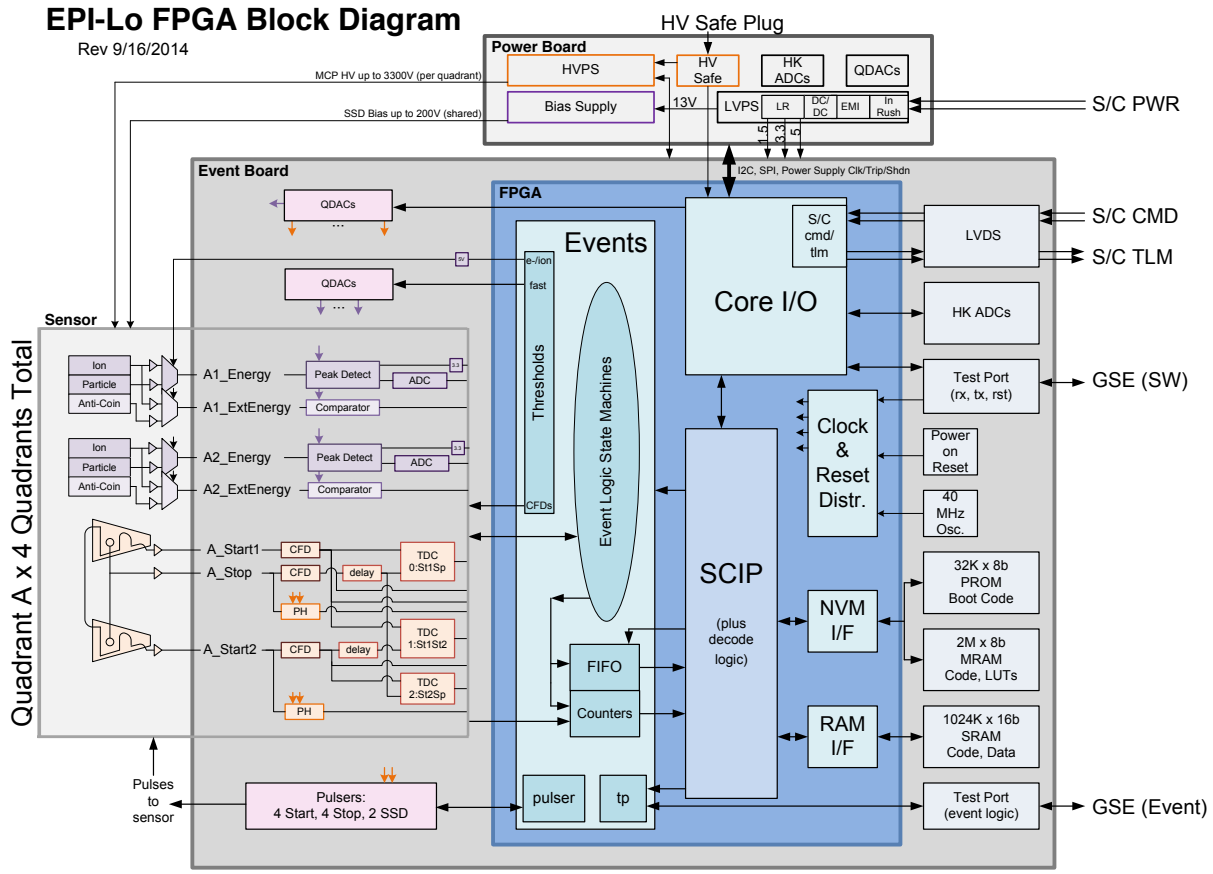

Figure 2: FPGA Block Diagram

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References

(1) 16105-ISIS-IRD-01, “INSTRUMENT REQUIREMENTS DOCUMENT SOLAR PROBE PLUS PROJECT ISIS INSTRUMENT”

(2) 7434-9066 SPP General Instrument ICD

(3) 7434-9058 SPP-ISIS ICD

(4) 7434-9039 SPP EDTRD

(5) 7434-9040 EMECP

(6) 7464-9004, EPI-Lo Software Requirements

(7) 7464-9005, EPI-Lo Flight Software Specification

(8) Hayes, J.R., “EPI-Lo FPGA Software Interface”, ???, 2014, SRI-14-???,

(9) Hayes, J.R., “The Architecture of the Scalable Configurable Instrument Processor (SCIP), August 8, 2005, SRI-05-030.

(10) SD-QP-775, “Spacecraft FPGA Electronics Design and Development Process”

Requirements

1.1 Clock Input

1.1.1 The FPGA shall create all internal clocks from a 40MHz input oscillator.

1.2 Reset Management

1.2.1 The FPGA shall be reset when both external power on reset signals are asserted.

1.2.2 The FPGA shall be reset when the external test port reset is asserted.

Note: There are a few clock cycles of filtering on this external test port reset, but it should also be filtered externally to the FPGA.

1.2.3 The FPGA shall be reset when the internal processor watchdog reset is asserted.

Note that some basic functions persist through an internal processor watchdog reset.

1.3 Processor

1.3.1 The FPGA shall contain a 16-bit Scalable Configurable Instrument Processor (SCIP).

The interface between the FPGA and the flight software is described in Reference (8) and the processor is described in Reference (9).

1.4 Processor Memory Interface

1.4.1 The FPGA shall read from one 32K x 8 PROM.

The PROM is used for boot code. When reading 16-bit instructions from PROM, each read requires 4 processor cycles. For simplicity, 8-bit reads also use 4 cycles. Interface details are in the UT28F256LVQLE datasheet.

1.4.2 The FPGA shall read from and write to one 2M x 8 MRAM.

The MRAM is used for software code, macros, and look-up tables. 16-bit MRAM access requires 4 processor cycles for a read or a write. MRAM interface details are in the UT8MR2M8-40YPC datasheet.

1.4.3 The FPGA shall read from and write to one 512K x 32 SRAM organized as 1024K x 16 bits.

The SRAM is used for software code, macros, telemetry, science data, and look up tables. SRAM access requires 1 processor cycle for a read or a write. SRAM interface details are in the HLXSR01632 datasheet.

1.5 Low Voltage Power Supply

1.5.1 The FPGA shall provide the low voltage supply with a 400 kHz clock (+/- 500ppm). (Requirement source: 7434-9040 EMECP)

1.5.2 The FPGA shall generate the low voltage clock with a ~50% duty cycle.

1.5.3 The FPGA shall continue to run the low voltage clock even during a FPGA reset.

1.6 MCP HV Power Supply

1.6.1 The FPGA shall provide the high voltage supply with a programmable clock and its inverse. The HV clock frequency is 5MHz/(N+1) where N is an 8 bit integer.

1.6.2 The FPGA shall generate the high voltage clocks with a ~50% duty cycle.

1.6.3 The FPGA shall be able to enable and disable the high voltage clock signals.

1.6.4 The FPGA shall drive both high voltage clocks high when they are disabled.

1.7 SSD Bias Power Supply

1.7.1 The FPGA shall provide bias voltage supply with a programmable clock. The bias clock frequency is 5MHz/(N+1) where N is an 8 bit integer.

1.7.2 The FPGA shall generate the bias voltage clock with a ~50% duty cycle.

1.7.3 The FPGA shall be able to enable and disable the bias voltage clock signal.

1.7.4 The FPGA shall drive the bias voltage clock low when it is disabled.

1.8 High Voltage Safing Plug

1.8.1 The FPGA shall read the status of the high voltage safing plug. This status is passed to the software; safing is a software function.

1.9 High Voltage Over-Current Monitor

1.9.1 The FPGA shall read the status of the MCP over-current trip in each quadrant.

1.9.2 The FPGA shall assert MCP shutdown for that quadrant if an over-current trip is detected in that quadrant and monitoring is enabled.

1.9.3 The FPGA shall assert MCP shutdown per quadrant when commanded from software.

1.9.4 The FPGA shall assert MCP shutdown for all quadrants if the MCP supply is disabled.

1.10 Serial Buses

1.10.1 The FPGA shall provide an I2C bus master to set thresholds.

There are I2C Quad DACs on the event board for setting energy thresholds and extended energy thresholds that use the "fast" I2C bus.

1.10.2 The FPGA shall provide a general-purpose I2C bus master.

There are I2C Quad DACs on the event board for setting pulse height thresholds and pulser configurations that use the "slow" I2C bus. There are I2C Quad DACs on the power board for setting power supply configurations that use the "slow" I2C bus.

1.10.3 The FPGA shall provide an SPI bus master.

The event board has 2 SPI ADCs and power board has 3 SPI ADCs used for monitoring housekeeping telemetry. The other SPI ADCs used for event logic are handled separately.

1.11 Constant Fraction Discriminators (CFDs)

1.11.1 The FPGA shall set individual CFD thresholds for the start1, start2, and stop CFDs for each quadrant. (Set by command/parameter.)

1.11.2 The FPGA shall set individual CFD autozeros for the start1, start2, and stop CFDs for each quadrant. (Set by command/parameter.)

1.11.3 The FPGA shall set a fixed CFD pulsewidth for the start1, start2, and stop CFDs (i.e., set to ~20ns nominal and not set by command).

1.12 Time Of Flight (TOF) Measurement

1.12.1 The FPGA shall detect TOF events from start1-to-stop, start2-to-stop, and start1-to-start2 for each quadrant.

1.12.2 The FPGA shall not use the fourth channel of each TOF chip.

1.12.3 The FPGA shall process TOF measurements independently for the four quadrants.

1.12.4 The FPGA shall set the Start2 delay per quadrant via TOF chip configuration. (Set by command/parameter.)

1.12.5 The FPGA shall set the Stop delay per quadrant via TOF chip configuration. (Set by command/parameter.)

1.12.6 The FPGA shall set a fixed polarity (active-low) and multi-hit mode (off) via TOF chip configuration. (Fixed. Not set by command/parameter.)

1.12.7 The FPGA shall accommodate the longest required TOF measurement. See Appendix B. Longest TOF Accommodation Notes

1.13 SSD Energy Measurement

Also see Appendix C. Types of Energy Measurements and Uses

Also see Appendix D. Energy Timing Notes

1.13.1 The FPGA shall select either ion with extended energy ion measurements or particle with anticoincidence measurements. This selection is made at the instrument level and cannot be mixed by quadrant. This selection can be time multiplexed at the slot level.

1.13.2 The FPGA shall detect SSD energy events for two SSDs per quadrant.

1.13.3 The FPGA shall process SSD energy measurements independently for the four quadrants.

1.13.4 The FPGA shall set individual thresholds for the energy pulses. (Set by command/parameter.)

1.13.5 The FPGA shall set individual baseline energy values for energy measurements. (Set by command/parameter.)

1.13.6 The FPGA shall report processed SSD energy measurements as the measured ADC value minus the baseline energy value. Values that would be negative are reported as zero.

1.13.7 The FPGA shall report processed SSD energy pulsewidths as the LED duration in 25ns step sizes (up to ~51us). (See Appendix E. Higher Energy Measurement Notes)

1.13.8 The FPGA shall report processed SSD energy extended energy as the extended energy duration in 25ns step sizes (up to ~51us) with inactive periods up to ~200ns included in the duration. (See Appendix E. Higher Energy Measurement Notes)

1.14 Coincident Event Detection

1.14.1 The FPGA shall detect particle events consisting of coincident TOF and SSD energy pulse events.

With the ion SSD selected, this is called Ion Composition Mode. With the particle SSD selected, this is called Particle Composition Mode

1.14.2 The FPGA shall have a fixed TOF to energy coincidence window for composition modes.

This includes start1 to energy LED, start2 to energy LED, stop to energy LED, and TDC valid event to energy LED. TODO: Draw windows.

1.14.3 The FPGA shall read the event's 3 TDC values, energy, and extended energy when coincident.

1.14.4 The FPGA shall handle coincident events from each quadrant independently but the coincidence modes are consistent across quadrants.

1.14.5 The FPGA shall have a non-coincident mode with energy event required but TDC event optional.

With the ion SSD selected, this is called Ion Energy Mode. With the particle SSD selected, this is called Particle Energy Mode.

1.14.6 The FPGA shall have a fixed TOF to energy coincidence window for energy modes.

This includes start1 to energy LED, start2 to energy LED, stop to energy LED, and TDC valid event to energy LED. TODO: Draw windows.

1.15 Event Logic Mode Summary

Note: Not a requirement. See requirements in subsequent sections.

Table 1: Event Types per Event Mode

	Event Logic Mode – Are These Events Produced?			
Event Type	**Ion Composition**	**Particle Composition**	**Ion Energy**	**Particle Energy**
Energy-only	No	No	Yes	Yes
TOFxE	As available	As available	As available	As available
TDC-only	As allowed	As allowed	No	No

1.16 Event Logic Settings Summary

Note: Not a requirement. See requirements in subsequent sections.

Table 2: Event Settings per Event Mode

	Event Logic Mode – Does the Setting Apply?			
Event Setting	**Ion Composition**	**Particle Composition**	**Ion Energy**	**Particle Energy**
Ignore some energy channels	Yes	Yes	Yes	Yes
Specify if start and energy or stop and energy coincidence is required	No (always required)	No (always required)	Yes	Yes
Specify if extended energy and energy coincidence is required	No (always ignored)	Yes	Yes	Yes
Accept/reject simultaneous energy events	Yes	Yes	Yes	Yes
Specify TDC Valid Criteria	Yes	Yes	No	No
Specify TDC-only acceptance %	Yes	Yes	No (none)	No (none)
Ignore some positions (set width 0)	Yes	Yes	No	No
Ignore/require valid position	Yes	Yes	No	No
Ignore/require position match SSD	Yes	Yes	No	No
Ignore/required TDC measurements match closely	Yes	Yes	No	No

1.17 Event Logic Settings – All Composition and Energy Modes

1.17.1 The FPGA shall have an option to ignore specific energy channels for event processing.

1.17.2 The FPGA shall set 20 positions per quadrant plus one pulser position per quadrant via a minimum Start1Start2 value and width per position. These values are in TOF units (~73ps/lsb).

1.17.3 See 1.18.5: In composition mode, setting a position width to 0 and requiring a valid position ignores specific positions for further event processing.

1.18 Event Logic Settings - Ion Composition and Particle Composition Mode

1.18.1 The FPGA shall report but ignore extended energy coincidence for ion composition mode. That is, ion composition events are valid for further event processing regardless of the extended energy coincidence. This reporting also indicates the presence of an extended energy width measurement.

TODO: Draw windows.

1.18.2 The FPGA shall have an option to require, ignore, or prohibit extended energy coincidence for particle composition mode. That is, particle composition events are valid for further event processing based on the extended energy coincidence as specified. This is alternately called anticoincidence and this reporting also indicates the presence of the extended energy width measurement.

TODO: Draw windows.

1.18.3 The FPGA shall have an option to require a specific set of individual TDC-measurements in a quadrant to be valid for further event processing in composition modes.

1.18.4 The FPGA shall have an option to accept or reject two nearly simultaneous coincident energy events within one quadrant. If accepted, one is randomly selected for further processing (after determining coincidence timing but before calculating the position and thus position matching.)

1.18.5 The FPGA shall have an option to set any position width equal to zero in order to reject specific positions for further event processing in composition modes.

1.18.6 The FPGA shall have an option to require the calculated position to be valid for further event processing in composition modes. That is, require the position be 0 through 19 or pulser position 20.

1.18.7 The FPGA shall have an option to require the calculated position to match the SSD for further event processing in composition modes. That is, require the position to be 0 through 9 if SSD1 or 10 through 19 if SSD2. The pulser position 20 is considered to match both SSDs.

1.18.8 The FPGA shall have an option to require TDC values to match closely for further event processing in composition modes. That is, require Start1Stop - Start2Stop + Delay ~= Start1Start2.

1.18.9 The FPGA shall set the expected delay and close enough values for each quadrant to evaluate whether the TDC values match closely. These values are in TOF units (~73ps/lsb).

1.18.10 The FPGA shall have an option to allow TDC-only events for further event processing in composition modes. That is, a TDC event is required for composition modes but a coincident energy event is optional.

1.18.11 The FPGA shall have an option to decimate TDC-only events for further event processing in composition modes. That is, in addition to the option of enabling all TDC-only events or disabling all TDC-only events, there are options to send some TDC-only events: every 2^{nd}, 4^{th}, 8^{th}, 16^{th}, 32^{nd}, or 64^{th}.

1.18.12 The FPGA shall mark the SSD ID "none" for TDC-only events and set the energy-based measurements to 0 (SSD coincidence, energy, pulsewidth, extended energy duration).

1.19 Event Logic Settings – Ion Energy and Particle Energy Modes

1.19.1 The FPGA shall have an option to require, ignore, or prohibit Start1 and Energy coincidence in ion energy mode and particle energy mode.

TODO: Draw windows.

1.19.2 The FPGA shall have an option to require, ignore, or prohibit Stop and Energy coincidence in ion energy mode and particle energy mode.

TODO: Draw windows.

1.19.3 The FPGA shall have an option to require, ignore, or prohibit extended energy coincidence for ion energy mode and particle energy mode. This is alternately called anticoincidence for particle energy mode only.

TODO: Draw windows.

1.19.4 The FPGA shall have an option to accept or reject two nearly simultaneous coincident energy events within one quadrant. If accepted, one is randomly selected for further processing (after determining coincidence timing.)

1.19.5 The FPGA shall report the calculated position when available for coincident energy events in energy modes.

1.19.6 The FPGA shall mark the position "invalid" for energy-only events and set the other TDC-based measurements to 0 (TDC values, calculated TOF).

1.19.7 The FPGA shall not apply composition mode event logic criteria in energy modes.

1.20 Event Logic Settings – Baseline Measurements

1.20.1 The FPGA shall have an option to collect baseline energy measurements instead of processing events.

1.20.2 The FPGA shall have an option to specify the baseline energy measurement collection channel.

1.20.3 The FPGA shall ignore any event activity while collecting baseline measurements.

1.20.4 The FPGA shall report the energy and channel while collecting baseline measurements.

1.20.5 The FPGA shall mark the position "invalid" for baseline measurements, set the other TDC-based measurements to 0 (TDC values, calculated TOF, flags), and set the other energy-based measurements to 0 (pulsewidth, extended energy, flags).

1.21 Event FIFO

1.21.1 The FPGA shall deliver event data to the software via a single FIFO.

1.21.2 The FPGA shall merge events from the four quadrants into the FIFO without showing favoritism between the quadrants.

1.22 Counters

1.22.1 The FPGA shall count each CFD, start pulse height, stop pulse height, energy LED, and extended energy pulse. Note however that even short pulses must be separated by >150ns to ever be counted and >250ns to always be counted. Note also that "each" includes each per quadrant.

1.22.2 The FPGA shall count valid events from each TDC state machine. That is, count valid events both per the TOF-chip and the TDC-level state machine. Note also that "each" includes each per quadrant.

1.22.3 The FPGA shall count valid events per quadrant. That is, count valid events per the quadrant-level event state machine. This includes all valid events per that event logic setting - for example, all TOFxE valid events and TDC-only valid events in ion composition mode when TDC-only events are enabled.

1.22.4 The FPGA shall count event state machine active time per quadrant. That is, the duration (in 100ns units) that the quadrant-level event state machine is not idle.

1.22.5 The FPGA shall count successful FIFO writes. There is only one FIFO so this is not per quadrant.

1.22.6 The FPGA hardware counters shall be large enough to accommodate the duration of one slot. This is because they are accumulated for one slot in hardware before being added to 32-bit software counters: ceiling(log2(1/8 second / 100ns) = 21 bit counters.

1.23 Rate Requirements

1.23.1 The FPGA shall be able to handle a total electron count rate of ≥ 70,000 counts per second. These events can be either evenly distributed over the entire instrument or concentrated in one wedge. (Requirement source: (1))

1.23.2 The FPGA shall be able to handle a total ion count rate (SSD and MCP valid coincident event) of ≥ 70,000 counts per second. These events can be either evenly distributed over the entire instrument or concentrated in one wedge. (Requirement source: (1))

1.24 Internal Pulser

1.24.1 The FPGA shall provide coordinated start, stop, and energy test signals.

1.24.2 The FPGA shall have a separate enable for the start test signal for each quadrant.

1.24.3 The FPGA shall have a separate enable for the stop test signal for each quadrant.

1.24.4 The FPGA shall have a separate enable for the energy test signal 1 (to all quadrants.)

1.24.5 The FPGA shall have a separate enable for the energy test signal 2 (to all quadrants.)

1.24.6 The FPGA shall have a variety of delay options from start to stop.

These delays are from approximately 0ns to approximately 187.5ns in approximately 12.5ns steps but the exact values are unimportant and any used values will be characterized.

1.24.7 The FPGA shall have a variety of delay options from start to energy test signal 1.

These delays are from approximately 0ns to approximately 787.5ns in approximately 12.5ns steps but the exact values are unimportant and any used values will be characterized.

1.24.8 The FPGA shall have a variety of delay options from start to energy test signal 2.

These delays are from approximately 0ns to approximately 787.5ns in approximately 12.5ns steps but the exact values are unimportant and any used values will be characterized.

1.24.9 The FPGA shall have a variety of rate options for the set of test signals.

These rates are ~300hz, 400hz, 500hz, ~600hz, ~700hz, 800hz, ~900hz, 1khz, 2khz, ~3khz, 4khz, 5khz, ~6khz, ~7khz, 10khz, and 25khz but the exact values are unimportant and any used values will be characterized.

1.24.10 The FPGA shall have an option to require test port input 1 to be asserted in order to enable the internal pulser.

1.25 Spacecraft Communication

1.25.1 The FPGA shall provide a UART interface operating at 115200 baud, with 8 data bits and odd parity [Source: 7434-9066 INST_012].

1.25.2 The FPGA shall be able to communicate over either A or B sides. [Source: 7434-9066]

1.25.3 The FPGA shall sample the received command messages such that any pulse of 50 nansoeconds or less in duration is rejected [Source: 7434-9066 INST_010].

1.25.4 The FPGA shall properly decode command messages for which the transmitter bit length is (1/115,200) seconds +/- 1.5% [Source: 7434-9066 INST_015].

1.25.5 The FPGA shall transmit at (1/115,200) seconds +/- 1.5% [Source: 7434-9066 INST_021].

1.25.6 The FPGA shall generate a synchronized virtual 1 PPS. [Source: 7434-9066 INST_016 and INST_017].

1.25.7 The FPGA shall use the virtual 1 PPS to generate an interrupt for every 1/8th second "slot".

1.26 Test Port

1.26.1 The FPGA shall have a processor test port serial interface operating at 19200 baud, with 8 data bits and no parity.

1.26.2 Also see 1.2.2 The FPGA shall be reset when the external test port reset is asserted.

1.26.3 The FPGA shall be able to enable and disable an auxiliary power output.

1.26.4 The FPGA shall include 2 general-purpose test port inputs and five test port outputs. The use of these signals is at the convenience of the FPGA engineer(s).

1.26.5 Also see 1.24.10 The FPGA shall have an option to require test port input 1 to be asserted in order to enable the internal pulser.

Appendix A. Acronyms

ADC	Analog to Digital Converter
CFD	Constant Fraction Discriminator (an APL ASIC)
CMD	Command
DC	Direct Current (usually as DC/DC converter)
dE/dx	Something Particle Physicists Want To Measure
EPI-Lo	Energetic Particle Instrument - Low Energy (this instrument)
E	Energy (as used in this document)
EMI	Electromagnetic Interference
ExtE	Extendend Energy (as used in this document)
FPGA	Field Programmable Gate Array
FSW	Flight SoftWare
GSE	Ground Support Equipment
HK	House Keeping (periodic current, voltage, etc. measurements)
HV	High Voltage
HVPS	High Voltage Power Supply
I/O	Input/Output
I/F	Interface
ICD	Interface Control Document
ISIS	Integrated Science Investigation of the Sun (this suite)
JHU/APL	Johns Hopkins University Applied Physics Laboratory
LED	Leading Edge Discriminator
LR	Linear Regulator
LUT	Look Up Table
LVDS	Low Voltage Differential Signal
LVPS	Low Voltage Power Supply
MCP	Micro Channel Plate
MRAM	Magnetoresistive RAM
NVM	Non-Volatile Memory
PH	Pulse Height
PKD	Peak Detector (an APL ASIC)
PW	Pulse Width
QDAC	Quad DAC (4 channel Digital to Analog Converter, an APL ASIC)
RAM	Random Access Memory
Rst	Reset
Rx	Receive (usually referencing serial command stream)
S/C	Spacecraft
SCIP	Scalable Configurable Instrument Processor
SPP	Solar Probe Plus (this spacecraft)

SSD..... Solid State Detector
SW..... SoftWare
TDC..... Time to Digital Conversion
TDC-only ..... Time to Digital Conversion measurements only (no energy)
TLM ..... Telemetry
TOF ..... Time Of Flight (general or the specific APL ASIC)
TOFxE..... Time Of Flight by Energy (coincident measurements)
Tx ..... Transmit (usually referencing serial telemetry stream)

Appendix B. Longest TOF Accommodation Notes

- Worst case path length = 9.60 cm
  - Measured in model from start foil in -17 collimator (bottom outside aperture of wedge) to opposite corner of stop foil
- Slowest particle = Iron
  - According to TRIM, Fe just barely gets into the active volume through (10 nm C + 20 nm Al + 35 nm Polyimid) stop foil + 50 nm Si (SSD dead layer) at 70 keV. About 20 % of the ions make it through at 100 keV. About 90% at 250keV. The 500keV requirement is for incoming particle energy and these numbers are for the post start-foil energy (need relationship).
- Longest TOF = Worst case path length + slowest particle + required delay
- To measure start1 to start2, need a TOF delay at least as long as anode delay length
  - Start anode length about 20ns.
  - To first order, delay = Tap/96 * [delay clock period / 2] with quasi-log options
  - Options with a 2.5MHz clock:
    - Tap 12 (command 0xB) is nominally 25ns
    - Tap 16 (command 0xA) is nominally 33.3ns
    - The measured value can be a few ns from the nominal value but only has about 50ps of jitter. Various over temperature are on the order of +/-1ns
- To measure start2 to stop, we also need a stop delay at least as long as anode delay length (the start2 delay does not apply)
  - This needs to be added to the measurement window. For example:
    - 250kV Fe: 103ns + 25ns => 128ns or 103ns + 33ns => 136ns
- TOF chips with a nominal gain around 100ps/dn have a variation in gain about 0.4% over temperature and 0.3% over supply voltage. They have a variation in offset about 1% over temperature and 0.4% over temperature. This is in addition to the few LSB offset and the gain characteristics they begin with.
- Nominal TOF chip full scale is the period of the cal clock. Options:

40 MHz oscillator divisor	Cal Clock In (MHz)	Nominal LSB (ps)	Nominal Max (ns)	Minimum Fe Energy (keV, after start foil, with 35ns for delays added)
4	10.00	49	100	
5	8.00	61	125	330
6	**6.67**	**73**	**150**	**205 Selected**
7	5.71	85	175	140
8	5.00	98	200	100

Appendix C. Types of Energy Measurements and Uses

Event Logic Mode	**SSD selected** for energy via peak detect	**Extended energy selected** for energy via comparator	Products from **composite energy** (E + PW)	Products from **extended composite energy** (E + PW + ExtE)	Products from **extended energy** (ExtE)	Products from **TDC-only**
Ion Composition	Ion	High energy ion	->	Ion composition	<-	TOF histogram
Ion Energy	Ion	High energy ion	->	Ion energy spectra	<-	No product
Particle Composition	Particle	Anti-coincidence	Moderate energy ion composition	no	no	TOF histogram
Particle Energy	Particle	Anti-coincidence	Electron energy spectra, High angular resolution electron energy spectra, (and ->->)	no (but ->)	dE/dX particles: Composite energy by extended energy matrix	No product

"Energy" is the ADC measurement of the captured peak detect. Also sometimes called "SSD energy"

- Ion energy (from ion SSD
- Particle energy (from flashed SSD formerly known as "electron energy")

"PW" is the "pulsewidth" - time over threshold measurement made with the peak detect and FPGA

- Ion PW
- Particle PW

"Composite energy" is the Energy + PW for Energy DN >= {a value}

- Ion composite energy
- Particle composite energy

"Extended energy" - time over threshold measurement made with the comparator and FPGA

- Ion extended energy (from ion SSD with low gain and thus called ion extended energy)
- Anti-coincidence extended energy (from anti-coincidence SSD)

"Extended composite energy" is the Energy + PW for Energy DN >= {a value} + ExtEnergy for PW >= {another value}

- Ion extended composite energy

"Composition" is TOFxE (E can be E+PW or E+PW+Ext)
"Spectra" is E-only (E can be E+PW or E+PW+Ext)
"Histogram" is TDC-only
"Matrix" is E+PWxExtE

Appendix D. Energy Timing Notes

Relevant requirements from 16105-ISIS-IRD-01, "INSTRUMENT REQUIREMENTS DOCUMENT SOLAR PROBE PLUS PROJECT ISIS INSTRUMENT"

- ISIS-100 The EPI-Lo instrument shall provide measurements of energetic electrons with an energy range of <=0.05MeV to >=0.5MeV.
- ISIS-106 The EPI-Lo instrument energy measurement range for ions (incoming energies) shall be <= 0.05MeV/nucleon to >= 5 MeV/nucleon to a maximum energy of 15 MeV.
- ISIS-111 The EPI-Lo instrument shall measure ion composition for the 0, 22.5, and 45 degree apertures with the following mass resolution:
    - H: 1.5 FWHM AMU for incoming energies between ≤0.05 MeV and ≥4.0 MeV
    - 3He, 4He: 0.5 FWHM AMU for incoming energies between ≤0.2 MeV and ≥2.0MeV
    - C, O: 2 FWHM AMU for incoming energies between ≤0.2 MeV and ≥5.0 MeV
    - Ne, Mg, Si: 2 FWHM AMU for incoming energies between ≤0.5 MeV and ≥1.5 MeV
    - Fe: 13.5 FWHM AMU for incoming energies between ≤0.5 MeV and ≥15 MeV

Event logic considerations

- Time to LED and Time to Anti depends on threshold setting
- 100ns clock period -> 100ns resolution
- Clock synchronization adds uncertainty: be careful!
- CFD, LED, and Anti are delayed 0.5 to 1.5 clock periods due to clock synchronization
- TOF valid event is delayed 1 to 2 clock periods due to clock synchronization

Energy chip timing

- Notes on time to peak from small samples: 5 MeV -> 1.1us, 25 MeV -> 2.1us
- Time to LED ~0.25us at 50keV (faster for larger energies)
- Time to Peak ~0.47us at 1MeV (faster for smaller energies)

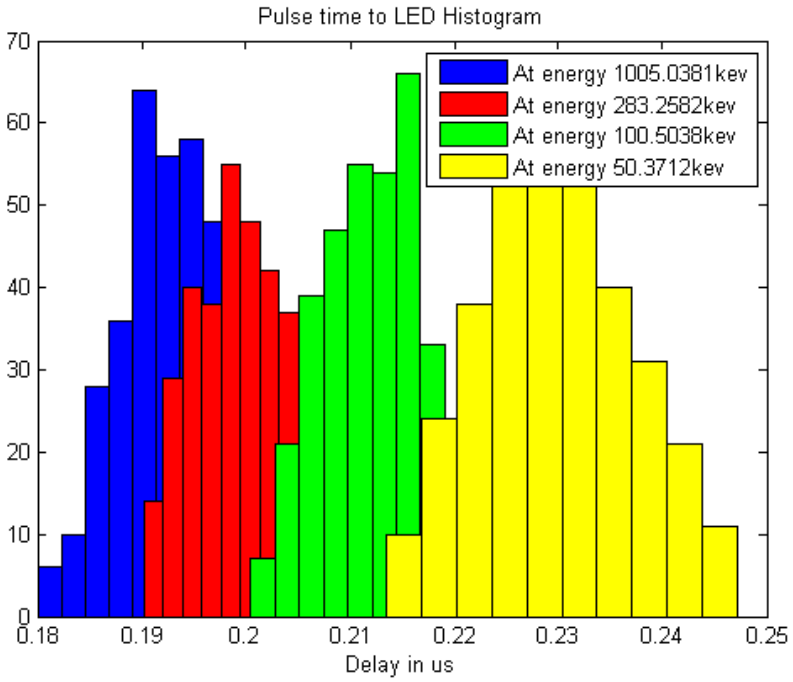

Figure 3 Pulse time to LED for RBSPICE flight parts as example

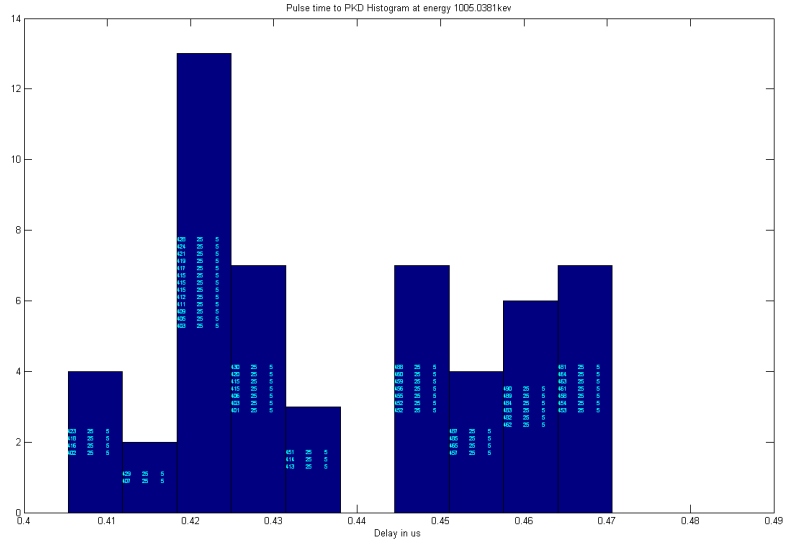

Figure 4 Pulse to Peak at 1 MeV = 0.47us max

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Appendix E. Higher Energy Measurement Notes

Pulse Width Energy: 1 - 20 MeV

The pulse width (PW) energy range (section 1.13.7) is approximately 1-20 MeV and the relationship between time-over-threshold (a measure of the pulse width) and energy is roughly 1us/MeV. The max of ~51us comes from requiring the timing range to have a factor of ~2 or greater margin over the expected saturation energy (~20 MeV). For the heritage Pucks (RBSPICE, JEDI, and MMS) a 100ns step size has been used, but we have elected to use 25ns resolution for EPI-Lo. This finer resolution corresponds to a minimum energy step of 25 keV. This is needed because for some data products (the binned TOF vs E software rates, for instance) we want energy bins with ~10 % energy spacing. At 1 MeV this means a bin would be 100 keV wide and we need to keep the innate resolution finer than this so we can have some flexibility and margin when we define the energy ranges of these bins. We decided a factor of four resolution increase (reducing 100 ns to 25 ns) was sufficient for these purposes.

Extended Energy: ~ 20 - 400 MeV (with caveats below)

The extended energy range (section 1.13.8) results from the low-gain branch of the SSD signal from the ion detector. This is not something that was done with the heritage Pucks. It was designed to allow measurement, in particular, of Iron in the ~20-100 MeV energy range so that there is energy coverage between EPI-Lo and EPI-Hi. Essentially the low gain signal can be analyzed just as the standard PW method (1.13.7) but the interpretation of the energy values change.

The extended energy range is approximately 20-400 MeV and the relationship between time-over-threshold (a measure of the pulse width) and energy is roughly 1us/20 MeV. For simplicity we've selected the same timing maximum (51 us) as the PW energy range (so the 400 MeV max derives from this choice, which is well over the minimum ~100 MeV Fe upper limit). The same 25 ns step size used for the regular PW measurements corresponds to ~0.5 MeV minimum energy step, or about 2.5 % at 20 MeV, also permitting an energy resolution of 10 % or better, with margin and flexibility.

Note that the extended energy range method does not return linear results between ~20 and ~50 MeV, so we are also using an absorber (Al flashing) over the particle detector to reduce the energy of the incident 20-50 MeV Fe to within the PW energy range (<20 MeV).