Solar Probe Plus

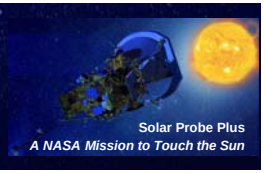
A NASA Mission to Touch the Sun

Integrated Science Investigation of the Sun
Energetic Particles

EPI-Lo Peer Review Event Board

Reid Gurnee

Suggested Outline



- Introduction & block diagram
- Driving requirements
- Design changes since PDR and rationale
- Detailed design description <this is the biggest section, of course>
- Resource requirements
- Design and analysis margins (performance, timing, derating, etc.)
- Peer review results
- EM testing and analysis
- Remaining EM work
- Status of special parts (e.g. ASICs)
- Plans for verification of design
- Development milestones and procurement status
- Known changes from EM to FM
- Drawing Status
- Summary

SPP Project Guidance for CDR (1/2)

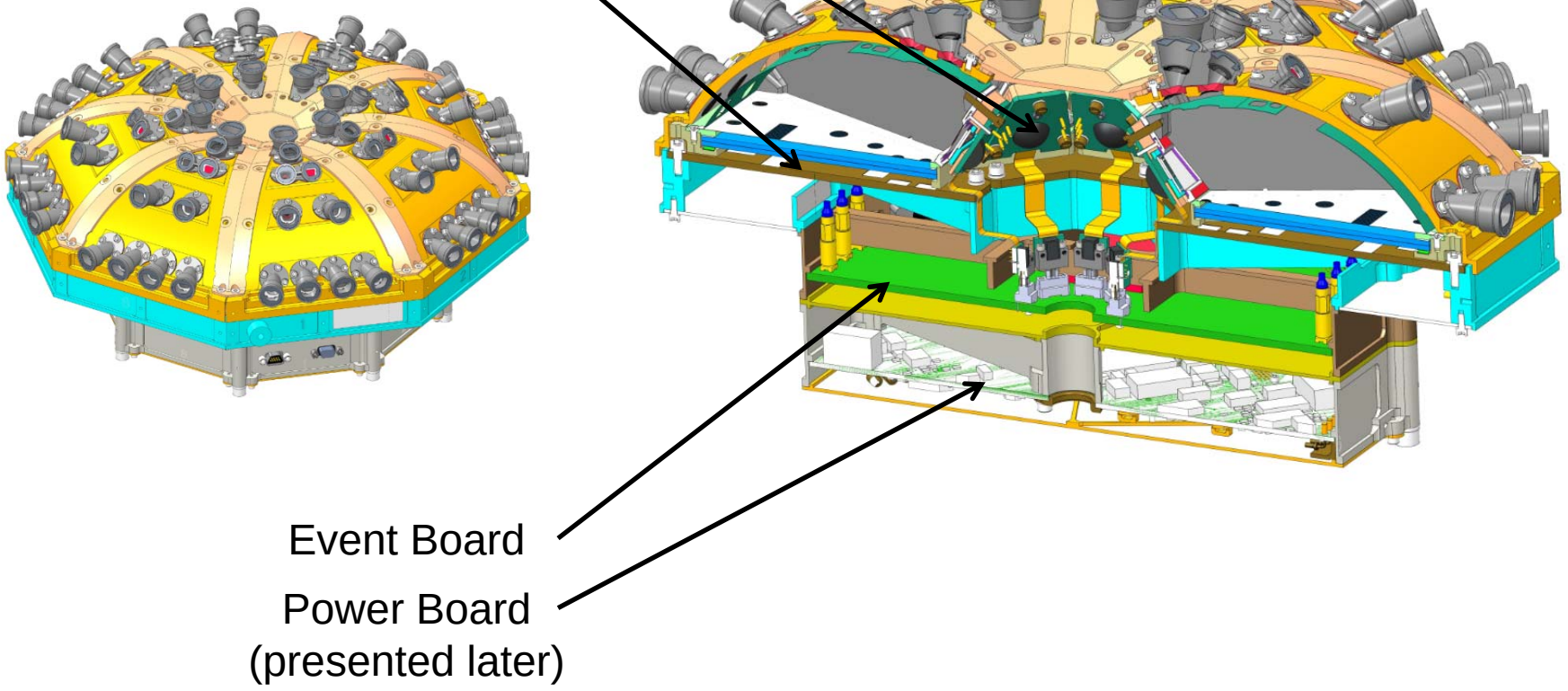
- List major subsystem performance requirements
  - Include their parent requirement
  - May be best presented in a table as a compliance matrix
  - Describe any changes in requirements or implementation since I-PDR
- Block diagram(s)
- Subsystem design description and top level specifications
  - Electrical and thermal subsystem design
  - Software architecture and design (if applicable)
  - Mechanical design and analyses
  - Design and performance margins
  - Discuss any changes since I-PDR
- Major mechanical and electrical interface requirements with other subsystems/components and how these are captured (mechanical ICD, electrical ICD, other?)
- Resource requirements
  - Table of mass and power for the components
  - Commanding and housekeeping telemetry requirements
  - Power services required
  - Other
- Breadboard/Engineering Model Testing
  - Status of testing
  - Approach to subsystem testing
  - Summarize tests
  - Results
- Describe ground handling
- Results of special parts testing, as applicable
- Results of packaging studies, show shielding plans

SPP Project Guidance for CDR (2/2)

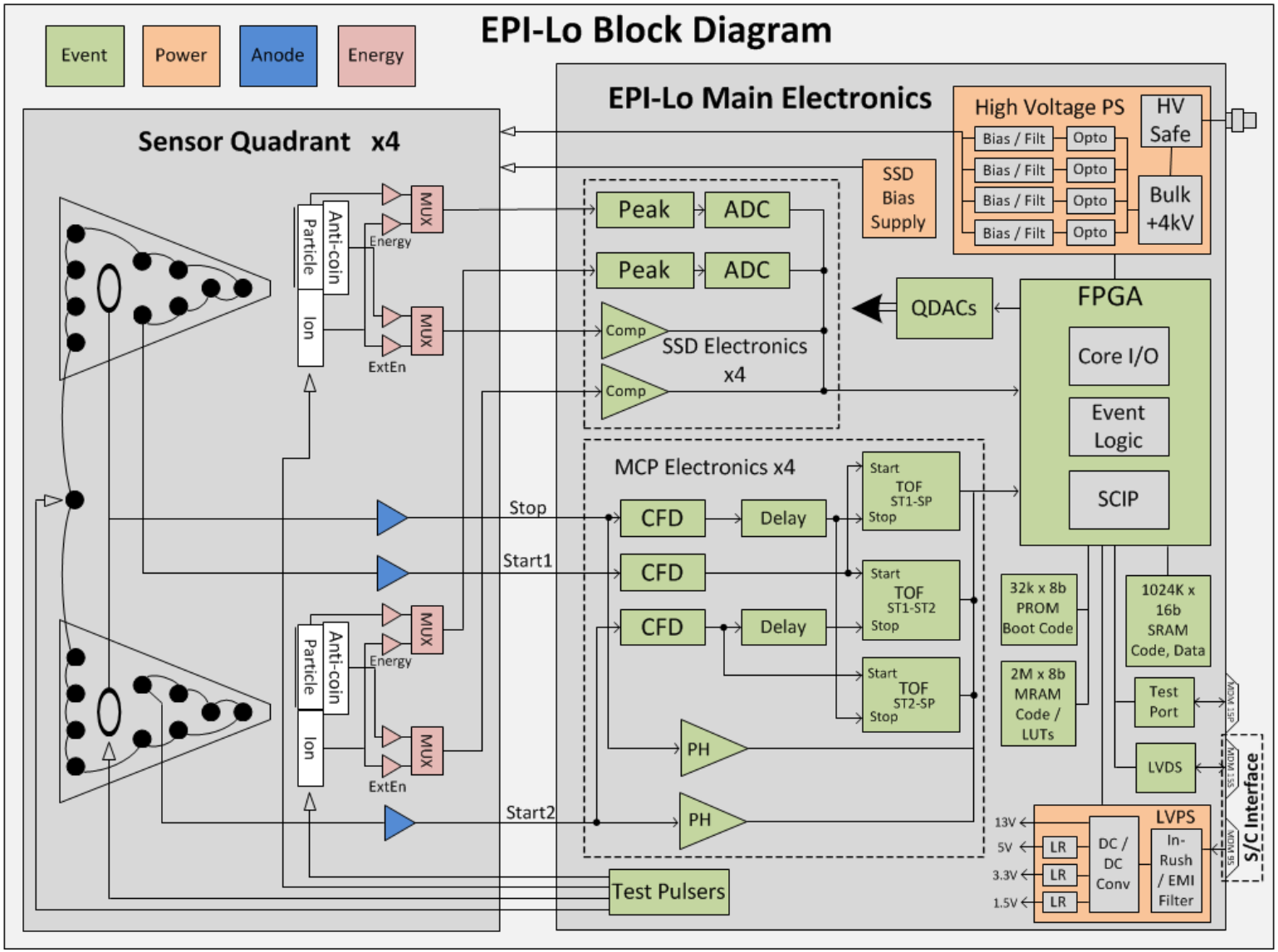
- Subsystem Verification
  - Plans for subsystem performance verification
  - Changes to plans for system verification since I-PDR
  - Status of any interface verification
- Subsystem Peer Reviews
  - Summary description of any subsystem peer reviews
  - Status of the action items (tabular format ok with list of actions items in backup)
- Discuss schedule for development/procurement
- Describe any changes planned from the EM to the FM
- Subsystem risks with mitigation plan and trigger dates per risk
- Describe any open work relative to design work yet incomplete
  - Include discussion of major component procurements
  - Include any major subcontracted fabrication activities
- Describe any special fabrication or test facility needs
- Drawing release status
- Parts/Materials PMPCB approval status
  - Include derating results
- Waivers sought against requirements

- Supporting the presentation (available hard copy in the room and electronically)
  - As-designed parts list with any parts requiring special screening identified
  - As-designed materials & processes list
  - Drawings (schematics, board artwork, assembly drawings)

EPI-Lo – Electronics Overview



Block Diagram



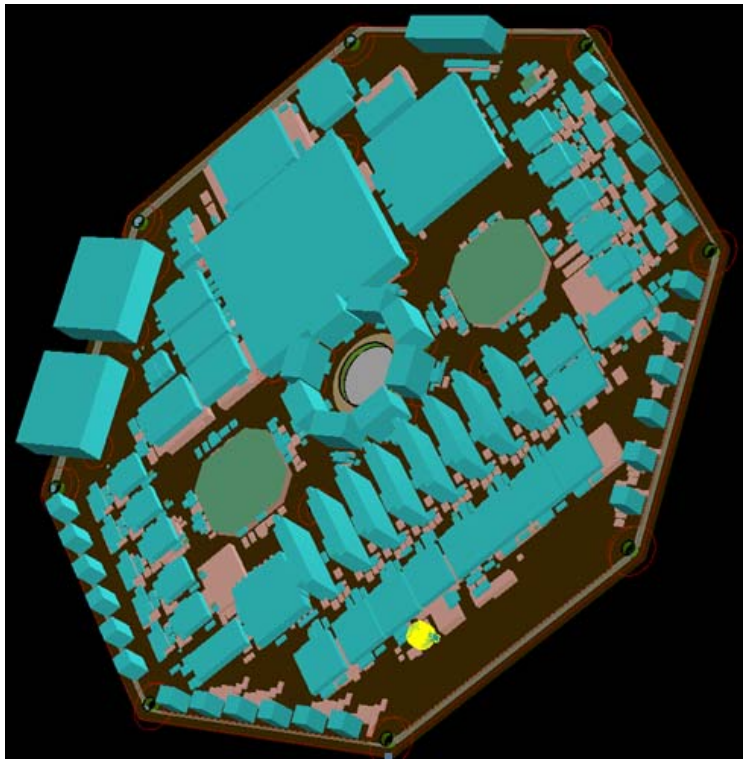
Event Board Driving Requirements

- Analog Performance
  - Timing resolution < 400 ps FWHM
  - Energy resolution < 15 KeV FWHM
- CFD dynamic range 35db
- Energy system dynamic range of 50 keV to 200+ MeV
  - Energies from 50 keV to 1.5 MeV use linear mode (ADC)
  - Energies from 1.5 MeV to 20 MeV use pulse width mode
  - Energies from 20 MeV to 50 MeV use absorber on particle detector
  - Energies >50MeV use extended energy range mode
- Temperature
  - Flight Survival: -45°C to +??°C
  - Flight Operational: -35°C to +25°C (35C with margin?)
  - Flight Board Level Testing (operational): -45C to +65C
- Radiation
  - TID: 25 kRad (based on FASTRad analysis)
  - SEL: 80 MeV-cm^2/mg

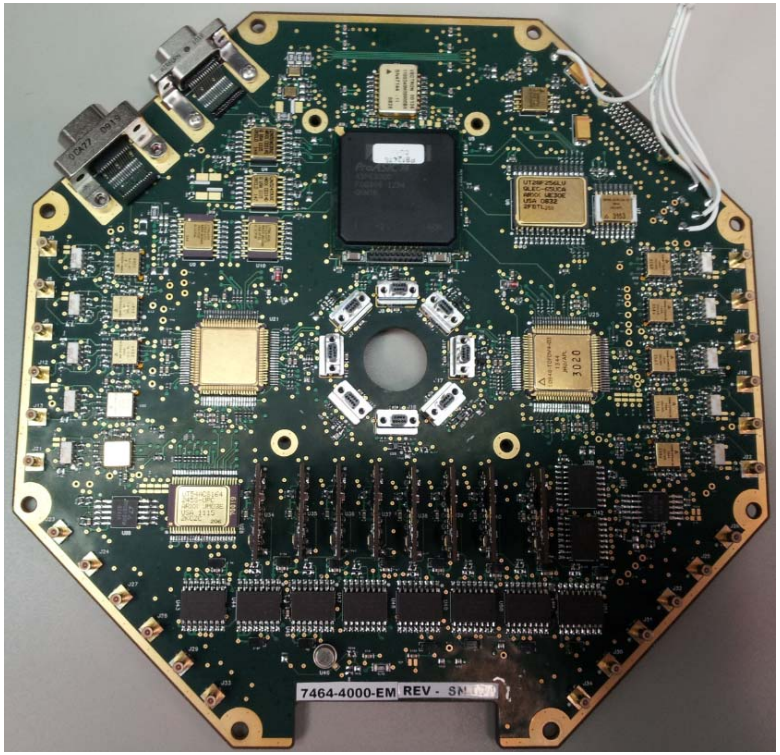
Design Changes Since PDR

- No board artwork changes
- Defined tailor values for all voltage reference control loop components
- At PDR, board parts placement and schematic were complete. That board has now been fabricated and tested.

PDR parts placement of EM board



EM board



Event Board Functionality (1/3)

- Instrument Processor
  - Embedded processor in RTAX2000
    - Execute flight code, accumulating and formatting telemetry, commanding, and alarm detection and action
  - Spacecraft Communication
  - Boot code in PROM, classification tables and application code in MRAM
  - Accumulate data into classification tables
- Event Processing
  - Communicate and handle timing with ADCs, TOF-Ds
  - Pre-process and accumulate event data
  - Accumulate rates

Event Board Functionality (2/3)

- Time-of-flight based on APL TOF-D and CFD-D ASICs
  - New ASICs developed for future programs
  - Improved size and performance from previous ASICs
  - 12 CFD-Ds and 4 TOF-Ds for timing system
- Solid-State Detector Energy Measurements
  - 8 Peak detect ASICs and A/D converters for energy system
  - Peak detect chips are APL ASICs flown on previous missions (PEPSSI, Jedi, RBSPICE)
- MCP pulse height comparators
- Pulsers
  - Independent pulsers for start and stop signals on each anode board
  - 2 pulsers for Energy system

Event Board Functionality (3/3)

- Power supply interface
  - Control four opto-coupler generated HVPS outputs and bulk supply
  - Provide high speed safing of HVPS in response to over current
  - Read housekeeping telemetry
  - Provide 400khz HVPS sync clock
  - Provide programmable bulk clock
  - Provide 50khz bias supply clock

Event Board Interfaces

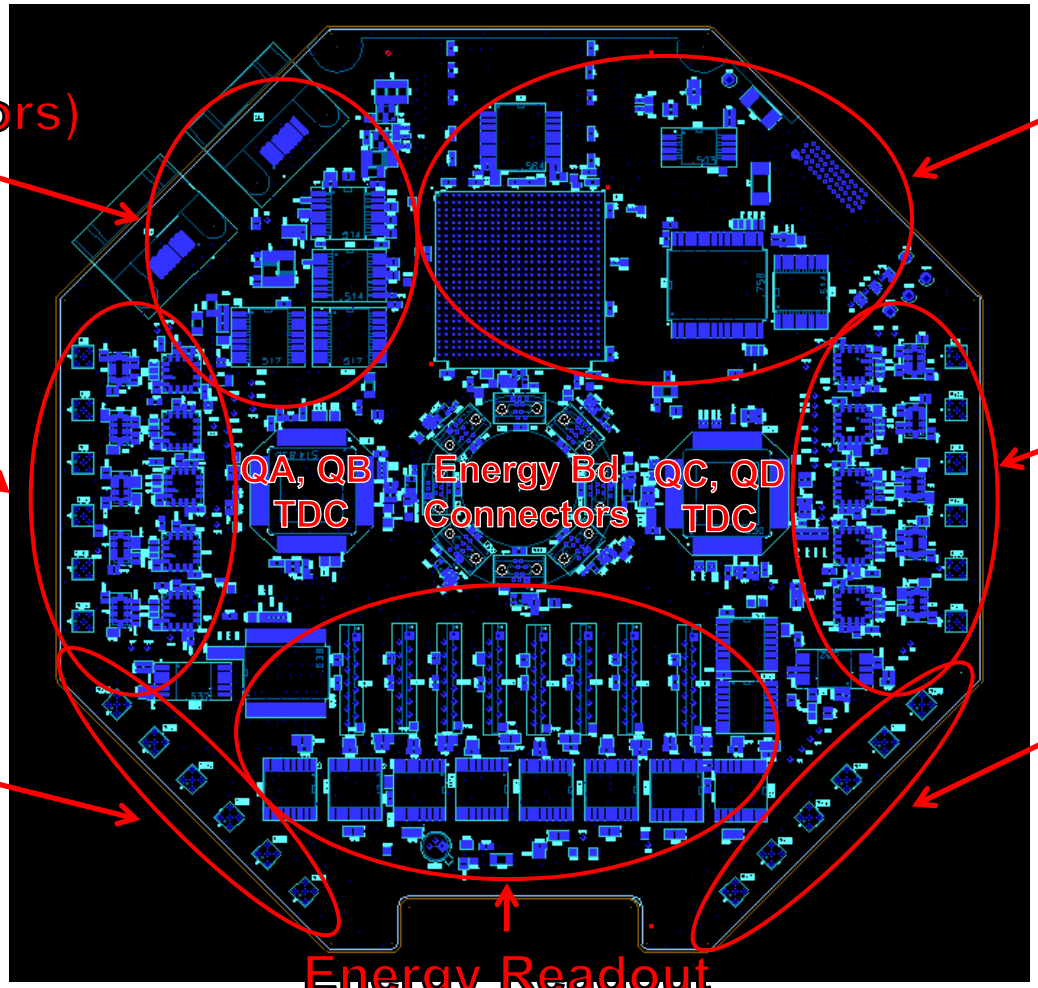
- Solid-State Detector Interface
  - 8 ndsub 9P connectors to energy boards
  - ~10 mV to 1 V unipolar-shaped pulses, control, pulser, and power
- Anode Board Interface
  - 12 Time-of-Flight Coax connectors
    - ~10 mV to over 1 V fast-shaped pulses
  - 4 power and 8 pulser Coax connectors
- Test Port Interface
  - MDM 15S connector
  - 2 test inputs (to aid in end-to-end timing tests)
  - 5 test outputs
- Spacecraft Data Interface
  - MDM 15P connector
  - Redundant LVDS interface (2 drivers, 2 receivers)
- Power Board Connector
  - 1 ndsub 51P connector for power and communication

Layout

- Sensitive analog is separated from digital
  - FPGA, S/C communication, SRAM, PROM, MRAM, and oscillator on top of board
  - TOF electronics on left and right of board
  - Peak detect and ADC electronics on bottom of board
  - All critical routing isolated by ground planes from digital routing
- 14 layers, 2 ground planes, 2 power planes (split), 10 routing layers
- Actel located with SRAM directly adjacent
  - Reduce track-length to SRAM to reduce noise
  - Actel on Primary side, to allow the Development Tool access to the program pins

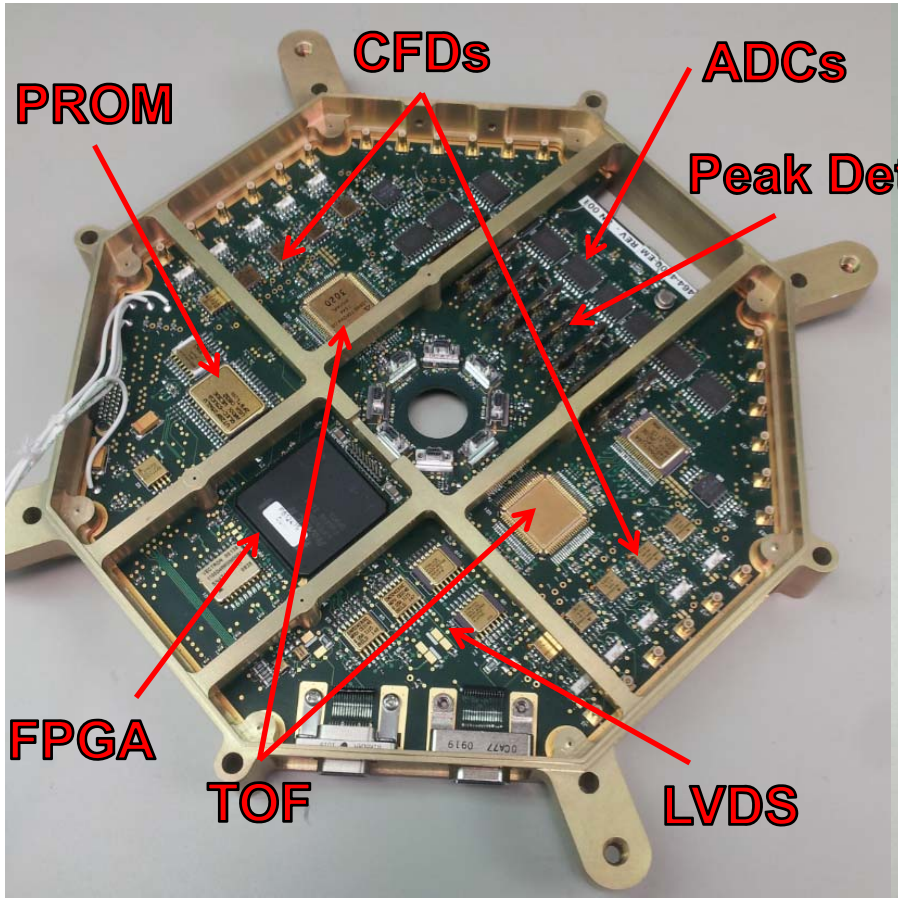
3 LAYER DETAIL CHART	
LAYER NAME	FINISHED CU WT (OZ.)
L1 - PRIMARY SIDE	1/2 MIN
L2 - GND	1/2 NOM
L3 - SIGNAL	1/2 NOM
L4 - SIGANL	1/2 NOM
L5 - +3.3V POWER	1/2 NOM
L6 - SIGNAL	1/2 NOM
L7 - SIGNAL	1/2 NOM
L8 - SIGNAL	1/2 NOM
L9 - SIGNAL	1/2 NOM
L10 - +1.5V / +5V POWER	1/2 NOM
L11 - SIGNAL	1/2 NOM
L12 - SIGNAL	1/2 NOM
L13 - GND	1/2 NOM
L14 - SECONDARY SIDE	1/2 MIN

Event Board Data Flow and Interfaces

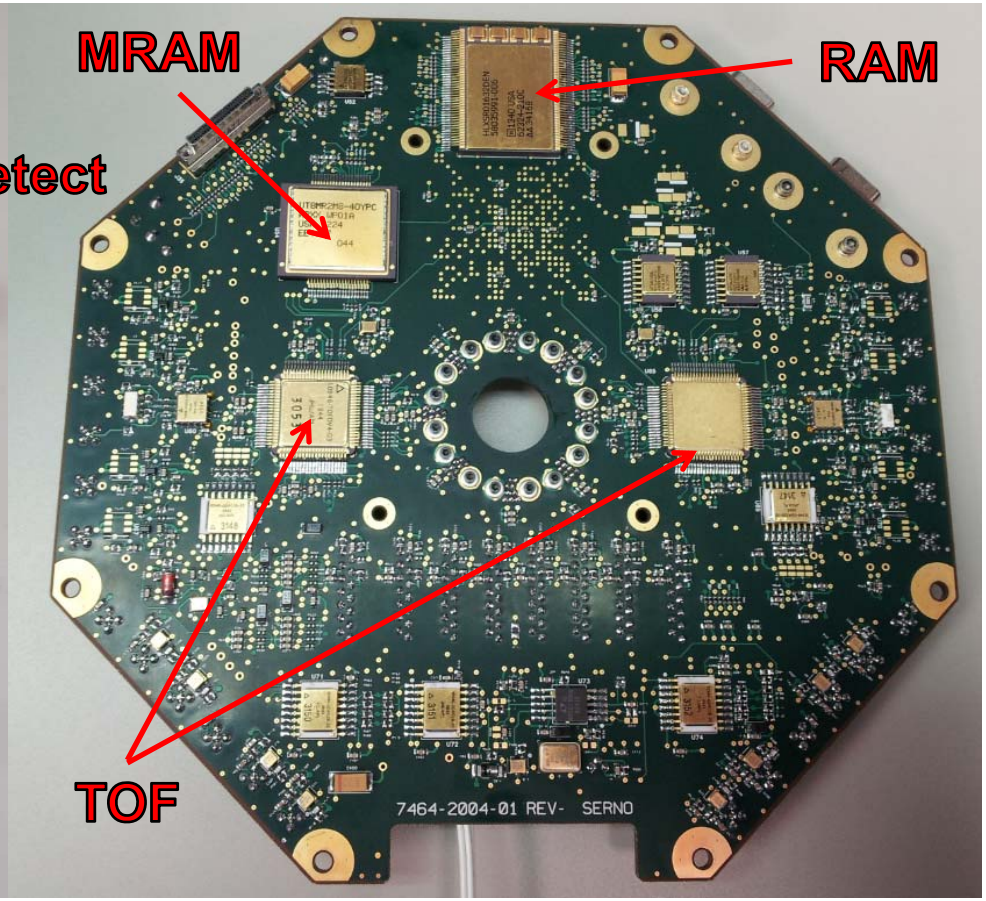


EM Event Board Components

EM Event Board in Frame



EM Event Board Secondary Side



Resources

- Mass
  - 221g (measured) + 20g (coating) + 8g (Flight FPGA) = 250g
- Power (measured and FM predict)
  - EM Measurement (standby)
    - 1.5V 60mA (90mW)
    - 3.3V 178 mA (587mW)
    - 5V 39mA (195mW)
    - 15V 0mA (0mW)
    - **Total: 872mW**
  - Flight Predict (operational)
    - 1.5V 80mA (120mW)
    - 3.3V 169mA (557mW)
    - 5V 46mA (230mW)
    - 15V 3mA (45mW)
    - **Total: 983mW**
  - EM measurements are on par with flight predict power
    - Differences in FPGA, test port connected, event rates, pulsers active

De-rating analysis

- De-rating analysis
  - All components meet de-rating analysis

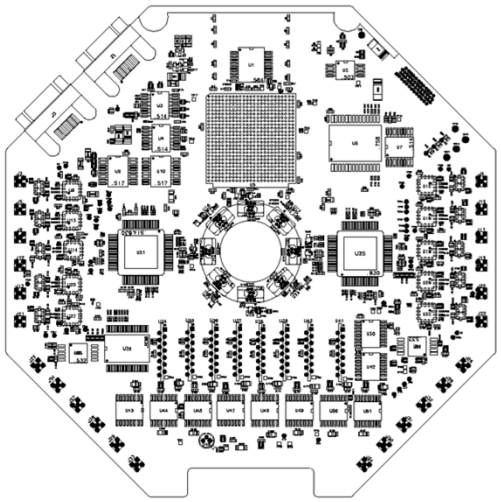
SEP-Assigned 'Order As' P/N	GPN	Circuit Designator	Capacitor Class	Voltage (V) If				Surge		Temperature (°C)			Notes	Web Address
				Rated	Derated	Actual	Stress	Actual	Duration (On-	Max. Operat	Max. Allowa	Actual		
311P829BDX104K6N	0603	C1	Ceramic	25	15	1.58	10.53%			125	110			
311P829BDX104K6N	0603	C2	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDX104K6N	0603	C3	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDX104K6N	0603	C4	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDX104K6N	0603	C5	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDX104K6N	0603	C6	Ceramic	25	15	1.58	10.53%			125	110			
311P829BDX104K6N	0603	C7	Ceramic	25	15		0.00%			125	110			
311P829BDX104K6N	0603	C8	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDX102K3N	0603	C9	Ceramic	100	60	1.58	2.63%			125	110			
CWR09HC226KCB	CWR09	C10	Tantalum, Solid	15	7.5	3.47	46.27%			125	110		3, 4	
311P829BDX102K3N	0603	C11	Ceramic	100	60	3.47	5.78%			125	110			
311P829BDX104K6N	0603	C12	Ceramic	25	15	5.25	35.00%			125	110			
311P829BDX104K6N	0603	C13	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDX104K6N	0603	C14	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDX104K6N	0603	C15	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDX104K6N	0603	C16	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDX104K6N	0603	C17	Ceramic	25	15	1.58	10.53%			125	110			
311P829BDX104K6N	0603	C18	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDX104K6N	0603	C19	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDX104K6N	0603	C20	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDX104K6N	0603	C21	Ceramic	25	15	1.58	10.53%			125	110			
311P829BDX104K6N	0603	C22	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDX104K6N	0603	C23	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDX104K6N	0603	C24	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDX104K6N	0603	C25	Ceramic	25	15	3.47	23.13%			125	110			
CWR09HC226KCB	CWR09	C26	Tantalum, Solid	15	7.5	5.25	70.00%			125	110		3, 4	
DNI_Cap	DNI	C27	Ceramic	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A		
311P829BDX104K6N	0603	C28	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDN220K3N	0603	C29	Ceramic	100	60	3.47	5.78%			125	110			
311P829BDX104K6N	0603	C30	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDX104K6N	0603	C31	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDX104K6N	0603	C32	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDX104K6N	0603	C33	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDX104K6N	0603	C34	Ceramic	25	15	2.6	17.33%			125	110			
311P829BAX102K3N	0504	C35	Ceramic	100	60		0.00%			125	110			
311P829BAX102K3N	0504	C36	Ceramic	100	60		0.00%			125	110			
311P829BAX102K3N	0504	C37	Ceramic	100	60		0.00%			125	110			
311P829BDX223K2N	0603	C38	Ceramic	50	30		0.00%			125	110			
311P829BDX103K2N	0603	C39	Ceramic	50	30		0.00%			125	110			
311P829BDX104K6N	0603	C40	Ceramic	25	15		0.00%			125	110			
311P829BDX104K6N	0603	C41	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDX104K6N	0603	C42	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDX104K6N	0603	C43	Ceramic	25	15	1.58	10.53%			125	110			
311P829BDX104K6N	0603	C44	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDX104K6N	0603	C45	Ceramic	25	15	1.58	10.53%			125	110			
311P829BDX104K6N	0603	C46	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDX104K6N	0603	C47	Ceramic	25	15	1.58	10.53%			125	110			
311P829BDX104K6N	0603	C48	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDX273K1N	0603	C49	Ceramic	25	15	15	####			125	110			
311P829BDX104K6N	0603	C50	Ceramic	25	15	3.47	23.13%			125	110			
311P829BDX103K2N	0603	C51	Ceramic	50	30		0.00%			125	110			
311P829BDX104K6N	0603	C52	Ceramic	25	15		0.00%			125	110			
311P829BDX104K6N	0603	C53	Ceramic	25	15		0.00%			125	110			
311P829BDX223K2N	0603	C54	Ceramic	50	30		0.00%			125	110			
311P829BAX102K3N	0504	C55	Ceramic	100	60		0.00%			125	110			
311P829BAX102K3N	0504	C56	Ceramic	100	60		0.00%			125	110			
311P829BAX102K3N	0504	C57	Ceramic	100	60		0.00%			125	110			
311P829BAX102K3N	0504	C58	Ceramic	100	60		0.00%			125	110			
311P829BAX102K3N	0504	C59	Ceramic	100	60		0.00%			125	110			

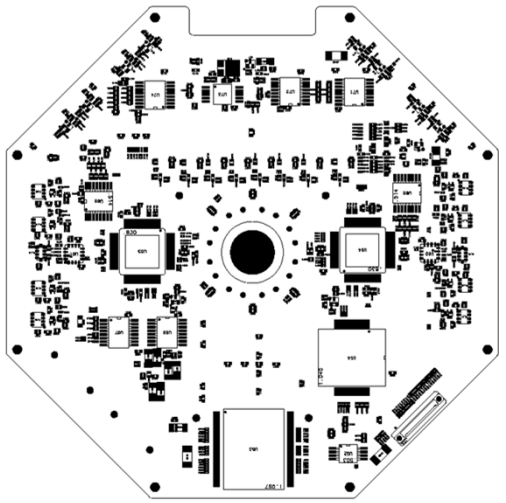
Thermal Analysis Overview

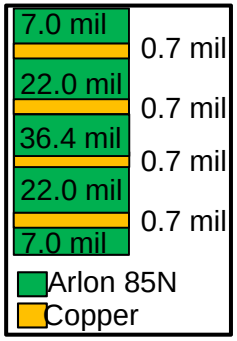
- Thermal Analysis Process
  - Instrument External Temperatures
    - Controlled with blankets, radiators and heaters
    - Determines internal PWA Board-to-slice interface temperatures
    - Interface temperatures used for board-level model boundary conditions
  - PWA Modeling
    - ECAD files (emn/emp) with component layouts are imported from Mentor Graphics
    - Software converts ECAD data to finite difference elements: resistors, interface, brick, plate, etc.
    - Model results include EEE part temperatures (board, junction & case) for all components
- Analysis Result Summary
  - Instrument chassis controlled to 25°C (max operating temperature),
  - PWA analyses assume 35°C frame temps, added 10°C margin to account for modeling uncertainties
  - Power dissipation provided by board leads
  - Evaluate thermal design and part margin for the EPI-Lo PWAs
    - Event PWA ➔ all parts operate with margin
    - Power PWA ➔ all parts operate with margin
    - Anode PWA ➔ all parts operate with margin

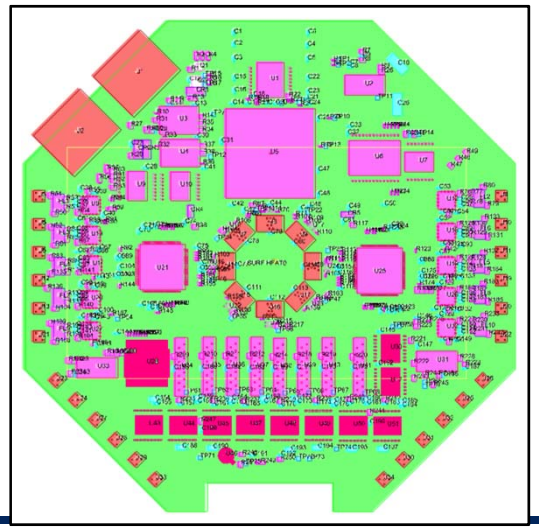
Event PWA Thermal Analysis: Model Overview

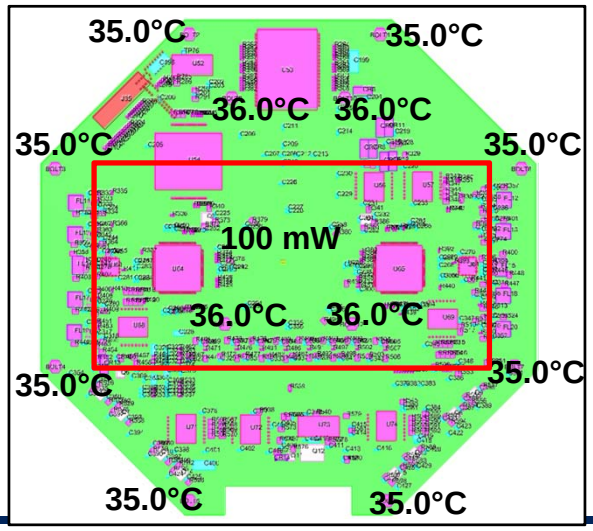
- 7464-4000 Event PWA
  - Detailed PWA model created using ECAD files
  - EEE parts mapped to thermal representations
  - PWB: modeled as 0.098” stackup with 4 (½ oz.) Cu planes
- Instrument level temps applied at PWA-to-frame mounting hardware
- EEE part maximum power dissipation in flight (1.532 W)
  - 1.432 W modeled on components
  - Component U54 has 560 mW, 3 sec. transient condition; steady state value of 36 mW used for analysis
  - Total of 100 mW spread on secondary side for passives





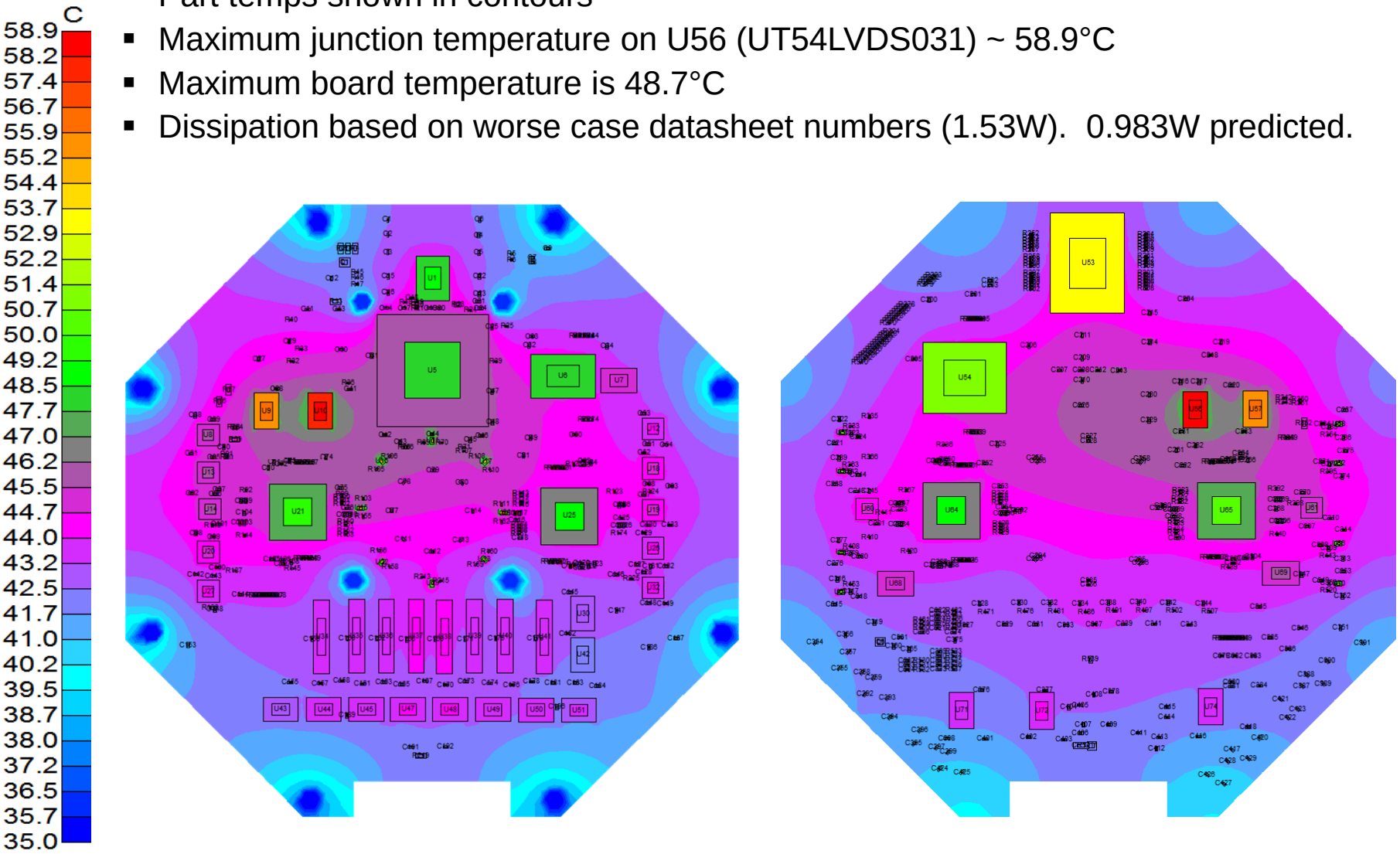


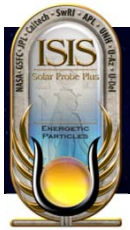




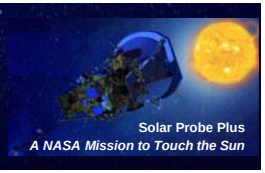
Thermal Analysis Results

- Part temps shown in contours
- Maximum junction temperature on U56 (UT54LVDS031) ~ 58.9°C
- Maximum board temperature is 48.7°C
- Dissipation based on worse case datasheet numbers (1.53W). 0.983W predicted.





Event PWA Modeling: Power Dissipation

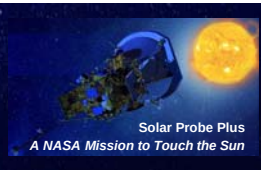


Ref	Part Number	PWR (mW)
U5	RTAX2000S-CGS624E	300
U10	UT54LVDS031LVE	60
U56	UT54LVDS031LVE	60
U57	UT54LVDS032LVE	50
U9	UT54LVDS032LVE	50
U53	HLXSR01632	45
U1	1103R40M00000BD	40
U54	UT8MR2M8-40YPC	36
U21	10946-TOF-D-03	33
U25	10946-TOF-D-03	33
U6	5962H0151704QXC	33
U64	10946-TOF-D-03	33
U65	10946-TOF-D-03	33
U11	ADCMP600BKSZ	18
U15	ADCMP600BKSZ	18
U16	ADCMP600BKSZ	18
U17	ADCMP600BKSZ	18
U22	ADCMP600BKSZ	18
U23	ADCMP600BKSZ	18
U24	ADCMP600BKSZ	18
U29	ADCMP600BKSZ	18

Ref	Part Number	PWR (mW)
U12	10946-CFD-D-03	16
U13	10946-CFD-D-03	16
U14	10946-CFD-D-03	16
U18	10946-CFD-D-03	16
U19	10946-CFD-D-03	16
U20	10946-CFD-D-03	16
U26	10946-CFD-D-03	16
U27	10946-CFD-D-03	16
U32	10946-CFD-D-03	16
U60	10946-CFD-D-03	16
U61	10946-CFD-D-03	16
U8	10946-CFD-D-03	16
U55	ADCMP600BKSZ	12
U58	ADCMP600BKSZ	12
U59	ADCMP600BKSZ	12
U62	ADCMP600BKSZ	12
U63	ADCMP600BKSZ	12
U66	ADCMP600BKSZ	12
U67	ADCMP600BKSZ	12
U70	ADCMP600BKSZ	12
U34	7425-4100-09	11.5

Ref	Part Number	PWR (mW)
U35	7425-4100-09	11.5
U36	7425-4100-09	11.5
U37	7425-4100-09	11.5
U38	7425-4100-09	11.5
U39	7425-4100-09	11.5
U40	7425-4100-09	11.5
U41	7425-4100-09	11.5
U43	ADC128S102QML	9
U44	ADC128S102QML	9
U45	ADC128S102QML	9
U47	ADC128S102QML	9
U48	ADC128S102QML	9
U49	ADC128S102QML	9
U50	ADC128S102QML	9
U51	ADC128S102QML	9
U68	10946-QDAC2B-03	5
U69	10946-QDAC2B-03	5
U7	10946-QDAC2B-03	5
U71	10946-QDAC2B-03	5
U72	10946-QDAC2B-03	5
U74	10946-QDAC2B-03	5

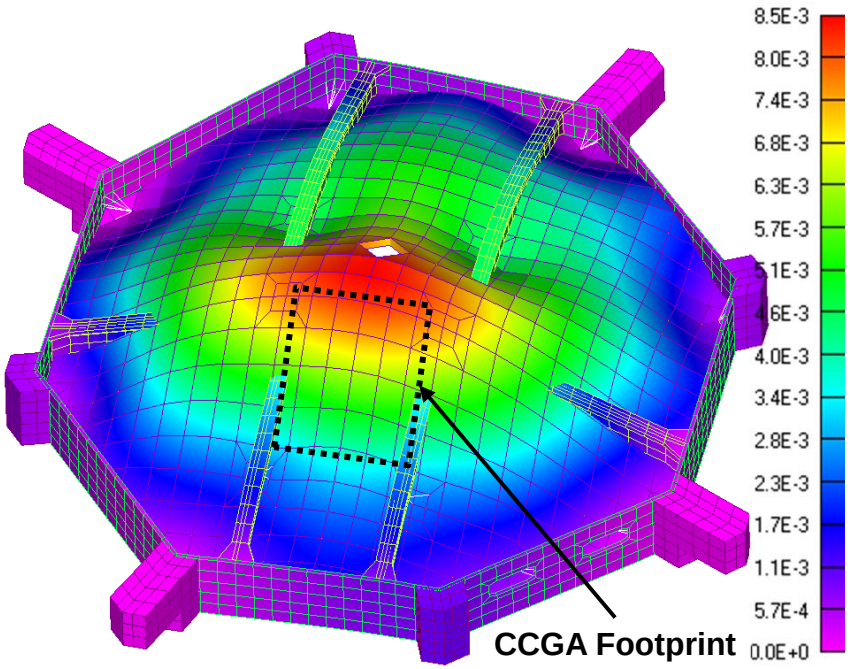
Event PWA Modeling: Model Results (Cont'd)



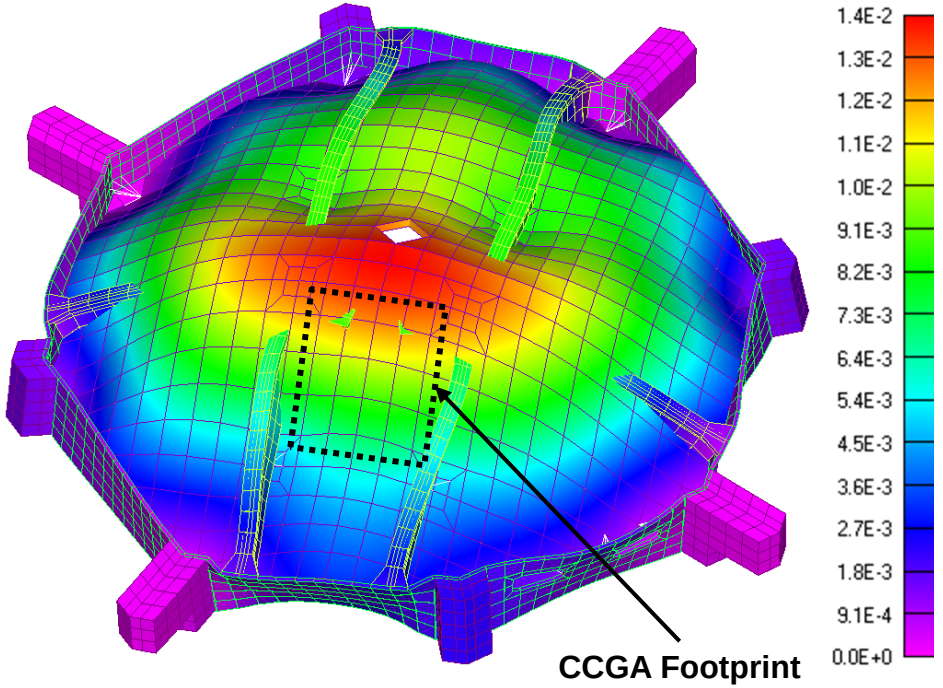
Ref Des	Library Name	Pdiss (W)	Tjunc. (°C)	Tcase (°C)	Tboard (°C)
U8	10946-CFD-D-03	0.016	45.7	44.9	44.9
U55	ADCMP600_KS-5	0.012	51.1	48.4	45.2
U58	ADCMP600_KS-5	0.012	52.6	49.9	46.2
U59	ADCMP600_KS-5	0.012	51.0	48.3	45.5
U62	ADCMP600_KS-5	0.012	52.8	50.1	46.7
U63	ADCMP600_KS-5	0.012	51.5	48.8	45.7
U66	ADCMP600_KS-5	0.012	52.7	50.0	46.3
U67	ADCMP600_KS-5	0.012	51.4	48.7	44.9
U70	ADCMP600_KS-5	0.012	51.6	48.9	45.4
U34	7425-4100-09	0.012	43.7	43.7	43.0
U35	7425-4100-09	0.012	43.6	43.6	42.7
U36	7425-4100-09	0.012	43.9	43.9	43.2
U37	7425-4100-09	0.012	44.1	44.1	43.5
U38	7425-4100-09	0.012	44.1	44.1	43.5
U39	7425-4100-09	0.012	43.8	43.8	43.1
U40	7425-4100-09	0.012	43.4	43.4	42.5

Ref Des	Library Name	Pdiss (W)	Tjunc. (°C)	Tcase (°C)	Tboard (°C)
U41	7425-4100-09	0.012	43.4	43.4	42.7
U43	ADC128S102QML	0.009	43.1	43.0	42.4
U44	ADC128S102QML	0.009	43.8	43.7	42.5
U45	ADC128S102QML	0.009	43.9	43.8	42.5
U47	ADC128S102QML	0.009	44.0	43.9	42.8
U48	ADC128S102QML	0.009	44.1	44.0	42.7
U49	ADC128S102QML	0.009	43.8	43.7	42.6
U50	ADC128S102QML	0.009	43.4	43.3	42.3
U51	ADC128S102QML	0.009	43.3	43.2	42.1
U68	10946-QDAC2B-03	0.005	44.8	44.7	43.3
U69	10946-QDAC2B-03	0.005	45.5	45.4	43.9
U7	10946-QDAC2B-03	0.005	45.1	45.0	43.6
U71	10946-QDAC2B-03	0.005	43.6	43.5	42.0
U72	10946-QDAC2B-03	0.005	44.0	43.9	42.5
U74	10946-QDAC2B-03	0.005	43.9	43.8	42.2

Vibration Analysis



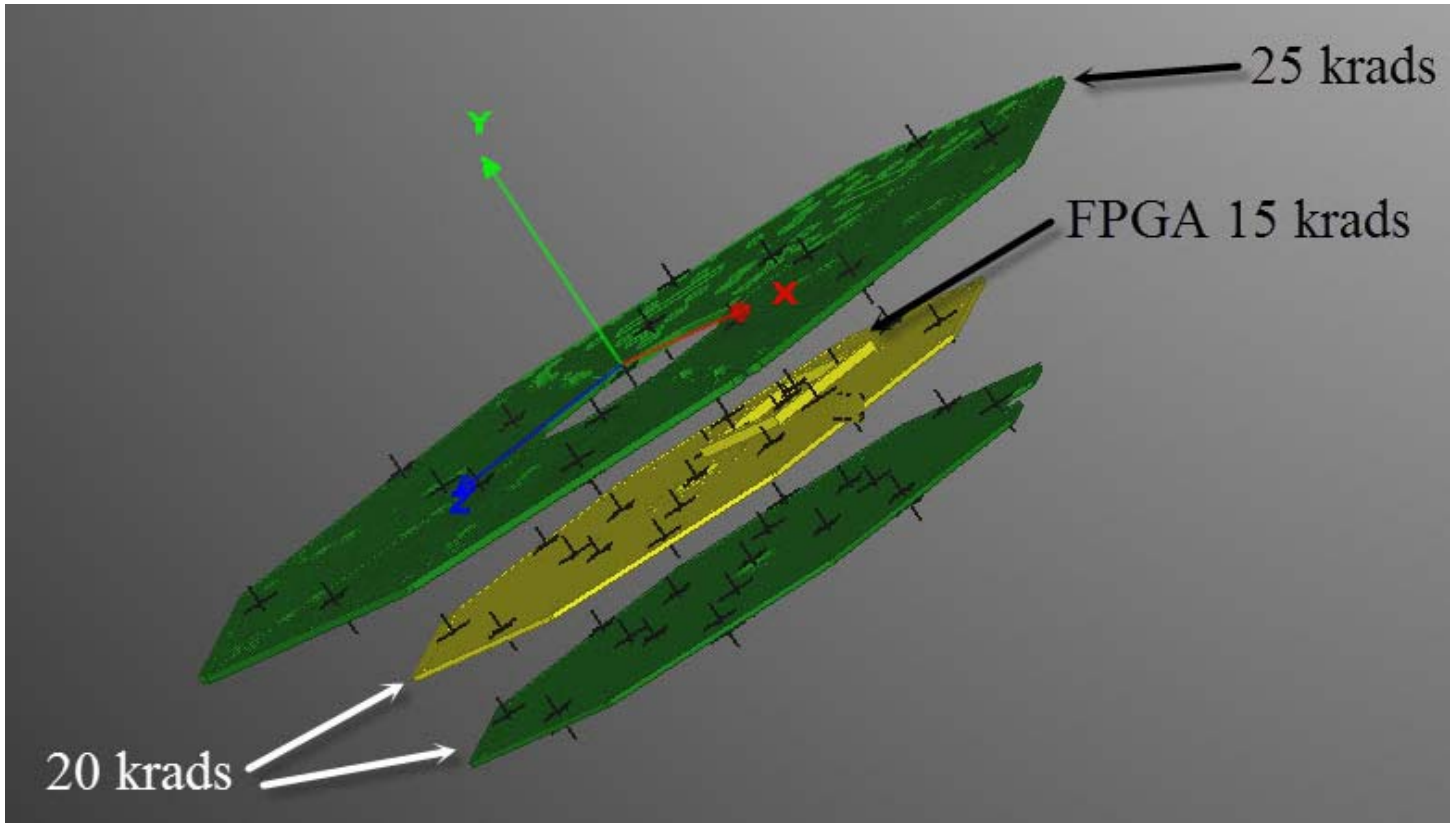
- Random Vibration Results
- Out-of-plane displacement (in) based on out-of-plane input
- EDTRD: 16.4 grms (max 1.25 G^2/Hz, from 60-200 Hz)
- Displacement over CCGA footprint: 0.004”, max allowable = 0.006”



- Quasi-static results based on random vibration Grms response
- Input vector (X, Y, Z): 25G, 160G, 25G
- Displacement over CCGA footprint: 0.006”, max allowable = 0.006”

FASTRad Analysis

- Updated analysis started by Dave Roth…
- PDR results showed no parts > 25krads (includes effective "RDM=2")

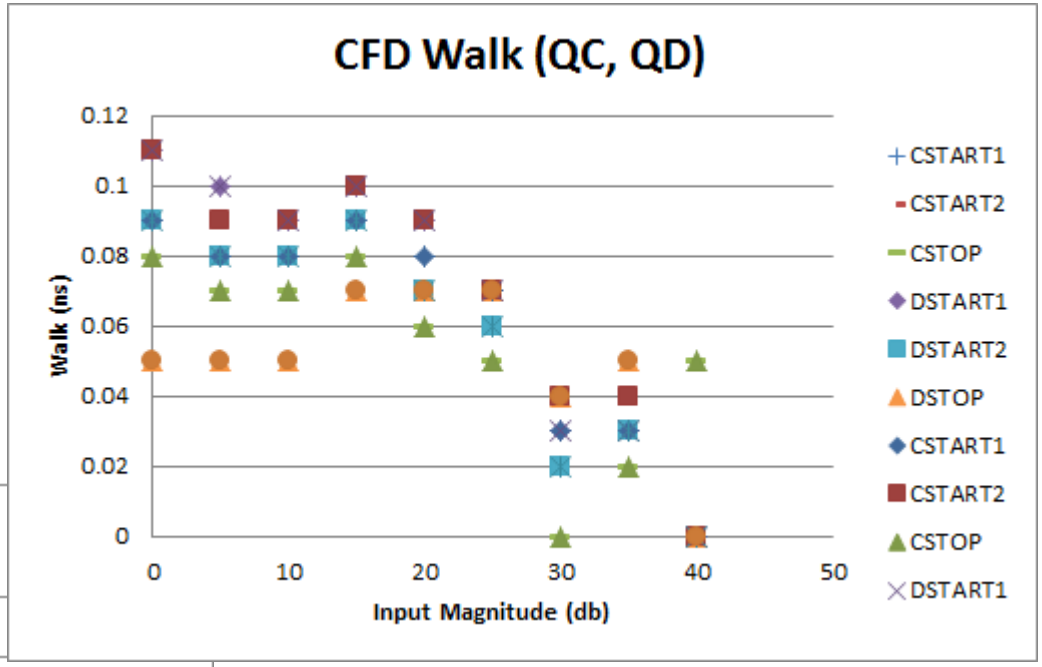


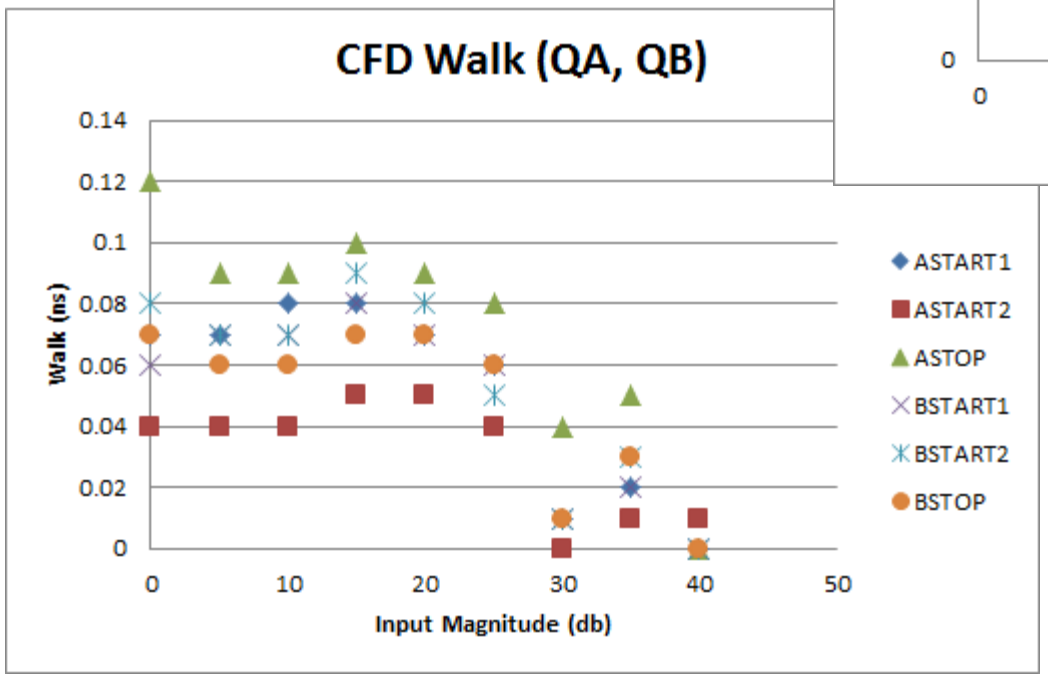
Peer review results

- Event and Power Board Initial Peer Review
  - August 21, 2013
  - Summarized with action items in memo SRI-13-029
  - 11 action items generated / 11 action items closed (6 for event board)
- Wait for peer reviews in November…

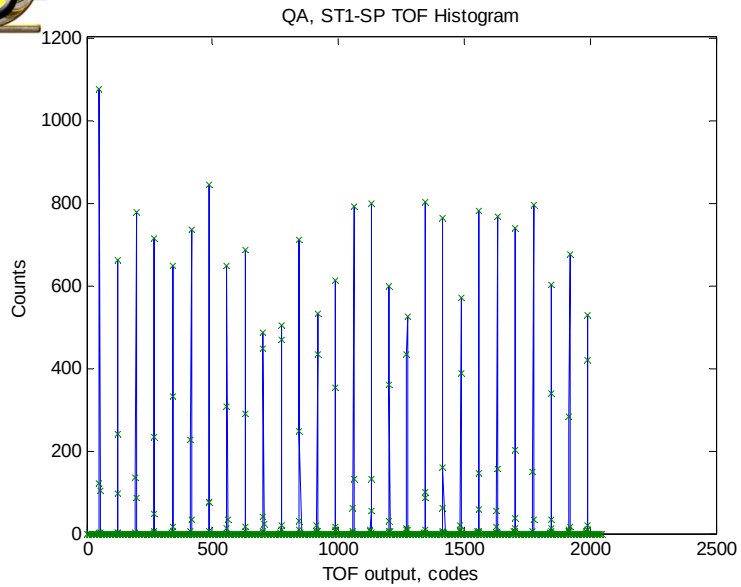
EM testing and analysis - CFD

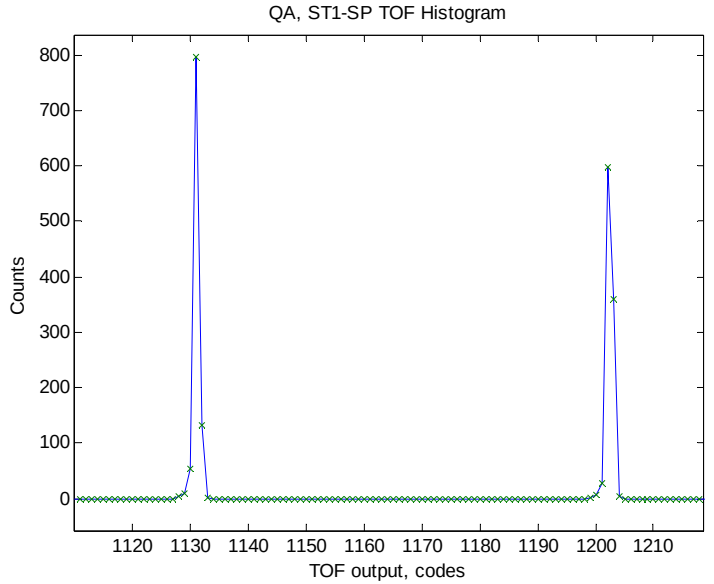
- CFD Walk
  - All walk < 120pS over 40db dynamic range
  - 40db = 10mV input

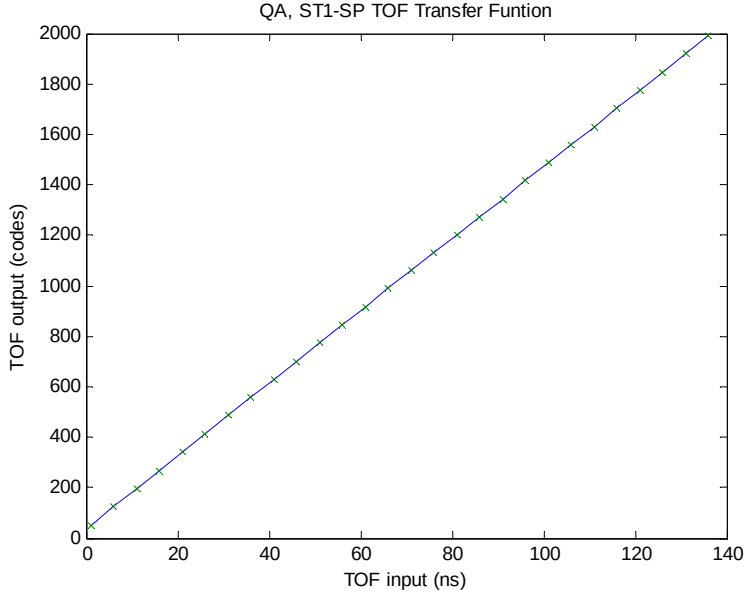


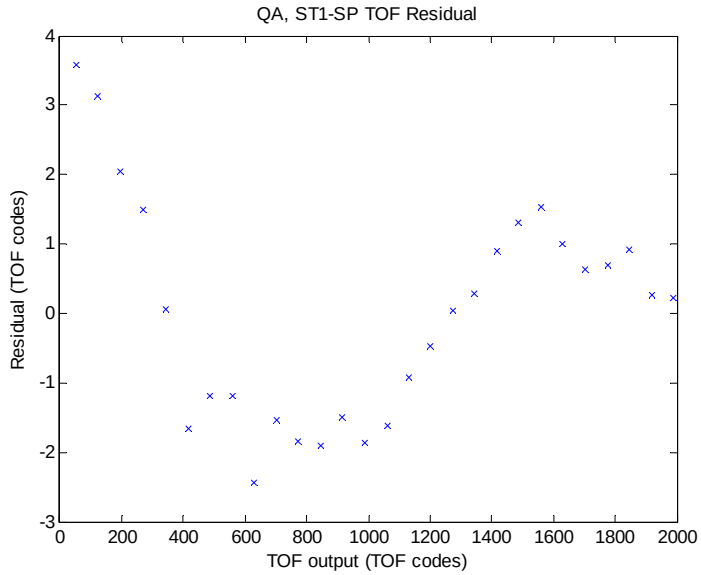


TOF Chip performance (73ps / LSB)

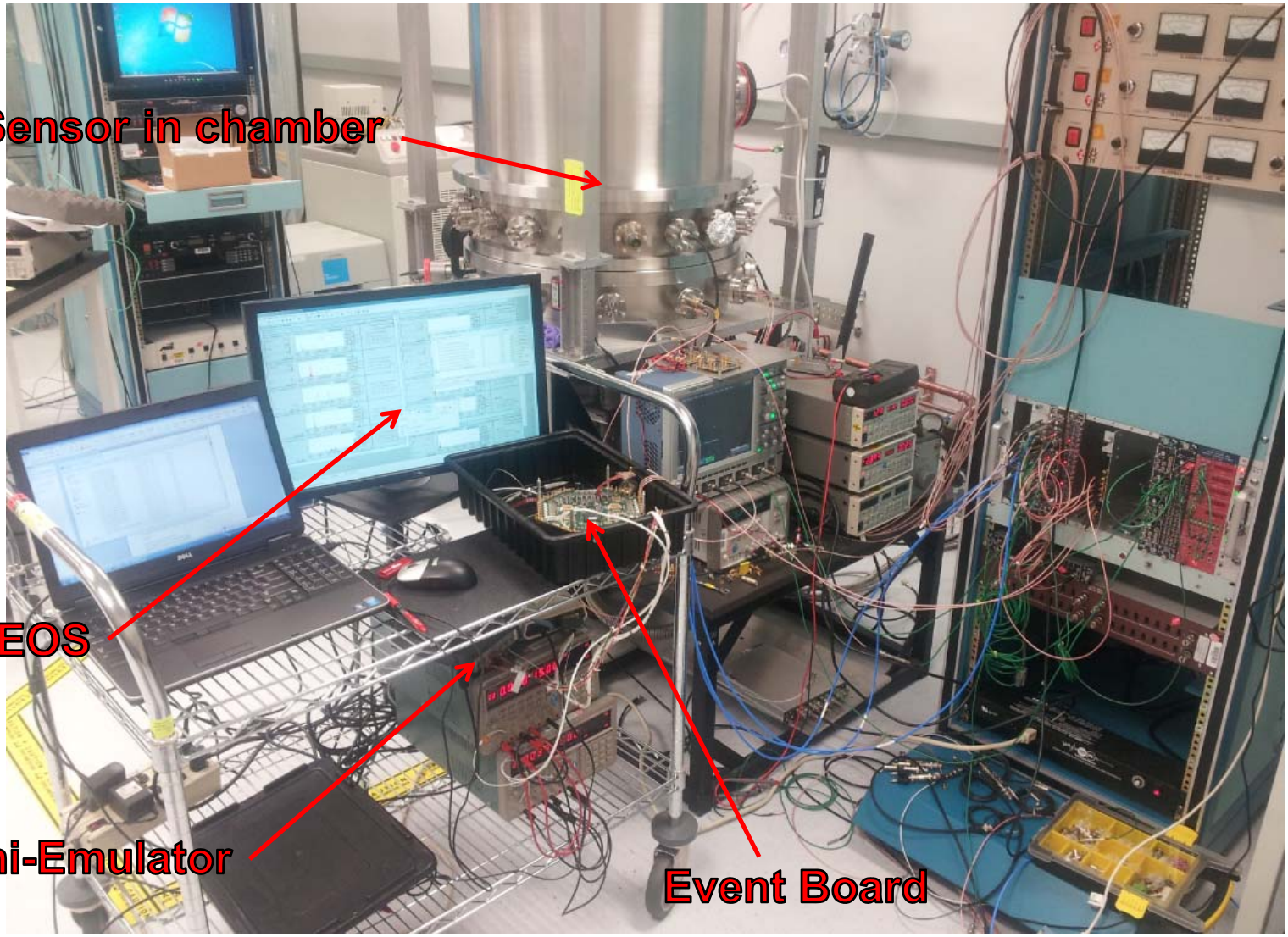




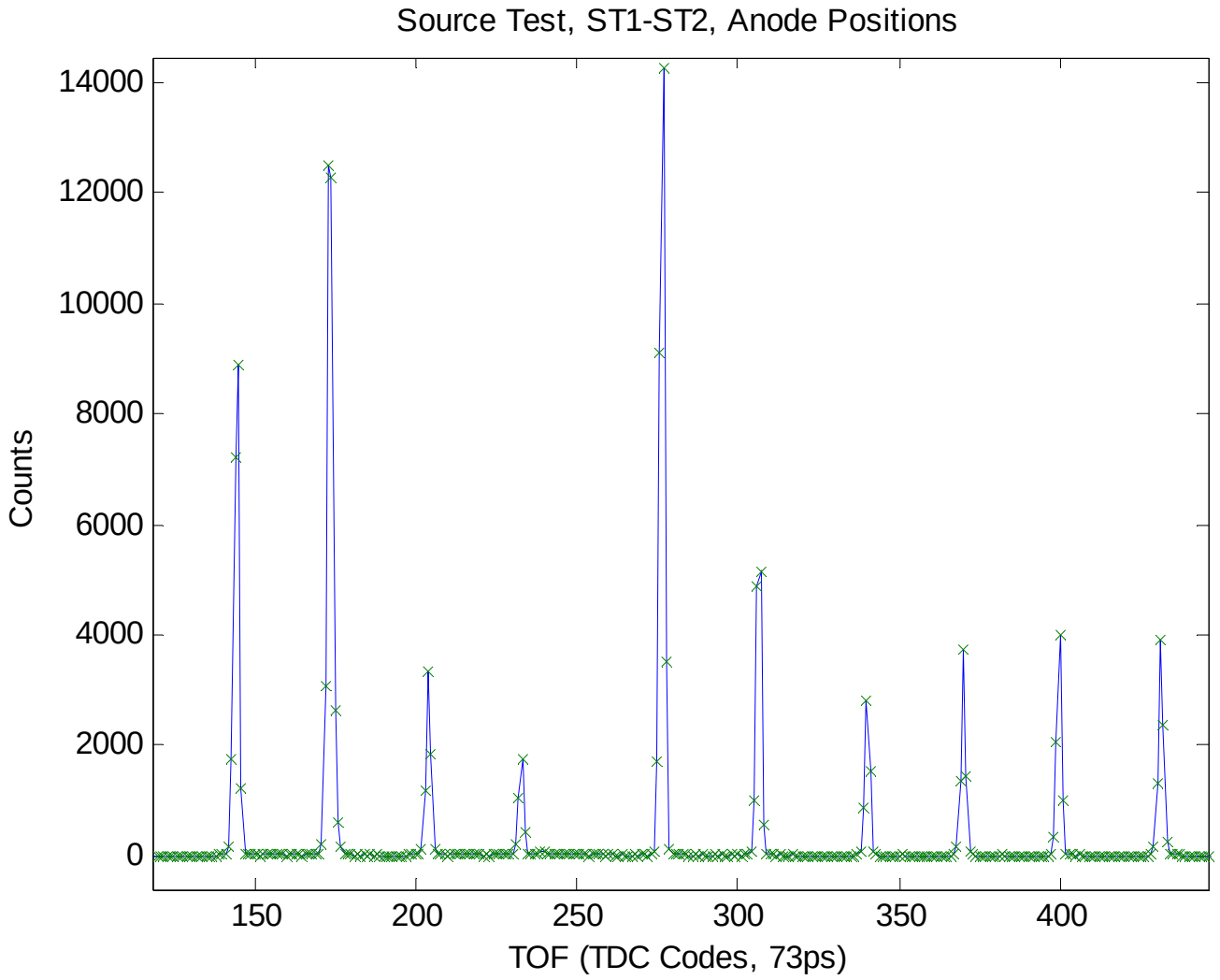




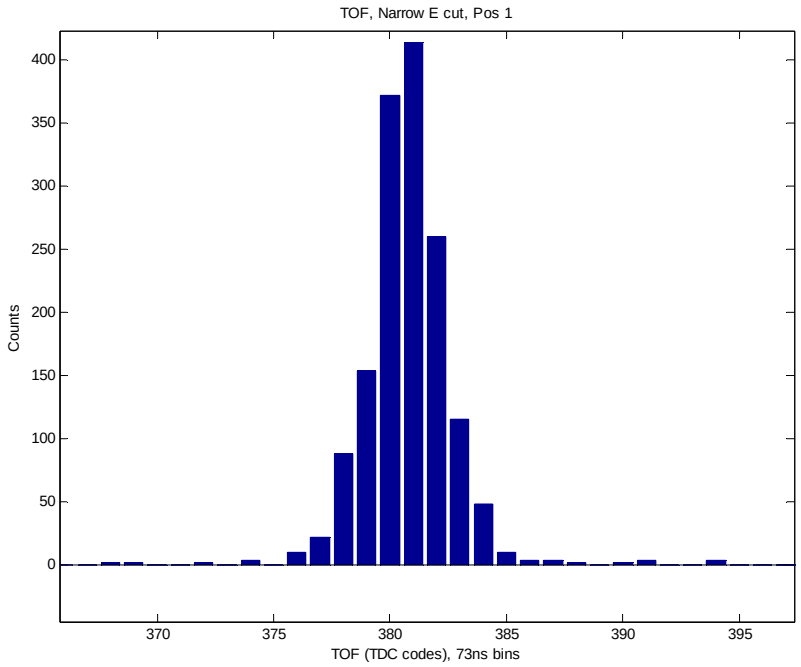
End-to-End performance: Anode Positions with sensor data

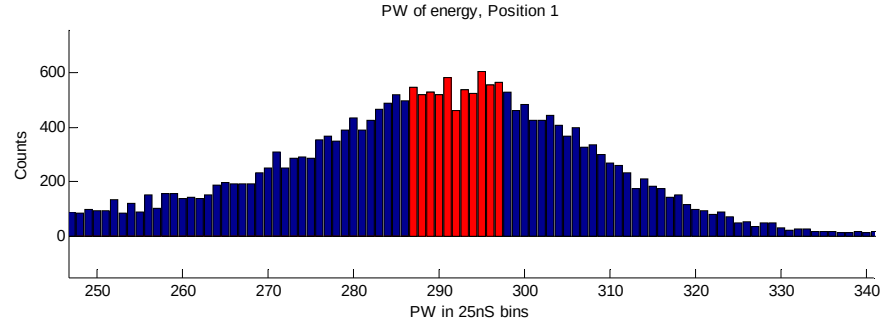


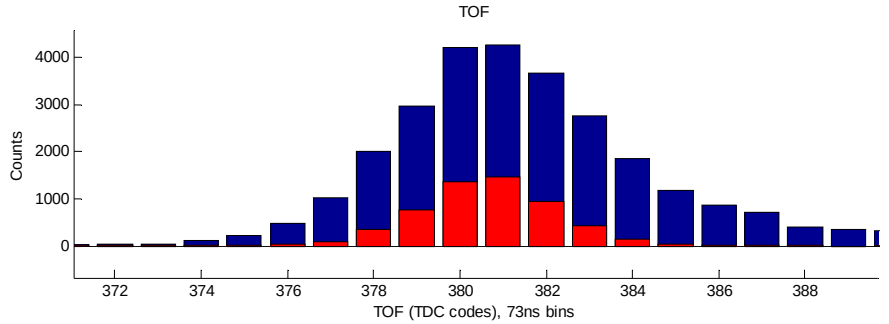
End-to-End performance: Anode Positions with sensor data



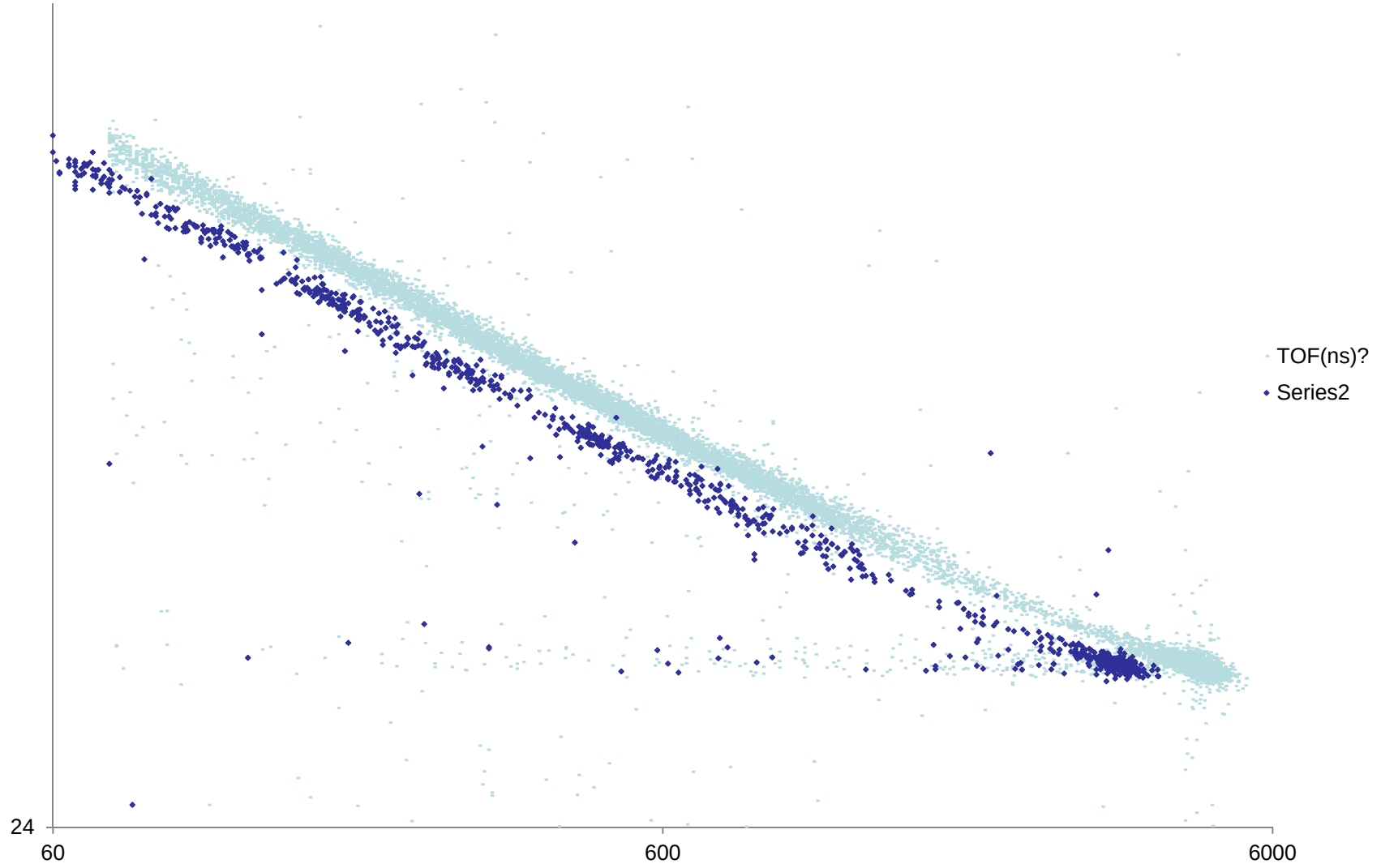
End-to-End performance: TOF of end-point alphas



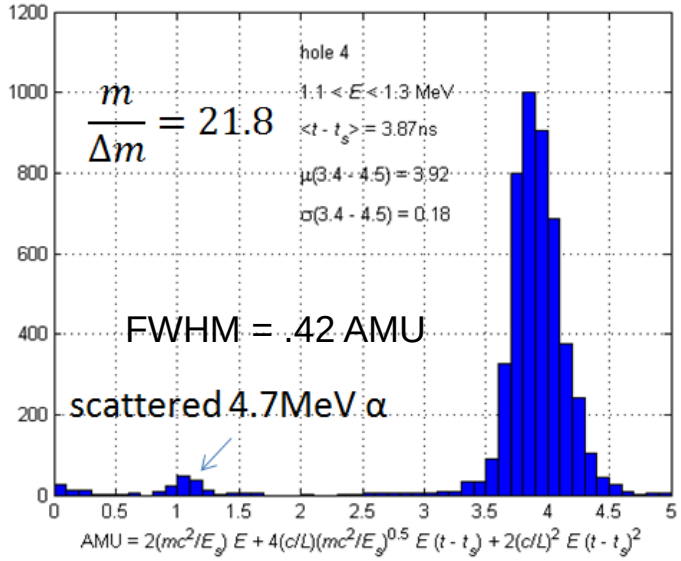


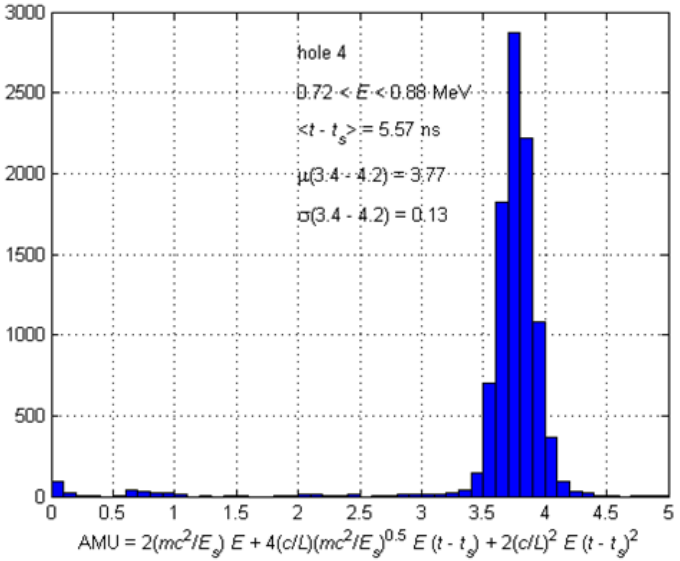


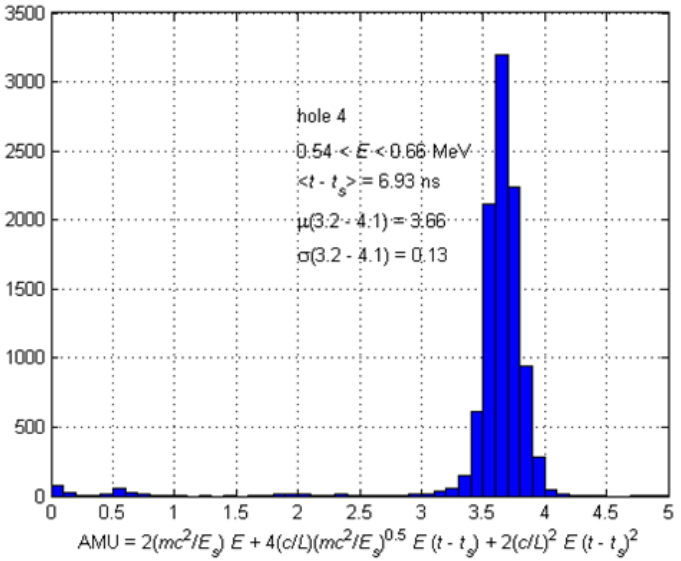
End-to-End performance: Alpha, He3 (simulated) track

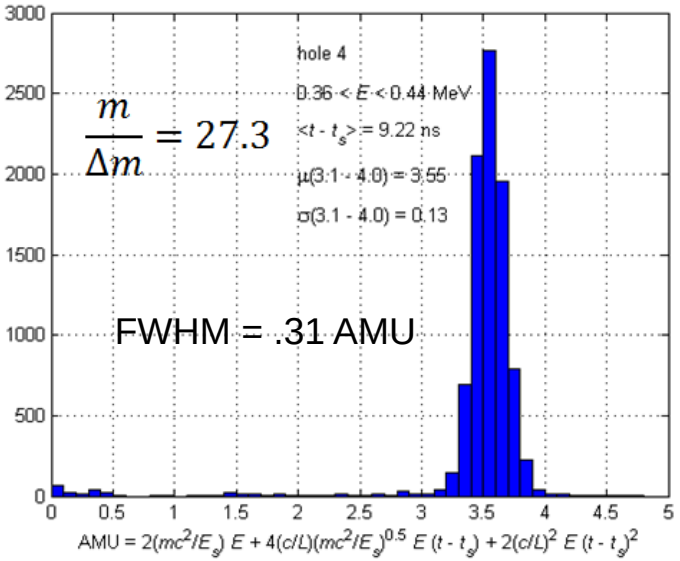


He4 Performance

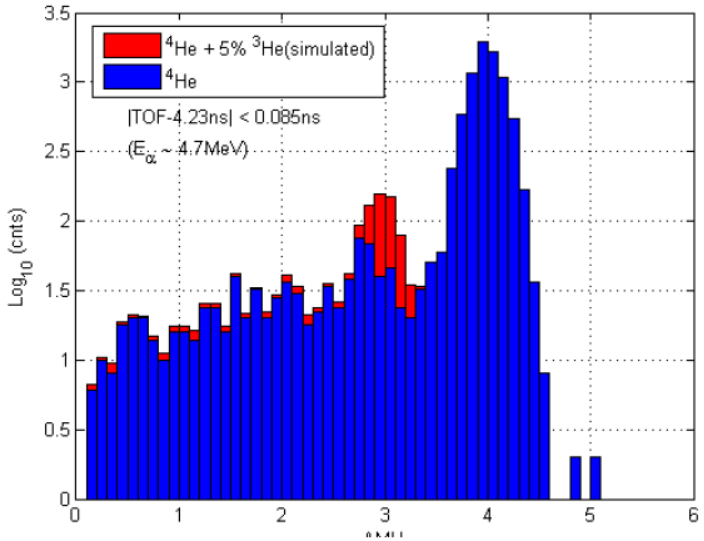


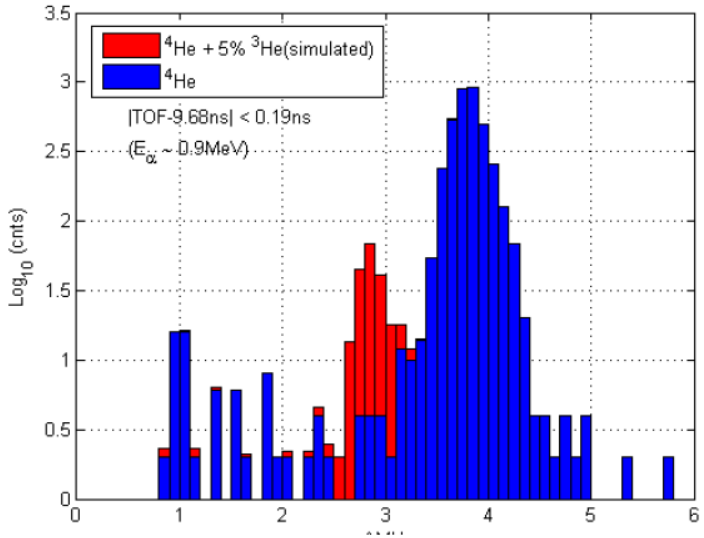




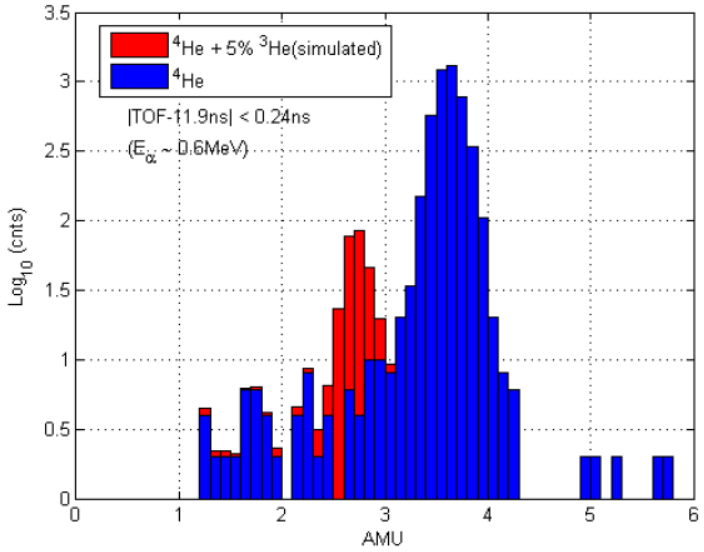


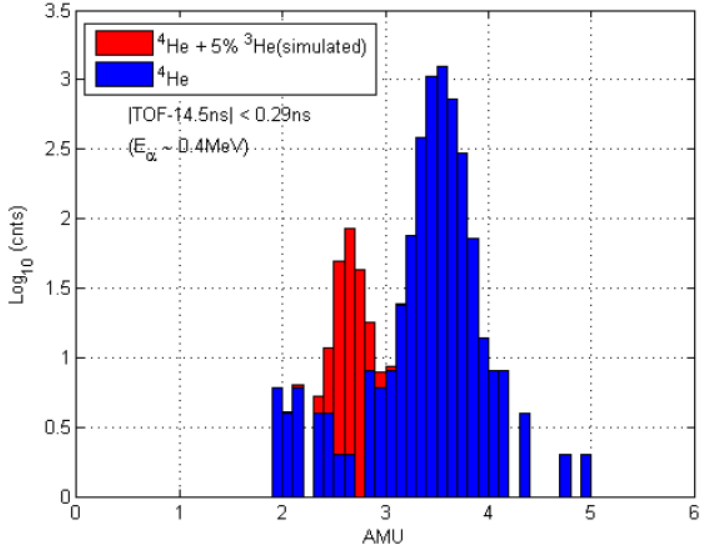
He3 – He4 Separation





Aperture 4





Remaining EM work

- Continue testing board with sensor

Status of special parts (e.g. ASICs)

- TOF ASIC
  - EM board has TOF ASICs from flight lot testing installed
- CFD ASIC
  - EM board has CFD ASICs from flight lot testing installed
- Both CFD and TOF ASICs have completed flight qualification testing

- Anything else or any relevant details from testing?

Plans for verification of design

- Initial build up by automated component placement and reflow will include all parts except Peak Detect SIPs, TOF chips, and ADCs
- Test procedures
- Temperature testing
- Flight software regression testing
- FPGA vector testing

Development milestones and procurement status

- EM complete and tested
- EM drawings signed off
- FM drawings complete but not signed off
- Need status on parts

Known changes from EM to FM

- No artwork changes?
- FM board will be fabricated from same design files as EM board?
- A few parts (delay lines) are jumpered across on EM and FM boards
- Some tailor components defined
  - CFD bias resistors
  - Linear regulator stability components

Drawing Status

- EM drawings released
- FM drawings complete but not released

Summary

- The Event EM board is fully tested
- FM board fabrication will begin after CDR