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HKCHIP and PHASIC pre-flight fab review summary

The HKCHIP and PHASIC are custom ASICs designed for use in the EPI-HI instrument of the Solar Probe Plus NASA mission. The two ASICs are intended to be fabricated at ON-SEMI’s C5N line with extra radiation hardening processing steps provided by Aeroflex Corporation. This note summarizes the final steps taken to identify and solve problems prior to the flight fab run in which both ASICs will be manufactured by combining the designs into a single reticle field.

HKCHIP

This ASIC contains the basic components needed to support the housekeeping, thermal and bias supply systems of a small space instrument. The ASIC includes a Sigma Delta type ADC, a 35 input analog multiplexor to select inputs for ADC conversion, 12 10 bit DACs with optional output buffer amplifiers, a power on reset circuit, and 12 digital outputs designed to sink 15 mA and intended to directly drive opt-couplers for control of heaters.

A prototype run of the HKCHIP design was performed through MOSIS using the ON-SEMI C5N process and initial testing suggested that the chip was entirely functional and adequate as is for use in EPI-HI. However, several problems were identified: 1) the linearity of the 10 bit DACs appeared to be good only to about 8 bits, when calibrated using the Sigma Delta ADC, 2) the rail to rail buffer amplifiers had a fairly large voltage offset (up to 30 mV) which could vary as a function of input voltage. Since these problems were not substantial enough to affect the EPI-HI application the HKCHIP was fabricated a second time with no changes as part of an engineering fab run of the PHASIC at ON-SEMI, in order to exercise the inclusion of two designs in a single reticle field.

In the past month the HKCHIP has been further studied in an effort to identify any additional problems prior to flight fab. Automatic test algorithms were developed for later use in screening the parts and to aid in a more thorough search for problems. During this process one additional problem was noticed: that the optional rail to rail buffer amps can oscillated when their outputs are close to the 5V or GND power rails. This problem does not affect all buffer amps, but is typically present. The root cause was easily found through SPICE simulation and is due to variability of the offset voltage in differential amplifier stages imbedded in the output stage and intended to aid the output stage current mirrors to operate close to the rails. Some consideration was given to removing these differential amplifiers in order to simplify the design. This could be expected to eliminate the near rail oscillation and allow operation somewhat closer to the power rails that in the present design.

Also during the more thorough testing it was noticed that the lack of 10 bit performance of the DACs was potentially due to the input bias current of the Sigma Delta ADC. This bias current was found to be comparable to that of similar designs reported in the literature. The current is proportional to ADC operating frequency. At the maximum operating frequency of 2 MHz the current varies from about 8 to 28 nA as a function of input voltage and is due mainly to charge injection from the Sigma Delta ADC input switches. Although the following obvious solution to this problem was not found in the literature, it was noted that if the input current is proportional to operating frequency it should be possible to obtain conversion results at two different frequencies and infer both the source impedance and the unloaded source voltage. Further study showed that indeed the input current was a linear function of frequency and approached zero current at zero frequency. It was found that by performing conversions at 2 MHz and 1 MHZ, with results N2 and N1, the unloaded voltage could be estimated accurately as 2\*N1-N2, while the product of source impedance times input current could be inferred as proportional to N1-N2. Recalibration of the 10 bit DACs using the input bias corrected ADC results revealed that the DACs indeed do perform at the 10 bit level, i.e. that the maximum deviation of the actual DAC output voltage from the nominally correct value of (setting/1023)\*Vref is always less that (1/1023)Vref. Figure 1 shows the linearity error of one of the 10 bit DACs as measured by the Sigma Delta ADC operating at dual frequency as described above. Figure 2 shows the uncorrected result (based on N2 only), while Figure 3 shows the difference N2-N1. In all three figures the horizontal axis is DAC setting value ranging from 0 to 1023, but also closely corresponds to DAC output voltage ranging from 0 to 5V.

Figure 1

The performance of the Sigma Delta ADC itself was measured using a precision Electronic Design Corporation DAC, whose performance was in turn checked using an HP precision DVM. (Both instrument’s calibration had expired and so these measurements need to be repeated later.) Once the Sigma Delta ADCs gain and offset where trimmed by a simple procedure and operated with a maximum count of 50,000, the accuracy and noise was verified to be less than a single count (0.1mV) over the range from 1 mV to Vref (nominally 5V) – 1 mV.

Once automated test procedures were in place, a single part (SN7) was tested at -35C, 25C, and 45C. No problems were noticed over temperature. DACs, ADC, digital outputs, input multiplexor and buffer amps all functioned properly over temperature, with no significant change in DAC or ADC performance.

Figure 2

Figure 3

The stability of all buffer amps over the 0.4 to 4.6 output voltage range was verified at each temperature using an oscilloscope to view the outputs while the DACs were ramped up and down to create triangular waveforms over that output range. The operation of the amplifier within the Sigma Delta ADC was also observed at each temperature using the scope monitor output dedicated to this purpose. No change was noted in the critically damped step transitions that occur during conversions, consistent with preserved gain and phase margins over temperature.

The operation of the digital outputs intended to drive optocouplers was tested by connecting each one of the outputs to a separate 221 ohm load resistor connected to 3.3V. Each of the 12 digital outputs were also connected to a separate input of the 35 input analog multiplexor and both the low and high output level state voltages were measured by the Sigma Delta ADC at each temperature. The output high voltage measurements always just equaled the 3.3 supply voltage, while the output low voltage measurements reveal how close to ground the outputs can pull the 221 ohm load, and hence how much power is dissipated in the output’s NMOS fet. The output low measurements over temperature showed the expected change caused by increasing FET transconductance with decreasing temperature. At the worst case (45C) the FETs still are able to pull down to less than 200 mV for a worst case power dissipation of only about (200mV)(15mA) = 3 mW.

PHASIC

Most PHASIC functions had been tested thoroughly prior to the recent month. However, in order to facilitate a comprehensive pre-flight-fab review, the automated test procedures used to screen flight parts for the earlier STEREO program were brought up to date (accounting for SPP design mods) and used to test a collection of eight PHASICs which contained die from the ON-SEMI engineering run. The PHASICs tested included one that was soldered down to a fixture that had been developed purely to debug noise issues which had plagued our socketed PHASIC test fixture. (Those noise issues had indeed been determined to be due to the socket and were ultimately fixed in the socketed fixture by use of an array of pogo pins to provide better ground connection to the socketed PHASIC body.) Temperature testing was recently performed only on the soldered down PHASIC.

The automated tests cover every aspect of PHASIC operation and include DC and AC measurements. The DC measurements check power supply current levels, bias voltages, DC levels at all internal test points, and the performance of DC elements such as the input current DACs and the current DACs that set signal thresholds (see AOG discussion below). The AC tests include measurement of each channel’s transfer function using the internal test pulsers and tests of the on-chip scalars and other dynamically stimulated functions. The AC tests are performed at several temperatures spanning the operation range from -35 C to +45 C. The excellent linearity and stability of the transfer functions is dependent upon the proper functioning of all the amplifiers in the signal processing chain and hence provide an end to end diagnostic of proper amplifier margins.

Using the full suite of automated tests revealed only two problems that needed to be fixed:

1. Double counting of singles scalars. Each PHASIC contains 16 pulse height analysis systems that each contain a low noise preamplifier whose output is coupled to two signal processing chains, one with high and one with low gain. Each signal processing chain contains a peak detector and Wilkinson rundown type ADC, in addition to a 23 bit scalar that counts the number of “events” by counting the number of “rundown” signals from the peak detector. (The rundown signal starts just after peak detection and lasts until the peak hold capacitor has been discharged linearly down to a level that is about 50 mV below baseline.) During automated testing of the scalars the internal test pulsers are used to stimulate events and the scalars are readout before and after a roughly fixed number of events have been generated. Most scalars worked properly such that the number of events generated matched the difference in the scalar readings. About half of the PHASICs tested showed all scalars working properly at room temperature. The other half showed that a few of the 32 scalars double counted, while one scalar over counted by a few percent. The scalars are ripple counters using D type flip flops. One of the changes to the PHASIC design for SPP was to replace the D flip flops with a “better” design that took less layout area. So the suspicion was that this change had something to do with the double counting. However, since the scalars mainly double count it seemed clear that the trouble resided only at the first flip flop of the 23 bit chain. The suspicion therefore was that the problem might be due to a glitch arriving at the first flip flop, i.e. a glitch on the rundown signal. So a SPICE simulation was performed which focused on the circuitry in a block called “belogic” that generates the rundown signal. The simulation included the first two stages of the scalar’s ripple counter. The very first such simulation produced a glitch that caused the counter to make an extra count. The glitch occurred not at the beginning or end of the rundown signal, but later at the time when a signal called PHARST\* performs an asynchronous clear of two flip flops involved in generating the rundown signal. The glitch results from the different delay time of the clear through the two flip flops and represents a fairly typical type of logic design error. It must have been present, though undetected, in the STEREO PHASIC. Now the question became why the glitch typically does not cause double counting. The initial SPICE simulation lacked parasitic layout capacitance and so the layout was inspected and the appropriate amount of capacitance on the relevant nodes was added to the simulation. This added capacitance reduced the glitch amplitude below the threshold for double counting. Presumably then, if the glitch was the root cause of the double counting, then the fact that only a few counters double count can be understood as the result of a marginal situation in which the glitch amplitude could vary as a function of fabrication variables such as P and N MOS FET threshold. To see if this was plausible the simulation was rerun with SPICE models representing four “corner cases”: (fast NMOS, fast PMOS), (fast NMOS, slow PMOS) , (slow NMOS, fast PMOS) and (slow NMOS, slow, PMOS). For the fast-fast case the glitch amplitude was indeed enhanced, nearly, but not quite, to the point of causing double counting. With these results in hand, temperature testing was performed and it was noted that double counting symptoms were unchanged at 45 C relative to 25 C, but a few additional scalars double counted at -35C. Indeed one scalar was observed to begin over counting by only a few percent near about -25C and transitioned to double counting by -35C, consistent with a marginally counting glitch that becomes more pronounced due to the increase of FET speed at lower temperature. Finally, the glitch hypothesis was checked by reading out the scalars just before and just after the leading edge of the PHARST\* signal and indeed the double counting scalars showed an extra count caused by PHARST\*. This test was arranged so that it could be repeated with no change except to delete the PHARST\* signal and deletion did cause the disappearance of the extra count from the double counting scalars. There were several options to remove the glitch and the one deemed to have the least possibility of unintended consequences was chosen. This fix involves the addition of an OR gate (NOT gate plus inverter) that guarantees the order in which the two flip flops are cleared.
2. Excess standing current at the AOG output. The AOG (Amplifier-Offset-Gate) is a section in each of the 32 signal processing chains on the PHASIC. Its purpose is to provide one of the amplifying/shaping stages, while also imposing a programmable threshold below which signals are blocked (gated) and above which signals are passed. It also can respond to a “CLG” (close linear gate) signal to block passage of all signals. This happens routinely during the processing of an event, since following peak detection it is desirable to block subsequent signals which could contaminate the detected peak voltage. To facilitate AOG operation the output of its shaping amplifier stage is converter from a precision voltage to a precision current. From this current, which must include the standing bias current of the output stage itself, is subtracted a programmable DC current. If the result is positive the remaining current passes through the gate portion of the AOG and the voltage signal is reconstituted on a subsequent load resistor. If the result is not positive no transient output occurs from the gate and the signal is blocked. During automated testing of the AOG section, the programmable threshold current is decreased until it falls below the amplifier’s output bias current allowing the baseline signal to pass through the gate. The point at which this occurs can be detected and allows the amplifier’s output stage bias current to be inferred. Due to process variations this bias current does vary from channel to channel and PHASIC to PHASIC. However, it was noted that while the range of variation was the same as for the STEREO version, the mean value of the bias current was somewhat shifted from the intended value of 5 uA to near 6.5 uA. One of the mods for SPP had been to lower the values of some resistors in the AOG in order to lower noise. The shift of the bias current apparently is caused by lack of resistor geometry matching in the layout of the new resistors. The consequences of this shift are to change the range of the programmable threshold setting from the range (0.002 to 0.06 of full scale) to a smaller range (0.002 to 0.04 of full scale). This was not a fatal problem, but it was decided to fix this since the fix involves only changing a single resistor from a value of 125K to 126.5K by slightly lengthening the resistor.

A third problem was identified that didn’t need to be fixed. The 23 bit scalars (the same ones that occasionally double count) were found to not reset correctly to zero. The problem was tracked to a design error in a new more compact flip flop used in various places to reduce the layout area and allow other mods to occur without growing the overall PHASIC die area. The design error causes the asynchronous clear of the flip flop to only work properly when the clock signal to the flip flop is high. The defective flip flops are used in three places in the PHASIC: 1) in the Wilkinson rundown ripple counters, 2) in the 23 bit scalar ripple counters and 3) in the 16 bit shift registers that were added to provide a cross-talk/pileup diagnostic. In cases 1 and 3 the clock signal turns out to be high during the clear operation, so the clear works. In case 2 the clear function is superfluous since an equivalent alternative to periodically reading out then clearing the counters is to read them out without a subsequent clear and subtract the prior readout value to obtain the counts recorded in the most recent interval. This change in the mode of operation of the scalars was implemented in the automated PHASIC test, demonstrating the method works, and also allowing the discovery of the double counting problem discussed above.