Solar Probe Plus HKchip User's Manual

WRC 8/12/13 original
JAB 9/04/13 editted

This document provides information on the use of the Solar Probe Plus HKchip (HouseKeeping chip) in the EPI-Hi instrument of the NASA's Solar Probe Plus mission spacecraft.

Document Version History

The HKchip design is new for Solar Probe Plus. The first version (8/12/13) of the manual was written after testing of prototype chips from a non-radhard run of ON Semi's C5N process, but before submission of the flight fab using Aeroflex's additional radiation hardening process steps. Editted (9/04/13) added diagrams, tables.

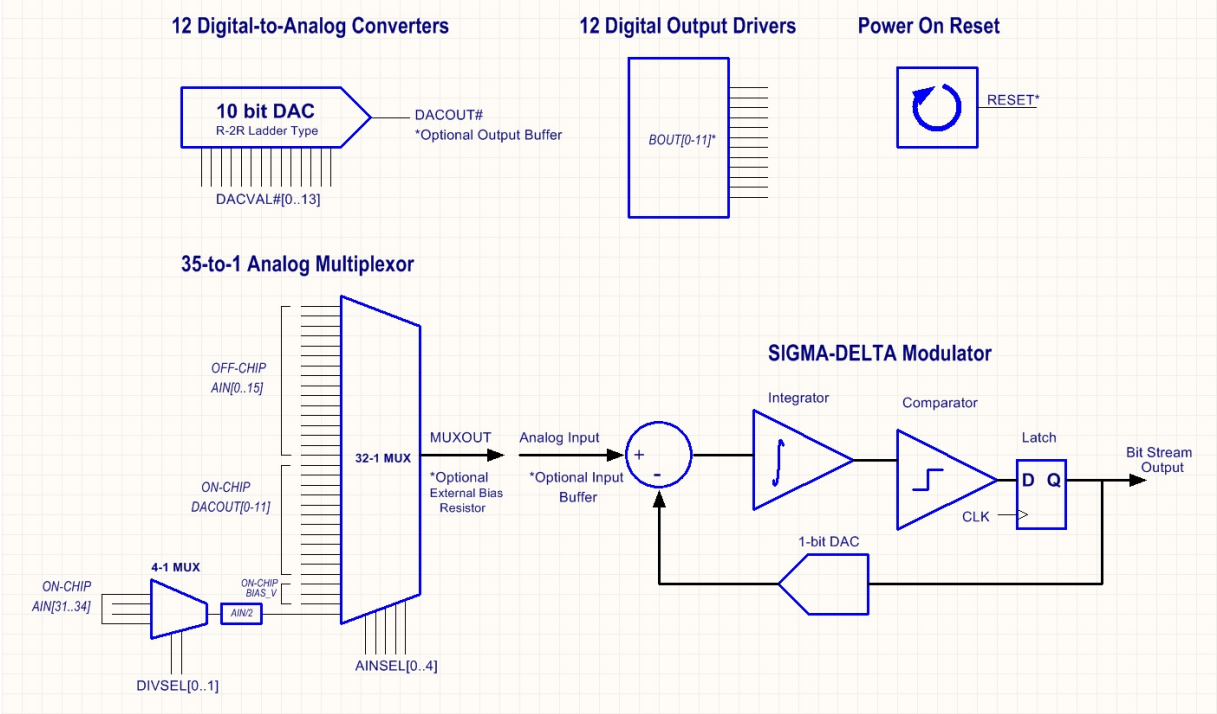

Figure 1: HKchip Block Diagram

Chip Overview

The Solar Probe Plus HKchip (hereafter, "the chip") is a custom-designed CMOS VLSI circuit that provides housekeeping functions typically needed in small space instruments. A block diagram of the chip is shown in Figure 1. The chip includes 12 10-bit DACs, a delta sigma modulator, a 35-input analog multiplexor, 12 digital outputs designed to drive opto-couplers for heater circuits, and a power on reset circuit. The analog multiplexor accepts 16 inputs from off-chip and 19 from on-chip, which include the 12 DAC outputs. The DACs are implemented as R-2R ladders and may be optionally buffered using on-chip unity gain amplifiers that function to within 20mV of the power rails. A similar unity gain buffer may be optionally configured to buffer signals at the input to the delta sigma modulator. Logic to operate the delta sigma modulator is not included on the chip, but is rather intended to be implemented in an external FPGA, allowing an easy trade-off between resolution and conversion time.

A unique feature of the HKchip is that the inherently low precision DACs may be ganged to yield very fine resolution, approaching 20 bits rather than 10. This feature together with the ability of the delta sigma modulator to provide precise measurements of the DAC output voltages allows the HKchip to be used to generate precise programmable DC voltages, with performance comparable to a 17-bit DAC. For EPI-Hi this enables accurate calibrations of the pulse height analysis channels without the need for external lab equipment. For the first time, a precise electronic calibration of the pulse height analysis channels should be possible in-flight.

The chip is designed for fabrication using ON Semiconductor's 0.5um CMOS process (C5N) incorporating high density linear capacitors and high value resistors suitable for mixed-signal designs. To achieve >100krad total dose tolerance for flight the chip will be fabricated with proprietary radiation hardening steps provided by Aeroflex Corporation.

The layout of the chip makes use of guard rings intended to raise the threshold for single event latchup to a high enough level to make latchup protection circuitry unnecessary. Similar guard rings were used in the layout of prior chips, for which latch-up testing at the Berkeley Cyclotron, found no latch-up up to an L.E.T. of 80 MeV/(mg/cm2).

Table 1. HKchip Specifications

# of 10 bit DACs	12
DAC linearity (unbuffered)	<0.5% max deviation from straight line
DAC impedance (unbuffered)	500kohm +- 10%
# external analog inputs	16
# internal analog inputs	19 (including 12 DAC outputs)
Delta Sigma Modulator max freq	4 MHz
Delta Sigma Modulator input current	<50nA
Unity gain buffer offset voltage	<25mV, from 20mV to Vcc-20mV
Unity gain buffer input current	<1pA
# of digital outputs	12, with 20mA sink capacity
Total dose tolerance	>100krad
Latch up threshold	>80 MeV/(mg/cm2)

HKchip Design and Operation

Power Supply Requirements. The chip operates with power supply voltages: 5Volts analog (a5V) and digital (d5V), 5Volts reference (5Vref), and digital interface supply voltage (ioVdd) in the range of 3.3 to 5Volts. Supply currents for d5V, ioVdd, and 5Vref are each less than 1 mA. Supply current for a5V depends on the number (N) of buffer amplifiers in use and is 1mA + (N * 1 mA). Since there are a total of 13 buffer amplifiers (12 for the DACs and 1 at the modulator input), the maximum a5V current is 14mA and maximum power consumption is 70mW. The diagnostic buffer amplifier used to deliver the modulator amplifier output to the ampmon pin draws 1.8mA from a5V when enabled. (In normal operation this amplifier is turned off.)

Maximum Voltages. The absolute maximum safe operating voltage is 5.5V. The absolute maximum safe voltage on input pins is "digital 5V" plus 0.5V. The maximum safe input current on digital inputs is 10mA (TBR).

DACs. The 10-bit DACs are intended to provide programmable DC voltages to control various instrument settings such as detection thresholds and HV bias voltages. The DACs may be used

either with the output buffered or unbuffered. The unity gain buffer amplifiers are designed to drive a resistive load of 20kohm. The unbuffered DAC output impedance is 500kohm +- 10%. While the DACs provide 10-bit resolution, the linearity is at only the 8-bit level. Each DAC spans a voltage range from its lower to upper reference voltage, normally 0 to 5V. However each DAC may be configured with either or both of its reference voltages sourced from neighboring DACs. For example, to provide more resolution in the DAC output, neighboring DACs could be used to set the lower reference to 1V and the upper reference to 1.5V so that the 10-bit DAC output spans the range 1 to 1.5V rather than 0 to 5V, improving the setting resolution by a factor of ten. This feature, together with the capability for each DAC output to be routed to the delta sigma modulator for precise DC measurement allows the relatively low precision DACs to be used to create high precision output voltages. In this case the DAC settings are iterated until the voltage measured by the modulator agrees with the desired setting. In this mode DAC output voltages can be set to within 50uV (10ppm of 5V) of any desired value between 20mV and ref5V-20mV. In EPI-Hi the capability of the HKchip to generate precise DC voltages enables built-in accurate calibration of the pulse height analysis chains without the need for external lab equipment, and hence allows accurate electronic calibration to be done in-flight.

Each DAC is controlled by a 14-bit word comprised of bits ampsel(1 bit), ampon(1 bit), refhi-sel(1 bit), reflo-sel(1 bit), R2Rsetting(10 bits) in order of most to least significant (the time order in which bits are serially loaded). The ampsel bit when set turns on an analog switch that connects the buffer amplifier to the DAC output pin. When cleared that switch is turned off and another switch is turned on to connect the unbuffered DAC voltage to the DAC output pin. The ampon bit when set applies power to the unity gain buffer. (So to obtain buffered output both ampsel and ampon bits need to be set.) The refhi-sel bit when set specifies that the high reference voltage for the R2R ladder comes from the DAC with next higher index number, otherwise the high reference voltage is set to 5Vref. The reflo-sel bit when set specifies that the low reference voltage comes from the DAC with next lower index number, otherwise the low reference voltage is set to GNDref. When an adjacent DAC is used to source a reference voltage, its buffer amp must be turned on.

Analog Mux. The analog mux is designed to route one of 35 signals to the delta sigma modulator. A unity gain buffer amplifier may optionally be used at the input of the modulator. The analog mux is composed of a 32 to 1 mux which is controlled by AINSEL (5 bits, see command register discussion below) and a 4 to 1 mux which is controlled by DIVSEL (2 bits). The analog signals selected by AINSEL and DIVSEL are listed in table 4 below. Sixteen of the analog inputs are external to the chip, while 19 are internal to allow measurement of the DAC outputs, power supply voltages, and bias voltages generated on-chip. The ability to route internal signals to the delta sigma modulator allows much of the functionality of the chip to be verified by self-test and simplifies the chip test fixture design and test procedures, in addition to providing the accurate DAC mode described above.

External Thermistor Bias Resistor. One of the options configurable with a bit in the “mux” command register (see below) allows an external bias resistor to be connected to the delta sigma modulator input for use in sourcing current to off-chip instrument thermistors selected for measurement via the analog mux. In this way the same bias resistor may be used for all thermistors eliminating the need to match resistor values for each thermistor. The matching of temperature measurements from different thermistors is hence limited only by the matching of the thermistors themselves which is typically <0.1 degC. For EPI-Hi the delta sigma modulator will be used to accurately measure the temperature of thermistors mounted on the PHASICs (Pulse Height Analysis System Integrated Circuit) so that, if needed, temperature compensation can be applied to the PHASIC gains and offsets. In addition accurate temperature measurement of the PHASICs will be used to correct the temperature sensitivity of the PHASIC detector leakage current measurements with the goal (not requirement) of measuring sub nA currents.

Digital Outputs. Twelve outputs are provided that are designed to drive optocouplers for heater circuits, motors etc. The outputs can safely sink 20mA (TBR).

Power On Reset. The chip includes a power on reset circuit which uses an external capacitor to set the length of the reset interval.

Delta Sigma Modulator. The 1st order modulator is provided for precise DC measurement of the signal selected by the analog mux. The modulator can be operated in both "forward" and "reverse" modes by proper sequencing of the control signals generated by external (FPGA) logic. The forward and reverse modes are used together to reduce offset errors. In addition, the offset of the amplifier in the modulator can be trimmed to zero using 14 bits in the "mux" command register. Once trimmed, the modulator is capable of excellent linearity (errors of less than 10uV) for low source impedance signals over the entire voltage range from 20mV to ref5V-20mV. However, when the in-line buffer amplifier is used its offset voltage variation over the input voltage range limits the net linearity to the 8-bit level. Also, for unbuffered high impedance input signals the modulators input current can distort linearity. The input current is due to charge injection by the input switches and varies smoothly as a function of input voltage. (The input current versus input voltage curve will be added to future versions of this document.) For diagnostic purposes the output of the charge sensitive amplifier in the delta sigma modulator is delivered to an output pin via a low precision, high speed buffer amplifier which is powered off during normal operation.

Digital Interface

Digital Signal Levels. The chip is designed for interfacing with 3.3 to 5 Volt logic. The high state voltage level for chip outputs is equal to the voltage applied to the ioVdd pin. The threshold voltage for all chip inputs is set near 1.65 Volts. Internally, the chip's digital circuitry operates at 5 Volts.

Command Register. Information specifying programmable chip features is stored in two on-chip "mux" and "dac" command registers. The registers are loaded in parallel on the rising edge of the signal **cmd-strobe** from data in corresponding on-chip shift registers. Data are loaded serially into these shift registers via the **cmd-data-in** and the **muxclk** and **dacclk** inputs. Inputting and shifting of data for the "mux" command register occurs on the positive edge of **muxclk**, while for the "dac" command register the positive edge of **dacclk** is used. The power on reset generated by the HKchip is used on chip to clear the contents of both command registers.

The ordering of bits along the "mux" command register is specified in Table 2 below. The listed order is the reverse of the time order in which bits need to be input. For the "dac" command register the bit ordering is specified in Table 3.

Delta Sigma Modulator Operation. (to be added)

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Table 2: Mux Command Register Bit Assignments

Description	FORTH bit names	# of bits
analog input select	AINSEL0..4	5
modulator input buf bypass	MUXOUTSEL	1
modulator input buf amp enable	BUFAMPON	1
thermistor resistor enable	TRESSEL	1
modulator buf amp enable	BUFON	1
divider voltage select	DIVSEL0,1	2
forward select	FORWARD	1
digital output control bits	BOUT0..11	12
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		24 total

Table 3: Dac Command Register Bit Assignments

Description	FORTH bit names	# of bits
DAC 11 control bits	DACVAL(11)0..13	14
DAC 10 control bits	DACVAL(10)0..13	14
DAC 9 control bits	DACVAL(9) 0..13	14
DAC 8 control bits	DACVAL(8) 0..13	14
DAC 7 control bits	DACVAL(7) 0..13	14
DAC 6 control bits	DACVAL(6) 0..13	14
DAC 5 control bits	DACVAL(5) 0..13	14
DAC 4 control bits	DACVAL(4) 0..13	14
DAC 3 control bits	DACVAL(3) 0..13	14
DAC 2 control bits	DACVAL(2) 0..13	14
DAC 1 control bits	DACVAL(1) 0..13	14
DAC 0 control bits	DACVAL(0) 0..13	14
trim DAC setting	trimdac0..13	14
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		182 total

Table 4: Mux Selections

Analog input	AINSEL value	DIVSEL value
External input ain0	0	don’t care
External input ain1	1	don’t care
External input ain2	2	don’t care
External input ain3	3	don’t care
External input ain4	4	don’t care
External input ain5	5	don’t care
External input ain6	6	don’t care
External input ain7	7	don’t care
External input ain8	8	don’t care
External input ain9	9	don’t care
External input ain10	10	don’t care
External input ain11	11	don’t care
External input ain12	12	don’t care
External input ain13	13	don’t care
External input ain14	14	don’t care

External input ain15	15	don't care
DAC0 output	16	don't care
DAC1 output	17	don't care
DAC2 output	18	don't care
DAC3 output	19	don't care
DAC4 output	20	don't care
DAC5 output	21	don't care
DAC6 output	22	don't care
DAC7 output	23	don't care
DAC8 output	24	don't care
DAC9 output	25	don't care
DAC10 output	26	don't care
DAC11 output	27	don't care
v2p5 (nominally 2.5V)	28	don't care
vn1a bias voltage	29	don't care
vn1 bias voltage	30	don't care
5Vref (divided by 2)	31	0
a5V (divided by 2)	31	1
d5V (divided by 2)	31	2
ioVdd (divided by 2)	31	3

Functional Pin Description

The packaged device pin assignments are shown in Figure 2. The pins are arranged to allow separation of the digital and analog sections on the printed circuit board. Detailed pin descriptions are in Table 5.

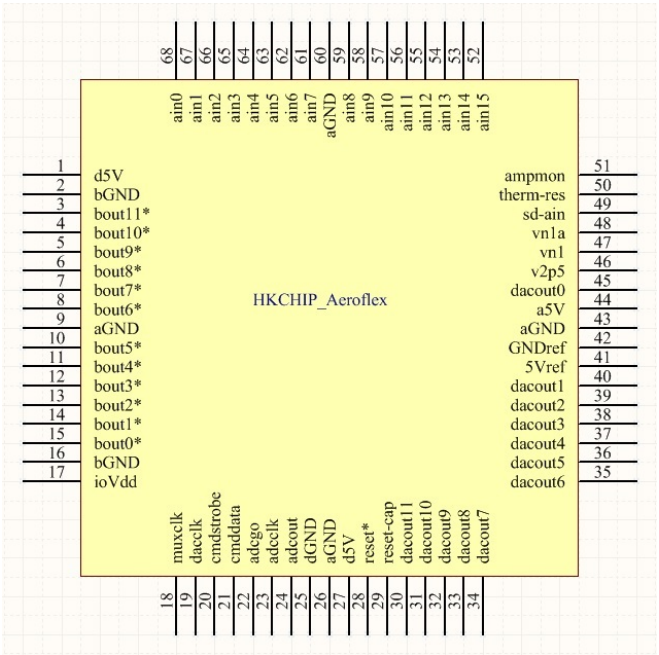

Figure 2. Package Pin Assignments

Table 5: Detailed Pin Descriptions

1.	**d5V**	digital 5V power. Attach a low pass filter composed of a 10ohm series resistor with parallel 0.1uF and 10uF tantalum bypass capacitors to dGND.
2.	**bGND**	separate GND return for the 12 digital output drivers.
3.	**bout11***	digital output from on chip driver. Max current sink 20mA.
4.	**bout10***	digital output from on chip driver. Max current sink 20mA.
5.	**bout9***	digital output from on chip driver. Max current sink 20mA.
6.	**bout8***	digital output from on chip driver. Max current sink 20mA.
7.	**bout7***	digital output from on chip driver. Max current sink 20mA.
8.	**bout6***	digital output from on chip driver. Max current sink 20mA.
9.	**aGND**	analog ground, connected to chip substrate.
10.	**bout5***	digital output from on chip driver. Max current sink 20mA.
11.	**bout4***	digital output from on chip driver. Max current sink 20mA.
12.	**bout3***	digital output from on chip driver. Max current sink 20mA.
13.	**bout2***	digital output from on chip driver. Max current sink 20mA.
14.	**bout1***	digital output from on chip driver. Max current sink 20mA.
15.	**bout0***	digital output from on chip driver. Max current sink 20mA.
16.	**bGND**	separate GND return for the 12 digital output drivers.
17.	**ioVdd**	digital I/O voltage. Attach a low pass filter composed of a series 10ohm resistor with parallel 0.1uF ceramic and 10uF tantalum bypass capacitors to ground. Place the ceramic capacitor close to the package pad. Connect to either 3.3V or 5V power supply compatible with controlling FPGA I/O.
18.	**muxclk**	digital input. Clock for on-chip 'mux' command register.
19.	**dacclk**	digital input. Clock for on-chip 'dac' command register.
20.	**cmdstrobe**	digital input. Synchronous update of command register outputs.
21.	**cmddata**	digital input. Command register data input.
22.	**adcgo**	digital input. Sigma-Delta Modulator initiate control signal.
23.	**adcclk**	digital input. Sigma-Delta Modulator clock.
24.	**adcout**	digital output. Sigma-Delta Modulator output to controlling FPGA.
25.	**dGND**	digital ground. Connect to ground.
26.	**aGND**	analog ground, connected to chip substrate.
27.	**d5V**	digital 5V power. Attach a low pass filter composed of a 10ohm series resistor with parallel 0.1uF and 10uF tantalum bypass capacitors to dGND.
28.	**reset***	digital output. Power-On-Reset for use external to hkchip.
29.	**reset-cap**	reference input. Connect to external capacitor to set length of reset* signal.
30.	**dacout11**	analog output. Output from on-chip dac.
31.	**dacout10**	analog output. Output from on-chip dac.
32.	**dacout9**	analog output. Output from on-chip dac.
33.	**dacout8**	analog output. Output from on-chip dac.
34.	**dacout7**	analog output. Output from on-chip dac.
35.	**dacout6**	analog output. Output from on-chip dac.
36.	**dacout5**	analog output. Output from on-chip dac.
37.	**dacout4**	analog output. Output from on-chip dac.
38.	**dacout3**	analog output. Output from on-chip dac.
39.	**dacout2**	analog output. Output from on-chip dac.
40.	**dacout1**	analog output. Output from on-chip dac.
41.	**5Vref**	analog input. Reference voltage.
42.	**GNDref**	reference input. Low reference voltage used by the dacs. Connect to aGND.
43.	**aGND**	analog ground, connected to chip substrate.
44.	**a5V**	analog 5V power. Attach a low pass filter composed of a 2ohm series resistor with parallel 0.1uF and 50uF tantalum bypass capacitors(tau=100usec) to aGND.
45.	**dacout0**	analog output. Output from on-chip dac.
46.	**v2p5**	2.5V reference voltage generated on chip. Bypass with 10nF ceramic capacitor to aGND.
47.	**vn1**	bias voltage generated on-chip. Bypass with 10nF ceramic capacitor to aGND.

48.	**vn1a**	bias voltage generated on-chip. Bypass with 10nF ceramic capacitor to aGND.
49.	**sd-ain**	analog input. External input to on-chip Sigma-Delta ADC.
50.	**therm-res**	external bias resistor connection. Use for thermistor measurements.
51.	**ampmon**	analog output. Monitor for modulator amplifier output.
52.	**ain15**	analog input. Connected to on-chip multiplexor.
53.	**ain14**	analog input. Connected to on-chip multiplexor.
54.	**ain13**	analog input. Connected to on-chip multiplexor.
55.	**ain12**	analog input. Connected to on-chip multiplexor.
56.	**ain11**	analog input. Connected to on-chip multiplexor.
57.	**ain10**	analog input. Connected to on-chip multiplexor.
58.	**ain9**	analog input. Connected to on-chip multiplexor.
59.	**ain8**	analog input. Connected to on-chip multiplexor.
60.	**aGND**	analog ground, connected to chip substrate.
61.	**ain7**	analog input. Connected to on-chip multiplexor.
62.	**ain6**	analog input. Connected to on-chip multiplexor.
63.	**ain5**	analog input. Connected to on-chip multiplexor.
64.	**ain4**	analog input. Connected to on-chip multiplexor.
65.	**ain3**	analog input. Connected to on-chip multiplexor.
66.	**ain2**	analog input. Connected to on-chip multiplexor.
67.	**ain1**	analog input. Connected to on-chip multiplexor.
68.	**ain0**	analog input. Connected to on-chip multiplexor.

Packaging

The chip is packaged in a hermetically sealed 64-pin ceramic quadflat package (NTK_IFK68F1-2179A-OP) The package dimensions are shown in Figure 3.

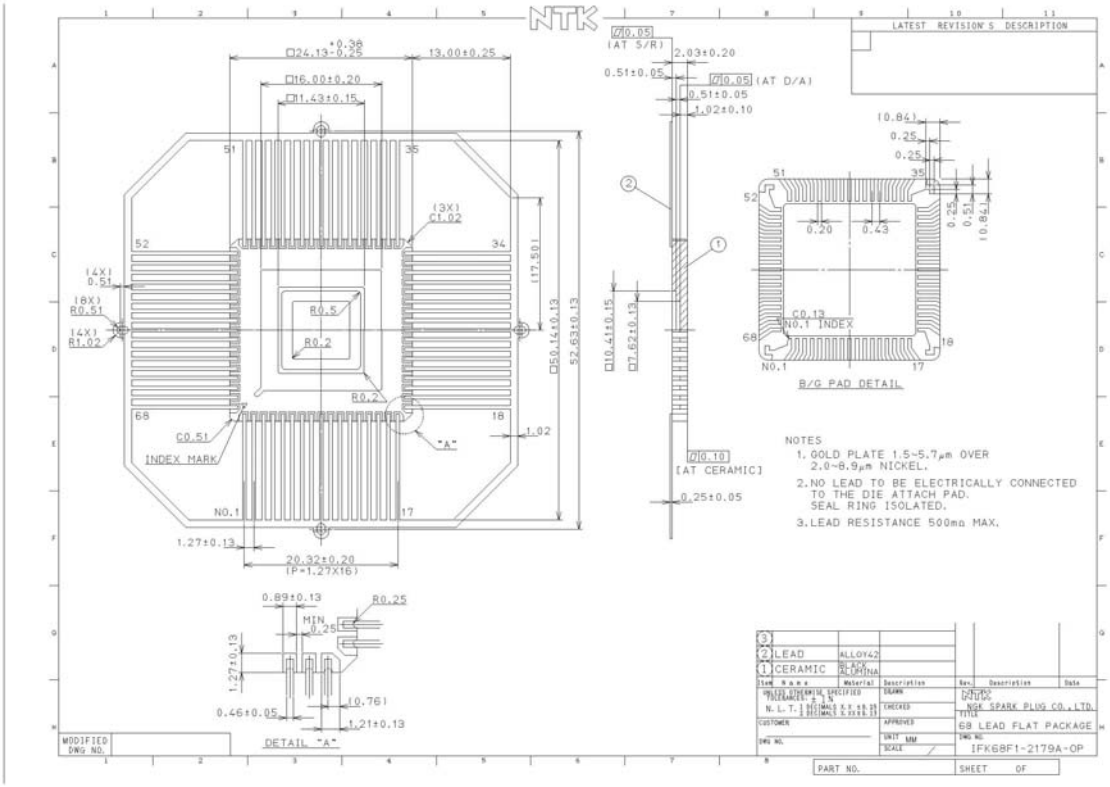

Figure 3. Package Dimensions