FPGA design margins

- For clock margin see telescope board discussion.
- MISC consumes 36% of RTAX 250 “R-cells” and 63% of “C-cells”, leaving 900 R-cells and 1050 C-cells available for application specific use.
- DPU board FPGA designs are (hopefully) complete.
- Application specific logic consumes: 730 R-cells (81% of available) and 860 C-cells (82% of available)
- Remaining available: 170 R-cells, 190 C-cells.
- (Should show more margin by CDR)