Solar Probe PHASIC User's Manual

WRC 11/29/12

This document provides information on the use of the Solar Probe PHASIC (Pulse-Height Analysis System Integrated Circuit) to pulse height analyze signals from the various silicon detectors contained in the EPI-HI instrument of the NASA's Solar Probe mission spacecraft.

Document Version History

The Solar Probe PHASIC design represents a modification of the design of the STEREO PHASIC and this document is a modification of the STEREO PHASIC User's Manual, whose document history is summarized in the next paragraph.

The (9/21/01) version of this document was published after most of the circuit design and after about one week of layout. It differs from earlier versions: 1) chip and hybrid pinouts are updated (still preliminary), 2) leakage current balancing capability at preamp inputs is described, 3) high/low gain ratio is 20 rather than 16, and 4) new read-reset, and rndn-gor-1,2,3 signals are described. The 10/22/01 version differs in the replacement of obsolete signals vleak and voffset with rGND and vthresh in the hyrid pin definition table and in adding preGND to the same table. For the 10/23/01 version the preGND pins were moved on the hybrid to avoid using aGND pins that were already committed in the package design. The 11/21/01 version incorporates some text corrections relating to the rndn-gor-0,1,2 signals. The read-reset signal has moved from the left to the right side of the chip. The 3/1/02 version follows layout completion and includes: new bond pad assignments, and complete command register specification. The 12/18/02 version has the pinout for the new hybrid package, corrected power supply current for -5Vref, radiation tolerance spec lowered from 20 krad to 12 krad (reflecting preliminary total dose test results), some modification of the data readout discussion, figures included electronically, and has been re-edited.

The first version of the document for the Solar Probe PHASIC is dated 11/29/12.

Chip Overview

The Solar Probe PHASIC (hereafter, "the chip") is a custom-designed CMOS VLSI circuit containing 16 nearly complete pulse height analyzer chains (PHA0-15). Each chain contains a preamplifier that is configurable for different detector capacitance and signal ranges. Each preamplifier output signal is coupled to two shaping amplifier/offset-gate/peak-detector/Wilkinson-ADC chains that operate in parallel, but with gains that differ by a factor of 68 (or 40). This dual-gain system achieves a wide dynamic range of up to 23000 from self-triggering threshold to full scale. The signal shaping is bipolar with time to peak near 1.9 usec. The primary shaping time constant is 1.2 usec. A block diagram of one dual-gain PHA is shown in Figure 1. The system is designed for positive polarity input signals. The PHA architecture, characterized by a "normally open" linear gate and lack of signal delay elements, has been used in numerous energetic particle instruments over the past 40 years.

Each dual-gain PHA chain is separately powered (on or off) under the control of a serially loaded on-chip command register. The power consumption is about 11 mW per active dual-gain PHA chain. On-chip digital circuitry provides control of the PHAs and sparse readout of the ADC data over a parallel buss. Two 23 bit scalars are included for each dual-gain PHA for independent monitoring of the high and low gain section trigger rates.

A precision test pulser for each dual-gain PHA chain may be used for functional test and calibration. An on-chip analog multiplexor and precision unity gain buffer amplifier allows DC and

AC monitoring of selected on-chip test points. A separate higher bandwidth unity gain buffer is provided for monitoring preamplifier output DC and transient response. A 10 bit programmable resistance to ground at each preamplifier input allows leakage current balancing when DC coupling to the signal source.

For Solar Probe applications the chip and supporting passive components are mounted on a ceramic substrate and installed in a standard 80 pin covar package to form a “PHASIC” hybrid.

The chip is designed for fabrication using ON Semiconductor’s 0.5 um CMOS process (C5) incorporating high density linear capacitors and high value resistors suitable for mixed-signal designs. To achieve >100 krad total dose tolerance for flight the chip will be fabricated with proprietary radiation hardening steps provided by Aeroflex Corporation.

The layout of the chip makes use of guard rings intended to raise the threshold for single event latchup to a high enough level to make latchup protection circuitry unecessary. Similar guard rings were used in the layout of the STEREO PHASIC, for which latch-up testing at the Berkeley Cyclotron, found no latch-up up to an L.E.T. of 80 MeV/(mg/cm2). Preliminary sepcifications are listed in Table 1.

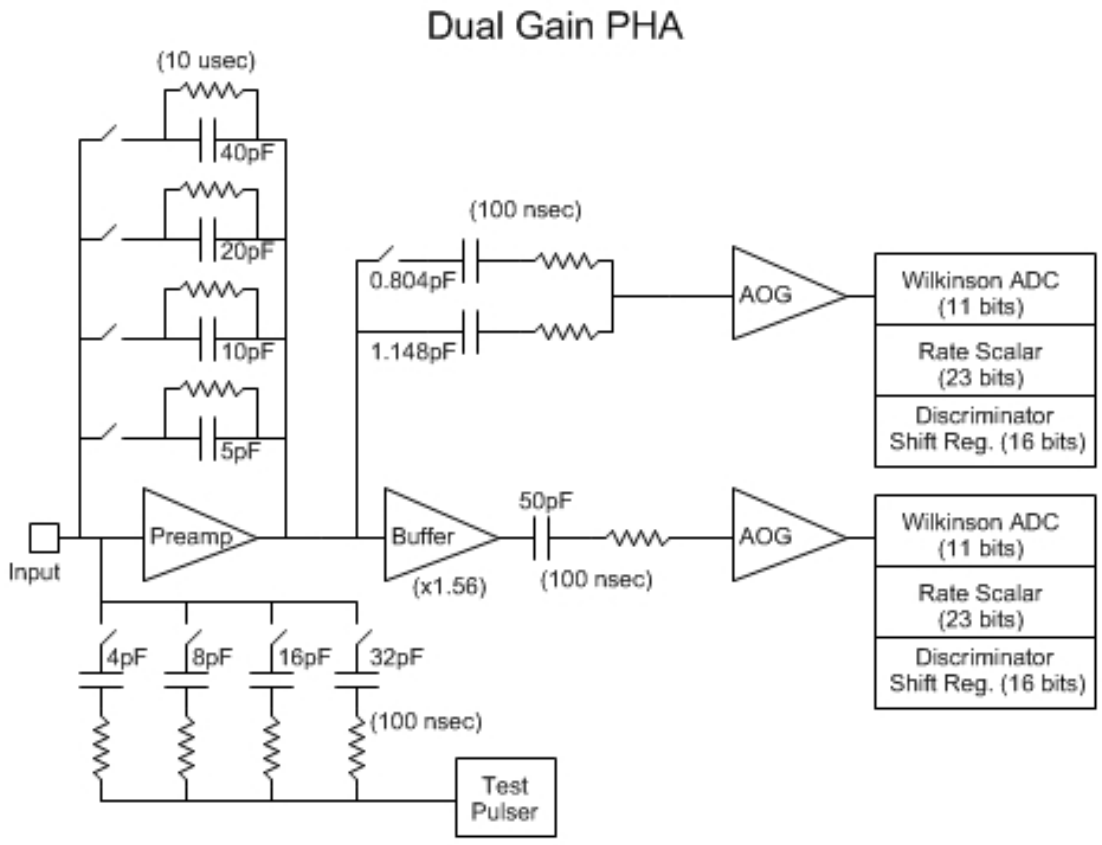

Figure 1. (Programmable input resistance not shown.)

Table 1. PHA Chip Specifications

Number of dual-gain PHAs	16
Chip size	7.4 mm by 7.4 mm
Power	11 mW per active PHA
Dynamic range	Up to 23000 (F.S./trig. thresh)
Integral non-linearity	<0.05% of F.S.
Differential non-linearity	<1%
High/Low gain ratio	68 or 40, configurable
ADC type	Wilkinson
ADC resolution (both gains)	11 bits, 12th bit overflow
Shaping	Bipolar, 1.9 usec to peak
Preamp feedback cap.	5-75 pF, programmable in 5 pF steps
Preamp full scale output swing	4.0 Volts
Cross-talk between adj. PHAs	<0.2%
Radiation Tolerance	>100 Krad, no latchup below 80 MeV/(mg/cm2)
Gain temp. coef.	<50 ppm/deg. C
Offset temp. coef.	<0.1 channel/deg. C
Operating temp. range	-30 to +50 deg. C
Leakage current balancing	up to 32 uA with 10 bit resolution
Threshold programmability	up to 6% of F.S. (each gain) with 10 bit resolution

PHA Design and Operation

Power Supply Requirements. The chip operates with power supply voltages: analog and preamp 5V, reference -5V, digital 5V, and interface 5 or 3.3 Volts. The analog 5V and preamp 5V supply currents are approximately 1.8 mA and 0.4 mA, respectively, times the number of powered PHAs. The reference -5V current is approximately 1.1 mA. The PHA gains are proportional to the actual voltage of the reference -5V supply, which therefore should be maintained stable over temperature and time. (Only a single 5V supply line is bought into the PHASIC hybrid, where separate power supply bypass networks distribute power to analog and preamp 5V.)

Preamplifier. The preamplifier is configurable for different input signal ranges via programmable feedback capacitance as illustrated in Figure 1. Any combination of 40, 20, 10 and 5 pF capacitances may be enabled (by setting PHA command bits **fbsel3**, **fbsel2**, **fbsel1**, and **fbsel0** respectively) to achieve net feedback capacitance in the range 5 to 75 pF. Parallel feedback resistances of 250K, 500K, 1M and 2M provide a fixed 10 usec feedback network time constant, independent of capacitance selection.

The preamplifier compensation capacitance is configurable to allow stable linear operation for various detector capacitance and signal ranges. The command bits **compsel1** and **compsel0** allow setting the feedback capacitance to 5, 10, 15 or 20 pF.

Table 2: Preamplifier Compensation Capacitance

compsel0	compsel1	pF
0	0	5
1	0	10
0	1	15
1	1	20

Additional control of the loop gain is achieved using external components as illustrated in Figure 2. In some configurations, external components limit the preamplifier slew rate to maintain good response linearity.

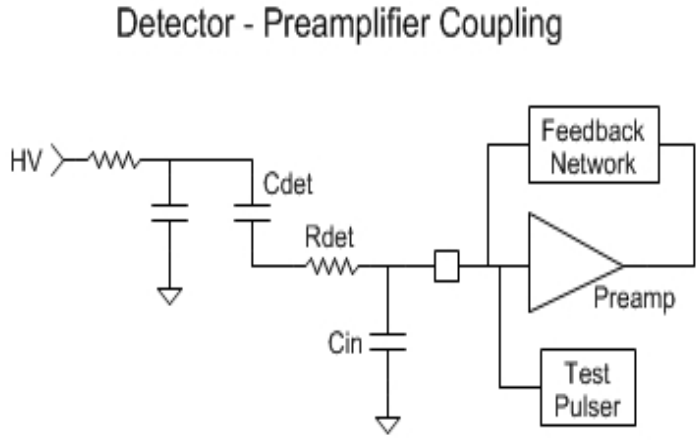

Figure 2. (Programmable input resistance not shown.)

Preamplifier outputs may be monitored one at a time at the **preout** output pin. (See discussion of diagnostics, below.) A 10 bit programmable resistance to ground is provided at the input of each preamplifier to allow leakage current balancing in DC coupled applications. The maximum leakage current that can be handled is approximately 32 uA. To achieve the full rated dynamic range (for low gain) it will generally be necessary to periodically monitor the preamplifier output DC levels and adjust the programmable input resistances to maintain the level at 4.6 Volts.

Table 3: Typical Preamp Configurations for EPI-HI

Det	Cdet (pF)	Rdet (ohm)	Cin (pF)	Nf	Threshold (MeV)	Full Scale (MeV)	Zn @ 45 (deg)	Freq(G.C.) (MHz)	Phase Margin (deg)
L0	**208**	**0**	**30**	**1**	**0.09**	**268**	**83**	**12.3**	**98**
L1	**93**	**30**	**40**	**1**	**0.05**	**268**	**251**	**13.3**	**65**
L2(H1)	**20**	**10000**	**60**	**6**	**0.12**	**2802**	**2660**	**13.4**	**60**
L3(H2)	**40**	**7500**	**80**	**9**	**0.19**	**4337**	**4092**	**10.8**	**61**
H3	**30**	**15000**	**80**	**13**	**0.28**	**6155**	**6203**	**10.5**	**56**

Table 3 lists values of the feedback capacitance (= Nf x 5pF), and external components suitable for the various detectors of the EPI-HI instrument, along with the lowest threshold compatible with

noise simulations. The full scale energy is compared to the maximum energy deposited by stopping Zinc nuclei at 45 degree incidence angle. Frequency of gain crossover and phase margin are also listed.

The loop gain and phase are plotted versus frequency in Figure 3 for the EPI-HI LET L2 detector configuration, illustrating the features typical for all configurations: unity gain crossover near 13 MHz with phase margin near 60 degrees and steep rise in gain below 2 MHz. This steep rise yields gain of greater than 10,000 near the 120 KHz center of the bandpass of the shaping amplifiers and filters that precede the peak detector. (The loop gain and phase of the shaping amplifiers and peak detector amplifier also are tailored to be similar to those shown in Figure 3).

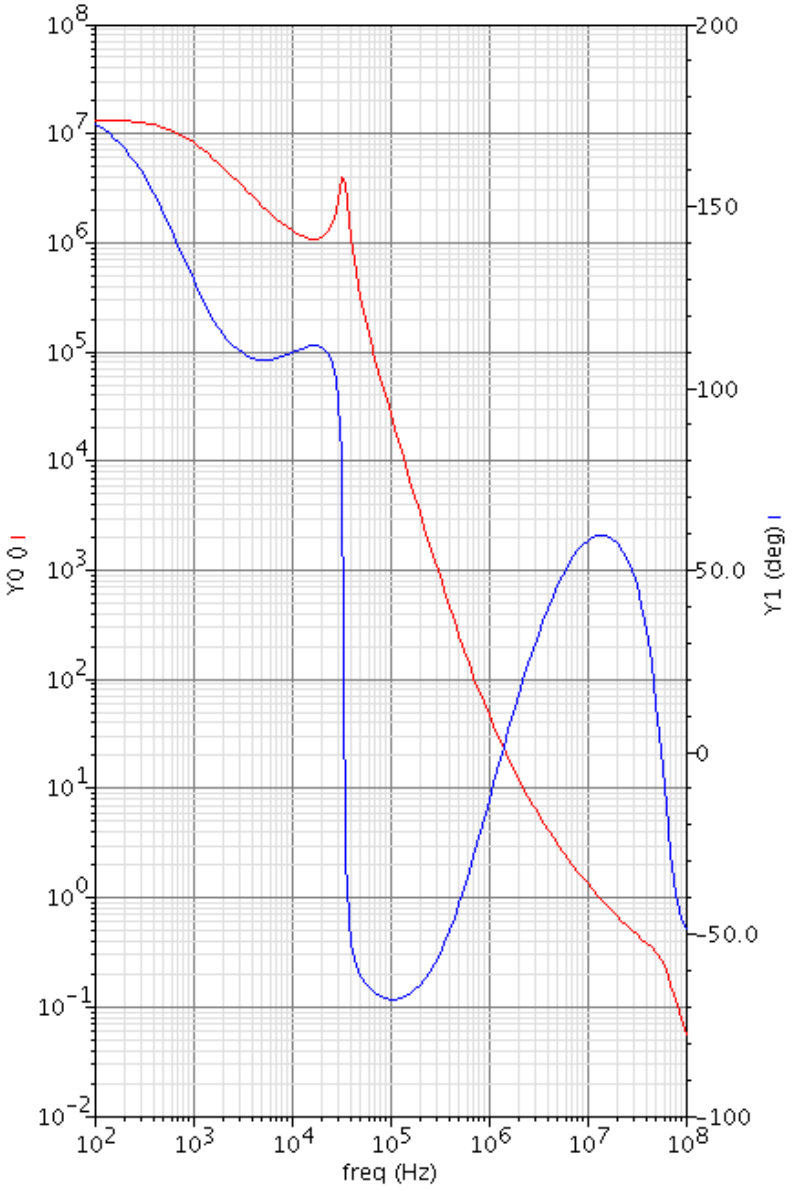

Figure 3.

The resonance peak in the gain plot is due to internal positive feedback within the preamplifier which boosts gain near 120 kHz, but has only a minor impact near gain crossover.

The source connection of each preamplifier's input PMOS FET is brought out to a separate pin. These signals are referred to as pre5V(i) and may be treated as separate low noise signal references. They may be tied to a common well-bypassed 5V node (as done in the PHASIC hybrid) or separately bypassed.

The preamp design was improved from the STEREO to Solar Probe PHASIC versions by increasing the linear range of the preamp's output voltage swing from 2.7 to 4 Volts. This was accomplished by replacing the voltage follower output stage with an open drain "rail to rail" type output. This type of output has inherently high impedance which was OK for driving the low gain signal chain but not the high gain one and this required the addition of a buffer amplifier to the beginning of the high gain chain. See "**Changes From STEREO PHASIC**" below for more details.

Amplifier/Offset/Gate. Each preamplifier's output is coupled to two separate linear pulse processing/ADC chains that operate in parallel. The overall gain difference between the two chains is configurable to either a factor of 68 or 40 corresponding respectively to settings of 1 and 0 for the **lgainsel** command bit (which adjusts the gain of the low gain channel by a factor of two).

The low and high gain signal chains are identical except for the presence of an additional amplifier at the beginning of the high gain chain and except for the values of passive components which couple the preamp signal to the two signal chains. The identical portion of each signal chain is illustrated in Figure 4. The second shaping amplifier stage shown in Figure 4 translates the signal from voltage to current mode representation. Signal current in excess of the threshold imposed by a programmable current source is directed to the output of the offset gate and flows across a load resistor for regeneration of the signal voltage. An amplifier then boosts the signal amplitude by a factor of 2 prior to input to the peak detector. The offset gate is "normally open" in the sense that any signal current in excess of the offset is automatically passed. However, after peak detection the gate is closed by on-chip logic, preventing contamination of the analog to digital conversion process by subsequent pulses.

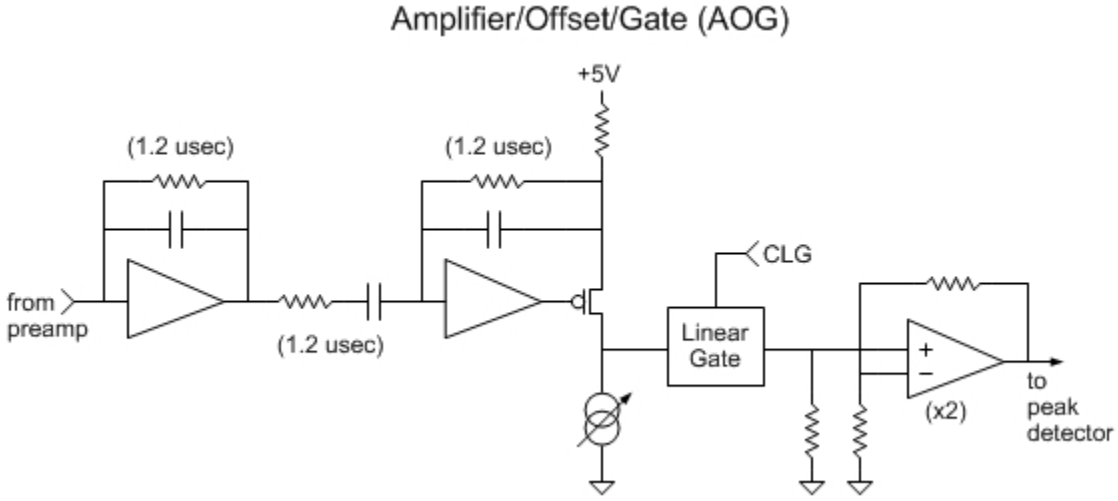

Figure 4.

The offset gate can operate in two modes depending on the size of the programmable offset current relative to the 5 uA standing current in the output FET of the second stage amplifier

shown in Figure 4. The normal "narrow range" mode of operation occurs when the programmable offset current source is set to exceed 5 uA by an amount sufficient to block the passage of front-end thermal noise to the peak detector. In this mode there is no DC output current from the offset gate and the baseline voltage at the peak detector input is independent of the programmable offset current setting. The "wide range" mode occurs when the programmable offset current is set below 5 uA allowing the offset gate to pass front-end thermal noise to the peak detector. In this mode DC current does flow from the offset gate output and the baseline voltage at the peak detector input is a function of the programmable offset current. In most cases the front-end thermal noise will be sufficient to cause continuous triggering of the peak detector, in which case this mode is only useful for diagnostic tests.

The programmability of the offset current sources (16 for low gain, 16 for high gain) is from 2.5 to 12.5 uA, with 10 bit resolution. Since full scale signal current is near 125 uA, the maximum threshold setting corresponds to (12.5uA-5uA)/125uA or 6% of the high or low gain full scale signal. The threshold setting resolution corresponds to about 1/8 of an ADC count. This fine resolution allows precise (<3%) threshold control even at the lowest practical threshold settings.

Wilkinson ADC. The shaped and thresholded signal from the AOG is input to a peak detect and hold circuit as illustrated in Figure 5. During the rising portion of an input pulse the peak detector amplifier charges the "hold" capacitor, causing its voltage to closely track the input. The charging current is mirrored and flows across a load resistor at the input to a discriminator. The net gain from peak detector input to discriminator input is quite large, so that the discriminator can be fired by an input pulse of only 2.5 mV peak amplitude.

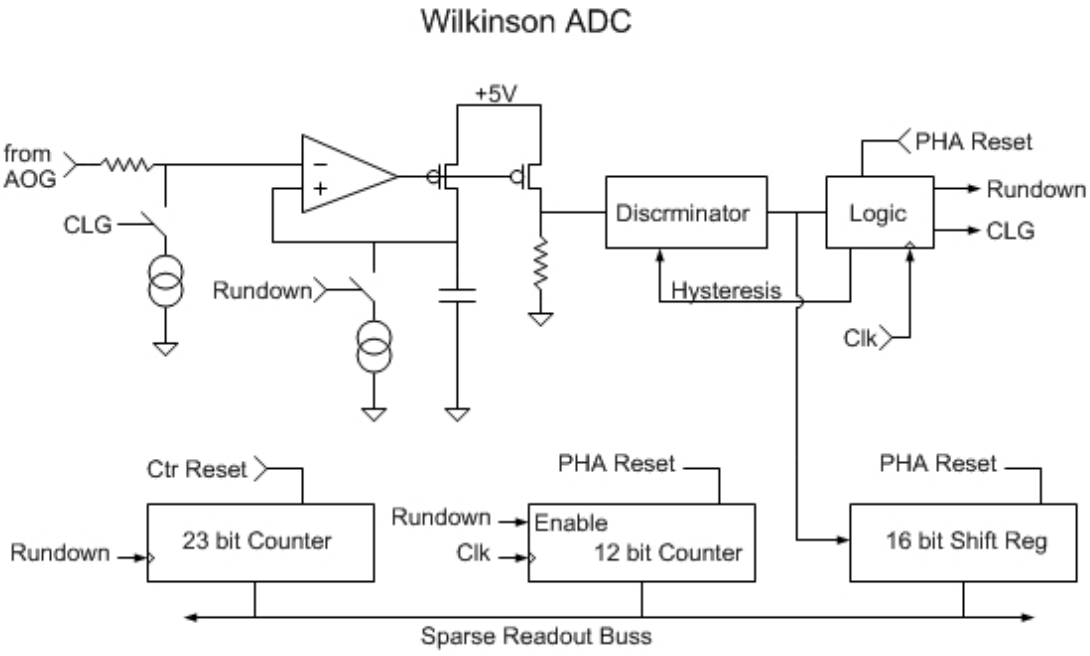

Figure 5

The signal presented to the discriminator is proportional to the time derivative of the input signal, such that the discriminator fires at least 0.5 usec prior to the input signal peak time. The discriminator firing sets a "trigger latch" that establishes hysteresis for the discriminator, shifting the threshold so that the discriminator will "un-fire" when the hold capacitor charging current drops to zero near the time of the input signal peak. This un-firing of the discriminator constitutes peak detection and initiates the **rundown** interval synchronously with the next positive edge of the system clock. During the **rundown** interval, a current source is turned on to ramp down the hold capacitor voltage at a precisely constant rate. Peak detector and linear ramp operation are

illustrated in Figures 6 and 7 which show the peak detector input and hold capacitor voltage waveforms for full-scale and near-threshold pulses respectively.

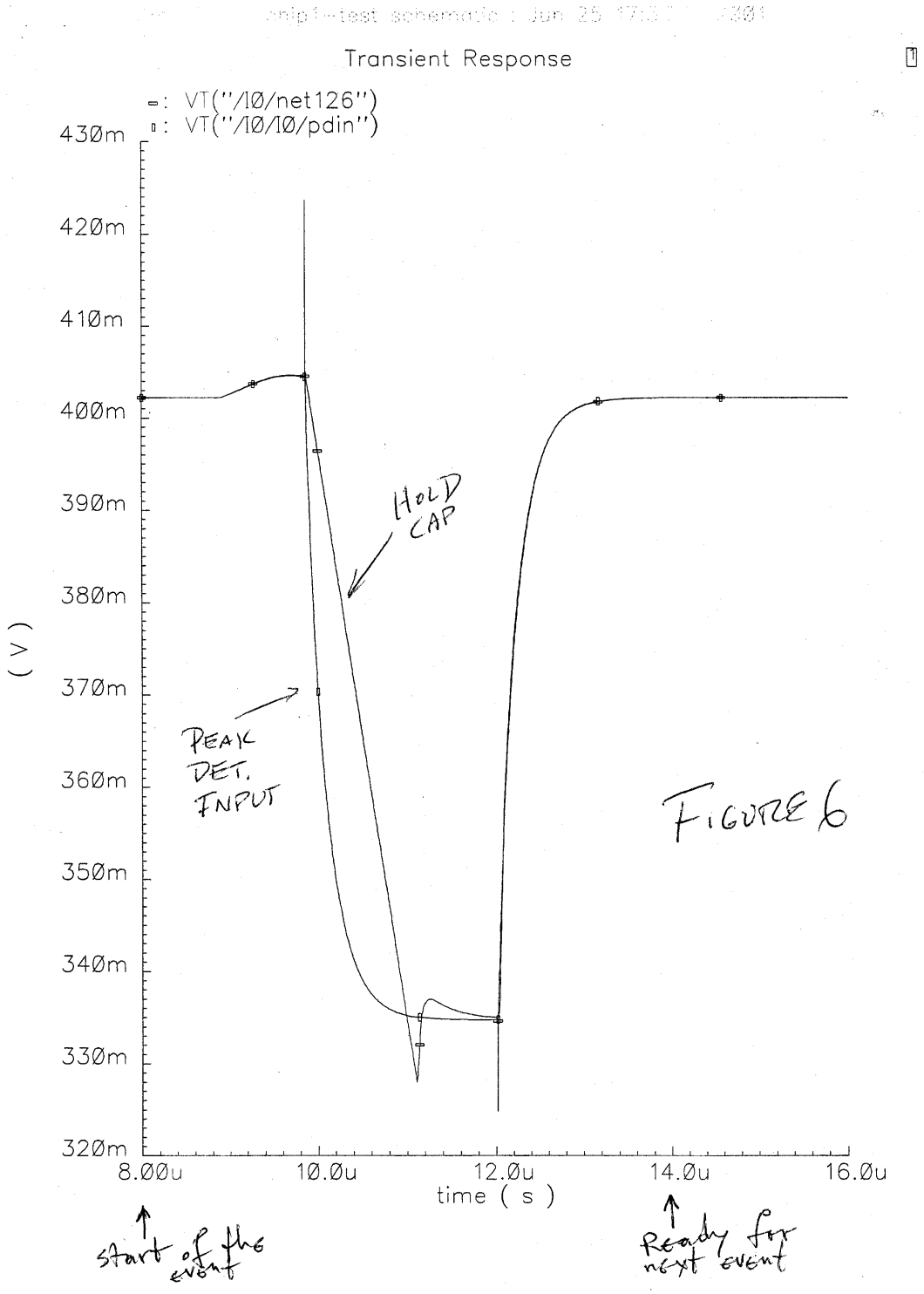

Figure 6.

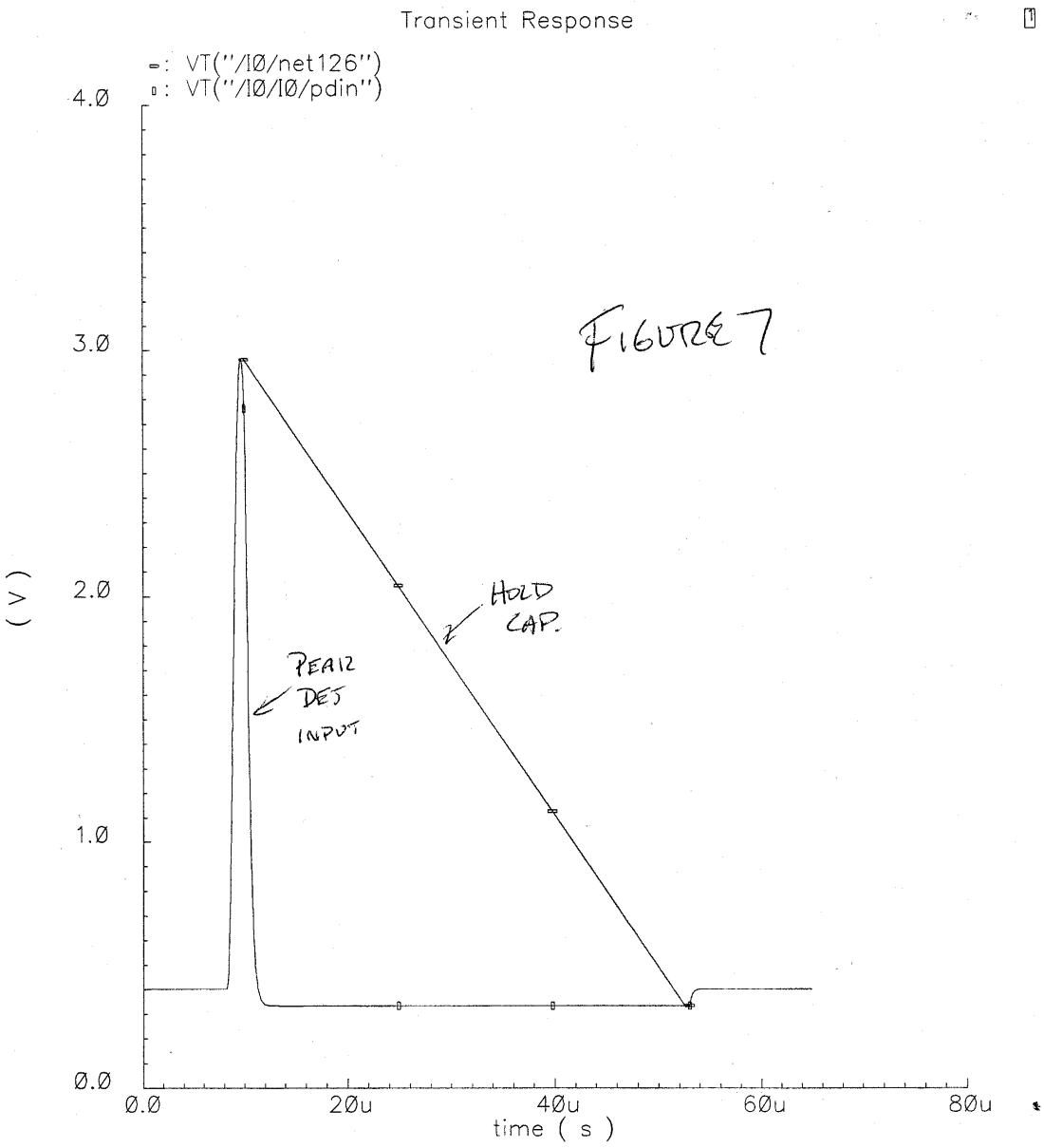
Transient Response
=: VT("/10/net126")
▯: VT("/10/10/pdin")
4.0
3.0
2.0
1.0
0.0
(V)
0.0
20u
40u
60u
80u
time (s)
FIGURE 7
HOLD CAP.
PEAK DET INPUT

Figure 7

Following peak detection the input signal drops below the stored voltage on the hold capacitor opening the feedback loop around the peak detector amplifier and turning off all charging current. The hold capacitor voltage then remains nearly constant (discharged only slowly by a 1.4 uA current source, not shown, that sets the standing bias of the output FET) prior to the initiation of the **rundown** interval. Whenever the peak detector amplifier loop is open the diagnostic signal **lop** goes high. The logical OR of all **lop** signals from active PHAs is an output signal from the chip named **lop-or**.

Coincident with the initiation of the **rundown** interval the local (per ADC) on-chip logic closes the linear gate, causing the voltage at the input of the peak detector to rapidly drop to the baseline. Simultaneously, a current source at the input of the peak detector turns on to shift the baseline downward a precise amount, introducing a reproducible pedestal count for all ADC conversions.

When the hold capacitor voltage has ramped down to the shifted baseline level, the amplifier loop re-closes and the current in the output FET rises rapidly from zero to equal the **rundown** current value. This sharp rise in output current re-triggers the discriminator, marking the end of the **rundown** interval. The use of the peak detector amplifier to sense the return of the hold capacitor voltage to the shifted baseline value virtually eliminates any transfer function dependence on the DC offsets of the peak detector and 2x amplifiers. This enhances stability of the transfer function offset, which is determined by the threshold setting (in narrow range mode) and fixed pedestal.

During the **rundown** interval, a 12 bit counter is enabled to count at the system clock rate. The magnitude of the rundown current, the size of the rundown capacitor, and the frequency of the system clock provide a full scale count near 2048 = 2^11, such that the 12th bit of the counter serves for overflow detection. With the 32 MHz system clock planned for STEREO applications, the maximum conversion time is 2048/32 usec = 64 usec. The minimum conversion time is due to the pedestal (about 46 counts) and is approximately 1.4 usec.

The **rundown** interval is generated locally only for those ADCs which are triggered. The **rundown** signals from active PHAs are logically OR'ed together to form the **rndn-or** signal. The rundown signals from selected PHAs (chosen by command register bits) are OR'ed to form the three signals **rndn-gor-0,1,2**. A total of 32*3 = 96 command register bits are provided for this function, allowing any combination of the 32 rundown signals to contribute to each of the "gated or" (gor) signals.

The net PHA threshold results from the combined actions of the AOG and the peak detector discriminator. However, for the sake of performance and simplicity, the peak detector threshold is set at a fixed low value and all adjustment of the net threshold level is made via the programmable AOG offset current. Second, adjustment of the net threshold in this way alters the offset of the linear "signal in to pulse-height channel out" transfer function. The relationship between AOG offset current setting and transfer function offset is linear, stable, and predictable, and will be measured as part of the calibration of each flight PHASIC.

Pileup/crosstalk detection. Pileup and crosstalk can significantly alter the shape of the signal at the input to the peak detector and hence alter the timing of the leading edge firing of the discriminator and of the peak detection. So, to aid in identifying signals that have been contaminated by pileup or crosstalk, a 16 bit shift register in each low and high gain signal chain is configured to sample the discriminator output. During livetime and for about 0.5 usec after the system-wide closing of all linear gates via the **clg** signal (see **PHA Control** below) the shift registers are clocked at 4 MHz. When the clocking stops following **clg** the shift registers are frozen till readout and contain information about the prior 4 usec of discriminator activity. (These shift registers for monitoring the discriminator activity were added for the Solar Probe PHASIC based on experience with the use of the STEREO PHASICs. In that case low level crosstalk within the PHASIC, as well as crosstalk that occurred at the segmented detectors, presented a challenge that complicated the flight event analysis software, but otherwise was tractable. A study of the sources of the cross talk showed that the level of cross talk within the PHASIC was already

so low that further improvement could not be guaranteed and that, of course, cross talk occurring at the detectors could also not be improved by PHASIC design mod. However, simulation showed the very different discriminator timing signatures of the different types of cross talk and this led to the inclusion of the shift registers for the Solar Probe PHASIC design.)

Linearity, Stability and Channel Matching. Unlike for typical ASIC pulse height analysis systems, the PHASIC achieves excellent linearity and stability of the the transfer function that is more typical of traditional precision non-ASIC systems (see Table 1). This performance is due to several design features including: 1) the absence of non-linear elements (such as current mirrors) in the signal path, 2) the use of a precision external resistor to set the rundown current for each Wilkinson ADC, and 3) the use of high loop gain, large operating point margins, and avoidance slew rate limitation for all amplifiers in the signal path. Item 2, the use of off-chip precision resistors to set the rundown currents, causes the transfer function gains to depend (to first order) only on the ratio of on-chip resistor values, which is important since the on-chip resistors have a terrible temperature coefficient near 2000 ppm/degC, but good tracking over temperature. The transfer function gains do linearly depend on the value of capacitance per unit area for on-chip poly-oxide-poly2 capacitors, but that is acceptable since these capacitors have a low temperature coefficient of about 20 ppm/degC. The fact that the transfer function gains are to first order independent of the resistance per square of on-chip resistors not only allows the gains to be stable over temperature (<50 ppm/degC) but also allows for good matching of transfer function gains from channel to channel and PHASIC to PHASIC. Transfer function gains for the STEREO PHASICs were typically matched to approximately 1 percent and such good matching should also happen for the Solar Probe version. However, the STEREO version of the PHASIC did suffer from excessive channel to channel variation of the peak detector threshold and changes in the design of the peak detector for the Solar Probe version are intended to reduce this variation. (See "**Changes from STEREO PHASIC**".)

On-chip Diagnostics. An on-chip precision test-pulser accompanies each preamplifier as shown in Figures 1 and 2. Each test-pulser is enabled/disabled with a separate command register bit. If a test-pulser is enabled and the chip input **test-pulse** is high, then the test-pulser output is connected via a low-impedance high-speed analog switch to the chip input **testRef**. Otherwise the test-pulser output is connected by a similar analog switch to **testGND**. Thus, each enabled test-pulser produces a square-shaped pulse of amplitude (**testReF**-**testGND**) and duration equal to that of **test-pulse**. The output pulse of each test-pulser is coupled to the corresponding preamplifier input via a test RC network that is programmable over the range of capacitance from 0 to 60 pF in 4 pF steps. The RC time constant of the test network is fixed at 100 nsec, independent of capacitance selection. A capacitance selection of 0 pF is allowed to aid in cross-talk measurements by preventing unwanted coupling of **testGND** transients into un-stimulated preamplifiers. The range of programmability of the test-capacitance is chosen to allow its setting to 4/5 the value of the chosen feedback capacitance and the low gain ADCs to be pulsed to full scale using a (**testRef**-**testGND**) voltage of approximately 5 Volts.

One at a time, preamplifier outputs may be routed through an on-chip precision unity gain buffer to the chip output pad **preout.** Command register bits **presel0,1,2,3** select which preamp output is routed when bit **preout-en** set. When bit preout-en is cleared (the default operating condition) no preamp signal is routed. The bandwidth of the unity-gain buffer is sufficient to allow oscilloscope verification of proper preamp signal overshoot and lack of ringing. The DC level of preamp outputs may be monitored to facilitate leakage current balancing in DC coupled applications.

An on-chip precision unity-gain buffer amplifier driving the **scope-out** signal allows oscilloscope monitoring of selected test points via an on-chip analog multiplexor programmed by command register bits. The **scope-in** signal is routable to the buffer amplifier input to allow stimulation to verify its AC and DC performance. Internal chip test-point selection is yet to be documented.

The **preout** and **scope-out** buffer amplifiers are designed to drive 2-3 feet of 95 ohm coax attached to a typical 15 pF oscilloscope input, yet remain stable with no load. In systems where the preout signal is monitored for detector leakage current balancing, the transient performance at the preout node may be maintained by coupling the node to monitoring hardware (ADC or comparator input with filtering capacitance) via a resistance near 100 kohm.

Digital Interface

Digital Signal Levels. The chip is designed for interfacing with 3.3 or 5 Volt logic. The high state voltage level for chip outputs is equal to the voltage applied to the IO-VDD pin. The threshold voltage for all chip inputs is set near 1.65 Volts. Internally, the chip's digital circuitry operates at 5 Volts.

Command Register. Information specifying programmable chip features (signal thresholds, preamp feedback and test input capacitances, etc.) is stored in an on-chip command register. The register is loaded in parallel on the rising edge of the signal **cmd-strobe** from data in a corresponding on-chip shift register. Data are loaded serially into this shift register via the **cmd-data-in** and the **cmd-clk-in** inputs. Inputting and shifting of data occur on the positive edge of **cmd-clk-in**. The shift registers on multiple PHA chips can be daisy-chained by connecting the **cmd-data-in** to **cmd-data-out** and **cmd-clk-in** to **cmd-clk-out** on adjacent chips as shown in Figure 8. Note that the data propagates from left to right, while the shift clock propagates right to left. The **cmd-strobe** signal is distributed to all PHA chips. The daisy-chaining of readout control is also illustrated in Figure 8 and is discussed below.

The chip input **cmd-reset*** asynchronously clears all command register bits to zero. The **cmd-reset*** may be asserted low during power-up to ensure that all PHAs are initialized to the powered off state. Alternately the **cmd-reset*** signal may be tied permanently high, in which case the command state will be uncontrolled until serially loaded as described above.

The ordering of bits along the command register is specified in Table 4 below. The listed order is the reverse of the time order in which bits need to be input. For example, the **rndn-gor-2/enable-rndn0H** bit is loaded first while **scopesel7** is loaded last. Most command register flip-flops are imbedded within the 16 PHA core and these core-imbedded registers are organized into four categories (Test pulse/feedback through PHA control) defined both by function and layout geometry. The path of data flow through the core-imbedded portion of the command register chain is serpentine. Beginning in the upper left corner of the core layout (near the preamp for PHA0) data flows across the chip from left to right through the Test pulse/feedback registers, then travels right to left through the Input resistance registers, than left to right again through the Threshold settings, and finally right to left through the PHA control registers. The alternating forward and reverse ordering of the PHAs along the core-imbedded portion of the command register is indicated in the column labeled PHA#.

The total number of bits in the command register is the same for the Solar Probe and STEREO PHASIC versions. However, the three bits {**lgainsel, compsel1,0**} in the Solar Probe case, have different functions than the three bits {**rdegsel2,1,0**} in the earlier STEREO case.

Table 4: Command Register Bit Assignments

category	PHA#	bit names	# of bits
Scope-mux	n/a	scopesel7,...,0, scope-enable	9
Preout-mux	n/a	presel3,2,1,0, preout-enable	5
Test pulse/feedback	PHA0,...,15	test-enable, testsel3,2,1,0, fbsel3,2,1,0	9*16
Input resistance, etc.	PHA15,...,0	lgainsel,compsel1,0, indac9,...,0	13*16
Threshold setting	PHA0H,...,15L	ioff9,...,0	10*32
PHA control	PHA15,...,0	hg-adc-en, lg-adc-en, verbose, power-on	4*16
rndn-gor-0	n/a	enable-rndn15L,...,enable-rndn0H	32
rndn-gor-1	n/a	enable-rndn15L,...,enable-rndn0H	32
rndn-gor-2	n/a	enable-rndn15L,...,enable-rndn0H	32
		Total # of bits:	846

PHA Chip Daisy-Chain

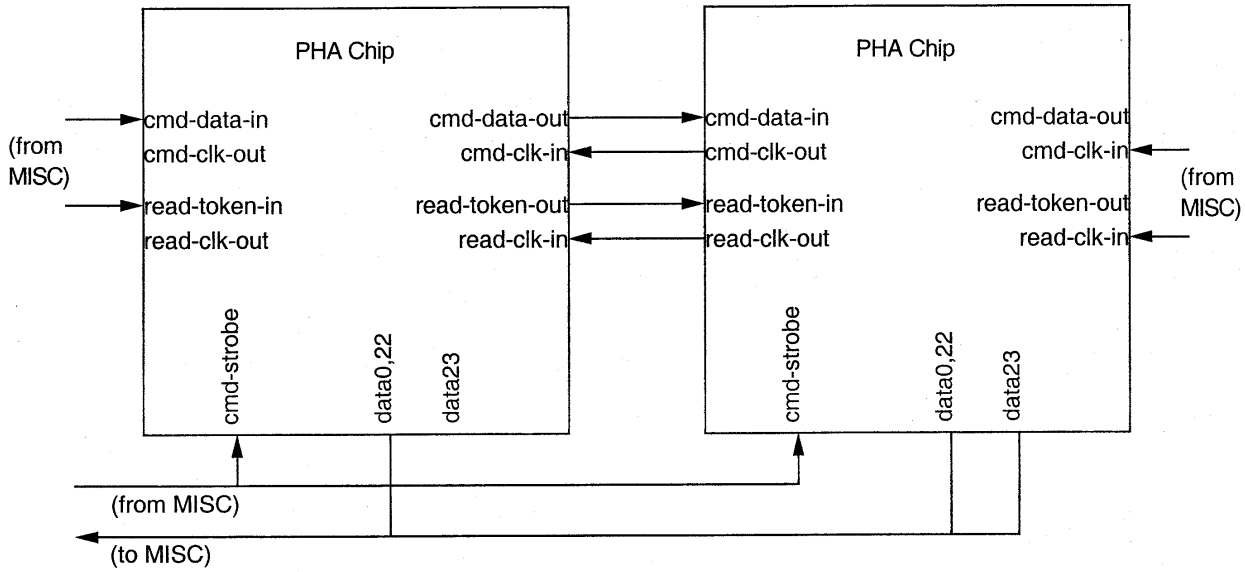

FIGURE 8

PHA Control. The pulse-height analyzer system interacts with off-chip system logic via chip outputs: **lop-or**, **rndn-or**, **rndn-gor-0**, **rndn-gor-1** and **rndn-gor-2**, and chip inputs: **clg** and **pha-reset**. In the quiescent state all these signals are inactive and the external system logic should be counting livetime and waiting for the appearance of **rndn-or** (or **lop-or**) which indicates that peak detection has occurred for at least one detector. The external logic should immediately stop counting livetime and begin timing a short "coincidence resolving" interval of length about 0.5 usec. At the end of that interval **clg** is asserted causing the closure of the linear gates of untriggered ADCs to block any subsequent signal pulses. (Linear gates for triggered ADCs are automatically closed by the per-ADC on-chip logic immediately following peak detection.) Following the assertion of **clg**, the external logic should wait for **rndn-or** to expire, at which time all analog to digital conversions are complete and pulse-height data are ready for readout as described below.

Readout of pulse height data is optional. The **rndn-gor-0,1,2** signals are provided to allow flexibility in deciding (off-chip) whether to readout pulse-height data. (Not only the presence of the **rndn-gor** signals, but also their durations contain preliminary information which may be used in deciding whether to readout data for a particular event.)

Following optional readout of pulse-height data, the external logic needs to simultaneously assert **pha-reset** and de-assert **clg**. After a 2 usec pause, **pha-reset** is de-asserted to re-enter the quiescent state and external livetime counting should resume.

Pulse-height Data Readout. Data are accessed from the chip over a 24-bit wide tri-state buss. A sparse readout scheme is used to minimize readout time. The readout process is controlled by the chip inputs: **read-reset, token-in**, **read-clk-in**, and **adc-read-sel**. Throughout the readout process **adc-read-sel** is held high to access pulse-height data, or low to access counter data. The read process is initiated by asserting **token-in** followed by **read-clk-in**. When **read-clk-in** is then taken low, a pulse-height data word (if available) is driven onto the 24-bit tri-state buss. The **token-in** signal is de-asserted for subsequent cycles of **read-clk-in**, each of which produces the readout of another pulse-height word. Following the positive edge of the **read-clk-in** associated with the last pulse-height available for readout, the chip output **token-out** goes high. If initially there are no pulse-height data available for readout (no triggers) then **token-out** goes high within 20 nsec of the initial low to high transition of **token-in**. The pulse-height word includes (in order from least to most significant): an 11-bit pulse-height, an overflow bit, two reserved bits, a low/high gain bit, a 4-bit PHA address, a 4-bit "chip address" and a bit reflecting the state of the **token-out** signal, for a total of 24 bits. After readout of the last pha data word,the **read-reset** signal should be pulsed high to reset the tri-state data buss lines to a low state. (The **read-reset** signal also needs to be pulsed high prior to the first readout after power up and this may be accomplished by including a **read-reset** pulse as part of a “chip reset” sequence performed at the beginning of any data accumulation interval and following every event.)

The pulse-height readout proceeds from dual-gain PHA0 toward PHA15 with high gain preceding low gain pulse-heights. There are two modes of sparse readout, specified separately for each dual-gain PHA by bits in the command register. For both modes, readout occurs only for active (powered) PHAs with one or both gain sections triggered. In the default "terse" mode (command bit equal to its initialized value of zero), only the high gain pulse-height is readout unless the high gain ADC has overflowed AND the low gain ADC has triggered, in which case only the low gain pulse-height is readout. In the "verbose" mode (configuration bit equal to one) the high and low gain pulse-heights are readout if the corresponding ADCs have triggered. (If both triggered, both are readout.)

For Solar Probe 16 bit shift registers were added to record a 4 usec history of the discriminator activity and aid in cross talk identification. The shift register readout follows the corresponding PHA word if **adc_read_sel** is high.

In systems with multiple PHA chips, the readout can be daisy-chained as illustrated in Figure 6. The 23 least significant bits of the tri-state readout buss are distributed in parallel to all chips. The **token-in** and **token-out** signals, as well as the **read-clk-in** and **read-clk-out** signals are connected on adjacent chips as shown, allowing the "token" signal to propagate from left to right, while the "read-clk" signal propagates from right to left. The external logic pays attention to the **token-out** signal from the last chip in the chain (or the most significant bit of the 24-bit tri-state buss of that chip) to determine when the last pulse-height word has been readout from all the chips in the chain. Each chip in the readout chain must be given a unique chip address by the hard-wiring the **chip-adr-0,1,2, and 3** inputs. However, the order of pulse-height readout is set not by the chip address, but by the ordering of the chips along the daisy chain (and proceeds from left to right in Figure 6).

In the STEREO instruments the data readout will be performed by embedded MISCs (Minimal Instructions Set Computers). The readout architecture is designed to allow fast readout under software control using the 24-bit MISC I/O buss (G-buss). Dedicated logic will handle PHA control up to the point of data readout, at which point a MISC interrupt routine will control the readout process, resetting the dedicated logic when done. In this case the 23 least significant bits of the 24-bit PHA data buss are connected to the least significant 23 bits of the 24 bit MISC G-buss input, while the most significant G-buss input bit is driven only by the most significant bit of the PHA buss readout pin from the last PHA chip in the daisy chain. This allows a tight software loop to read the data and quickly test the most significant bit of the input (via shift left and branch on carry) to ascertain when the last data word has been read.

Counters. The 23 bit counters are asynchronously cleared by a high level on the **ctr-reset** chip input. The counters are readout in the same way as pulse-height data, but with the **adc-read-sel** chip input held low. Only counters for active (powered up) PHAs are included in the readout.

Changes from STEREO PHASIC

The Solar Probe PHASIC design derives from the STEREO PHASIC design with modifications intended to allow better performance for the particular range of detector capacitances and signal amplitudes of the EPI-HI Silicon detectors. An improvement in dynamic range was needed mainly for the LET 500 um L2 detectors, where the desire for detection of minimum ionizing electrons implied a threshold target of near 120 keV and a desire to keep 45 degree stopping Zn nuclei on scale implied a full scale near 2700 MeV. The changes to the PHASIC to meet these goals included: 1) a different method of preamp compensation that does not compromise noise performance, 2) a different output stage for the preamp to enlarge the linear output voltage swing from 2.7 to 4.0 Volts, 3) a buffer amplifier at the beginning of the high gain signal chains, 4) enlargement of the high/low gain ratio from 20 to 68 (or 40), and 5) modification of the peak detector for lower noise. The enlargement of the high/low gain ratio from 20 to 68 was suitable for the thicker detectors, but a lesser ratio (40) was preferable for the thinner detectors and so one of the command bits was used to make the ratio of 68 or 40 selectable. No net increase in the number of command bits was made since the new preamp compensation method requires only two configuration bits, rather than the 3 used in the STEREO version. In order to ensure that the preamp outputs could still be monitored accurately using the preout scope pin, the preout buffer amplifier was also modified slightly to enlarge its output swing.

During the redesign of the PHASIC for Solar Probe, an effort was made to understand the source of cross talk within the PHASIC to assess the possibility of reducing or eliminating it. Cross talk measurements were made using a STEREO PHASIC including capture of scope traces of cross

talk produced transients at each of the available test points along a signal chain. In addition the amplitude and shape of cross talk signals was compared as a function of “distance” between the cross talk generating and receiving channels. While the general level of cross talk could be reproduced, the agreement between simulation and observation was not good enough to conclude that a quantitative understanding of the cross talk mechanisms had been achieved. However, the study did show that various types of cross talk (i.e. within the PHASIC versus at the detectors) did produce differently shaped waveforms at the peak detector input. As a result a 16 bit shift register was added to each signal chain and configured to sample the discriminator output at 4 MHz, providing a 4 usec history of the discriminator output. This added information along with each pulse height should allow the in-flight software to more easily identify signals resulting from cross talk (or affected by pileup). Given the lack of a good quantitative understanding of the internal cross talk mechanism no design mods were aimed at reducing the internal cross talk. Rather the approach was to preserve the cross talk’s known level and character; improving the cross talk situation only via addition of the 16 bit shift registers.

In using the STEREO PHASIC it was learned that following pulse height analysis of signals of amplitude near 1/5 F.S. there was a tendency to retrigger. This is caused by the shape of the signal at the input to the discriminator having an overshoot during recovery to baseline and occurs only for events whose PHA analysis completes 10-15 usec after initiation, during the time of the overshoot. Fortuitously, changes made in the preamp to postamp coupling and slight changes made to various shaping time constants resulted in lowering the amplitude of this overshoot which should reduce the retriggering problem. The intention is to also address the retriggering in the external logic design by extending enforced deadtime to beyond 15 usec for events which would otherwise terminate in the 10 to 15 usec window.

Chip Layout

The chip layout is shown in Figure 9. Preamplifier input bond pads are across the top. Generally power supply and other DC signal bond pads are on the sides with digital i/f signals along the bottom. In the figure large capacitors appear as dark purple rectangles. The 200 pF hold capacitors can be seen (32 of them) just above the digital circuitry which appears whitish at the bottom. About half of the chip area is consumed by passive components.

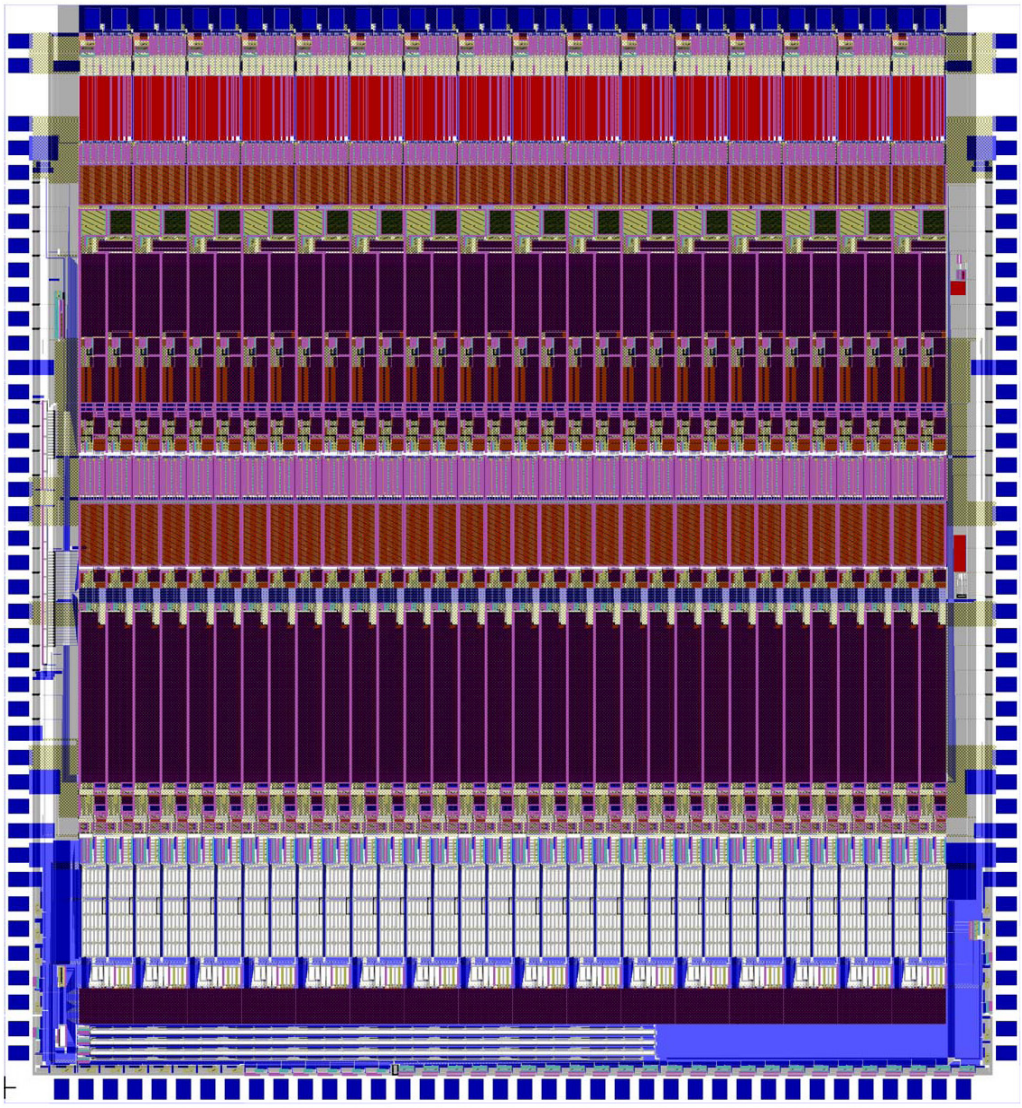

Figure 9 (Currently shows the STEREO phasic layout. Mods for Solar Probe are in progress.) The signal names associated with each bond pad are listed in Table 5:

Table 5: Bond Pad Assignments

Index	Top	Left	Right	Bottom
0	prein-0	testRef	testRef	adc-read-sel
1	pre5V-0	testRet	testRet	cmd-strobe
2	prein-1	preGND	preGND	cmd-reset*
3	pre5V-1	aGND	aGND	ctr-reset
4	prein-2	irndn-00H	irndn-15L	pha-reset
5	pre5V-2	irndn-00L	irndn-15H	clg
6	prein-3	irndn-01H	irndn-14L	clk
7	pre5V-3	irndn-01L	irndn-14H	test-pulse
8	prein-4	vn1a	preout	rndn-or
9	pre5V-4	irndn-02H	irndn-13H	rndn-gor-0
10	prein-5	irndn-02L	irndn-13L	rndn-gor-1
11	pre5V-5	vn2	vp2	rndn-gor-2
12	prein-6	a5V	a5V	disc-or
13	pre5V-6	irndn-03H	irndn-12L	lop-or
14	prein-7	irndn-03L	irndn-12H	data-0
15	pre5V-7	irndn-04H	irndn-11L	data-1
16	prein-8	irndn-04L	irndn-11H	data-2
17	pre5V-8	aGND	vp1a	data-3
18	prein-9	r5V	r5V	data-4
19	pre5V-9	scope-in	irndn-10L	data-5
20	prein-10	irndn-05H	irndn-10H	data-6
21	pre5V-10	irndn-05L	scope-out	data-7
22	prein-11	rGND	rGND	data-8
23	pre5V-11	irndn-06H	irndn-09L	data-9
24	prein-12	irndn-06L	irndn-09H	data-10
25	pre5V-12	irndn-07H	irndn-08L	data-11
26	prein-13	irndn-07L	irndn-08H	data-12
27	pre5V-13	n5Vref	vthresh	data-13
28	prein-14	discGND	discGND	data-14
29	pre5V-14	aGND	aGND	data-15
30	prein-15	vn1	vp1	data-16
31	pre5V-15	d5V	d5V	data-17
32		dGND	dGND	data-18
33		ioVdd	ioVdd	data-19
34		chip-adr-0	chip-adr-2	data-20
35		chip-adr-1	chip-adr-3	data-21
36		cmd-data-in	cmd-data-out	data-22
37		cmd-clk-out	cmd-clk-in	data-23
38		token-in	token-out	
39		read-clk-out	read-clk-in	
40		bias	read-reset	

Packaging

The chip is packaged in an 80-pin covar package having dimensions as shown in Figure 10. Also included in the package are precision resistors that set the rundown current for each ADC and power supply by-pass networks. The pin assignments for the package are listed below in Table 6. The package is square shaped with 20 pins on each side. Pin numbering proceeds from pin 1 at the top of the left side, increasing counterclockwise to 80 at the leftmost pin on the top side. The sensitive preamplifier inputs are along the top side, while digital signals are along the sides and bottom.

Table 6: Package Pin Assignments

Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal
1	aGND	21	rndn-gor-0	41	data-15	61	aGND
2	n5V	22	rndn-gor-1	42	data-16	62	aGND
3	scope-in	23	rndn-gor-2	43	data-17	63	prein-15
4	5V	24	disc-or	44	data-18	64	prein-14
5	chip-adr-0	25	lop-or	45	vtresh	65	prein-13
6	chip-adr-1	26	data-0	46	data-20	66	prein-12
7	cmd-data-in	27	data-1	47	data-21	67	prein-11
8	cmd-clk-out	28	data-2	48	data-22	68	prein-10
9	token-in	29	data-3	49	data-23	69	prein-9
10	read-clk-out	30	data-4	50	read-reset	70	prein-8
11	adc-read-sel	31	data-5	51	read-clk-in	71	prein-7
12	cmd-strobe	32	data-6	52	token-out	72	prein-6
13	cmd-reset*	33	data-7	53	cmd-clk-in	73	prein-5
14	ctr-reset	34	data-8	54	cmd-data-out	74	prein-4
15	pha-reset	35	data-9	55	chip-adr-3	75	prein-3
16	clg	36	data-10	56	chip-adr-2	76	prein-2
17	clk	37	data-11	57	ioVdd	77	prein-1
18	test-pulse	38	data-12	58	scope-out	78	prein-0
19	rndn-or	39	data-13	59	preout	79	aGND
20	dGND	40	data-14	60	aGND	80	testRef

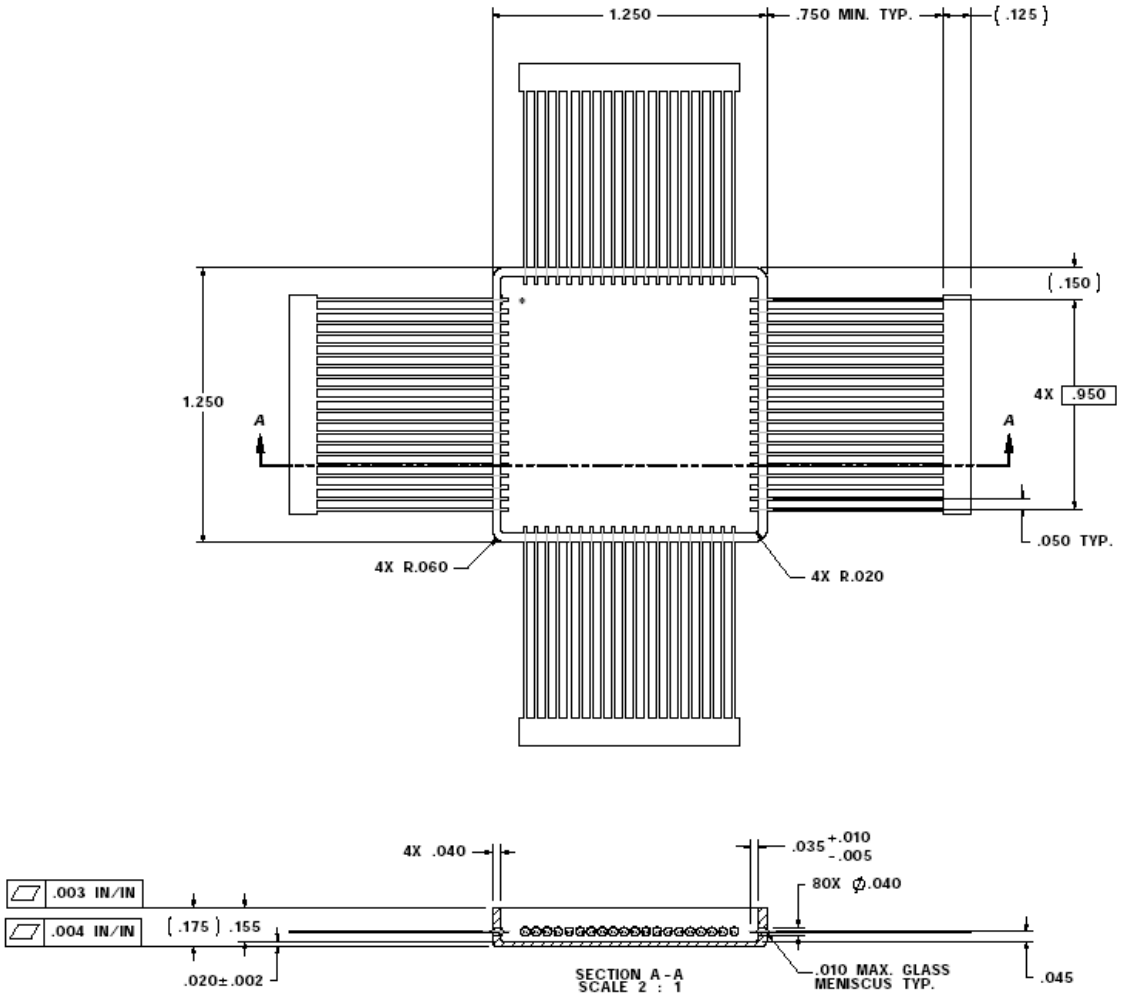
1.250
.750 MIN. TYP.
(.125)
(.150)
1.250
A
A
4X .950
.050 TYP.
4X R.060
4X R.020
4X .040
.035 +.010 -.005
80X ⌀.040
.003 IN/IN
.004 IN/IN
(.175) .155
.020± .002
SECTION A-A
SCALE 2 : 1
.010 MAX. GLASS MENISCUS TYP.
.045

Figure 10.