TOTAL MISC IO AVAILABLE (115)

TOTAL MISC IO NEEDED = 59 + 27 = 86

MEMORY (59)

address lines (21)
data lines (24)
memory ctrl (4) mr/w, mr*/w, mram*, ram**
parity (7)
clk(1)
serial_boot(1) not needed for flight
zz_sleep(1)

Other MISC CTRL Signals

MISC IO Needed (2+4+2+9+8+1+1=27)

Interface Enable (2)

EN_TLM_A
EN_TLM_B

SC IF(4)

DPU_CMD_A*
DPU_CMD_B*
DPU_TLM_A*
DPU_TLM_B*

GSE IF(2)

GSE_CMD*
GSE_CMD_ECHO*

telescope IF (9)

LET1_CMD*
LET1_CMD_ECHO*+
LET1_DATA*+
LET2_CMD*
LET2_CMD_ECHO*+
LET2_DATA*+
HET1_CMD*
HET1_CMD_ECHO*+
HET1_DATA*+

HKCHIP(8)

ADCOUT
ADCCLK
DACCLK
MUXCLK
ADCGO
CMDDATA
CMDSTROBE
PO_RESET*

BIAS(1)

BIASCLK

LVPS(1)

LVPS_SYNCH

ACTEL
AXcelerator FPGAs
AX250-PQ208
208-PQFP

U2
EM: AX250-PQ208 FLIGHT: RTAX250SL-CQ208B

U3
UT8MR2M8[CDFP-40_Y]

AEROFLEX
2M x 8-Bit
MRAM
UT8MR2M8
CDFP-40_Y

Approvals	Date	Title	Solar Probe Schematic, DPU_MISC
Drawn: J.Burnham	09-05-13		
Checked:		MISC, OSC, MRAM	
Approved:		Size: C	DWG. No. 500101 Revision: A Sheet 1 of 8
File:			

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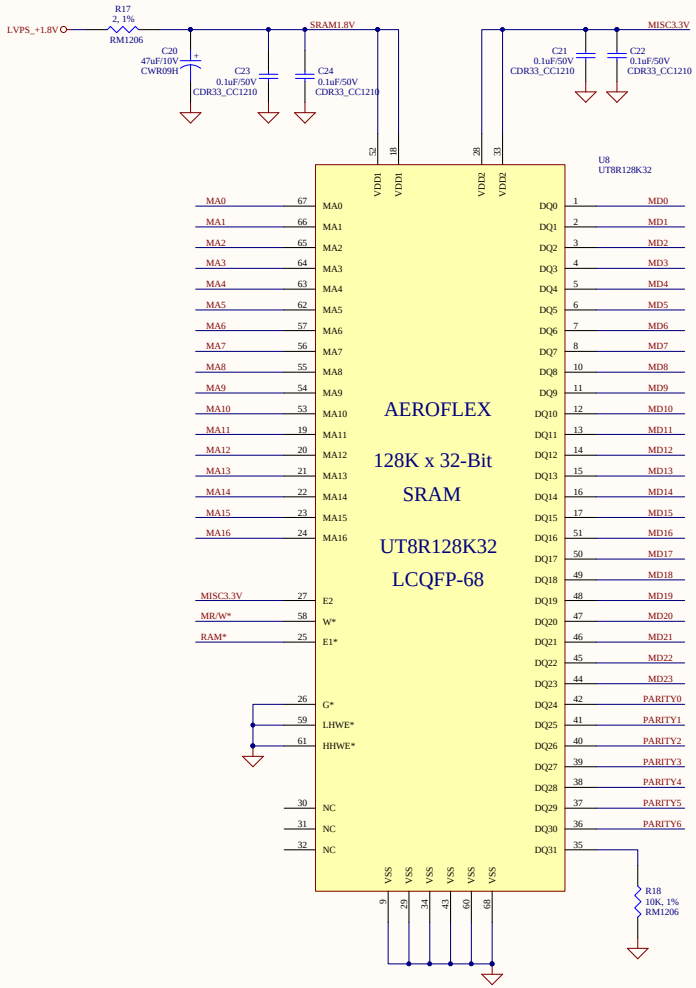

Approvals	Date	Title	
Drawn: J.Burnham	09-05-13	*Solar Probe*	
Checked:		*Schematic, DPU_SRAM*	
Approved:		*SRAM, Power_On_Reset*	
File:		Size: C DWG. No. 500101 Revision: A Sheet 2 of 8	

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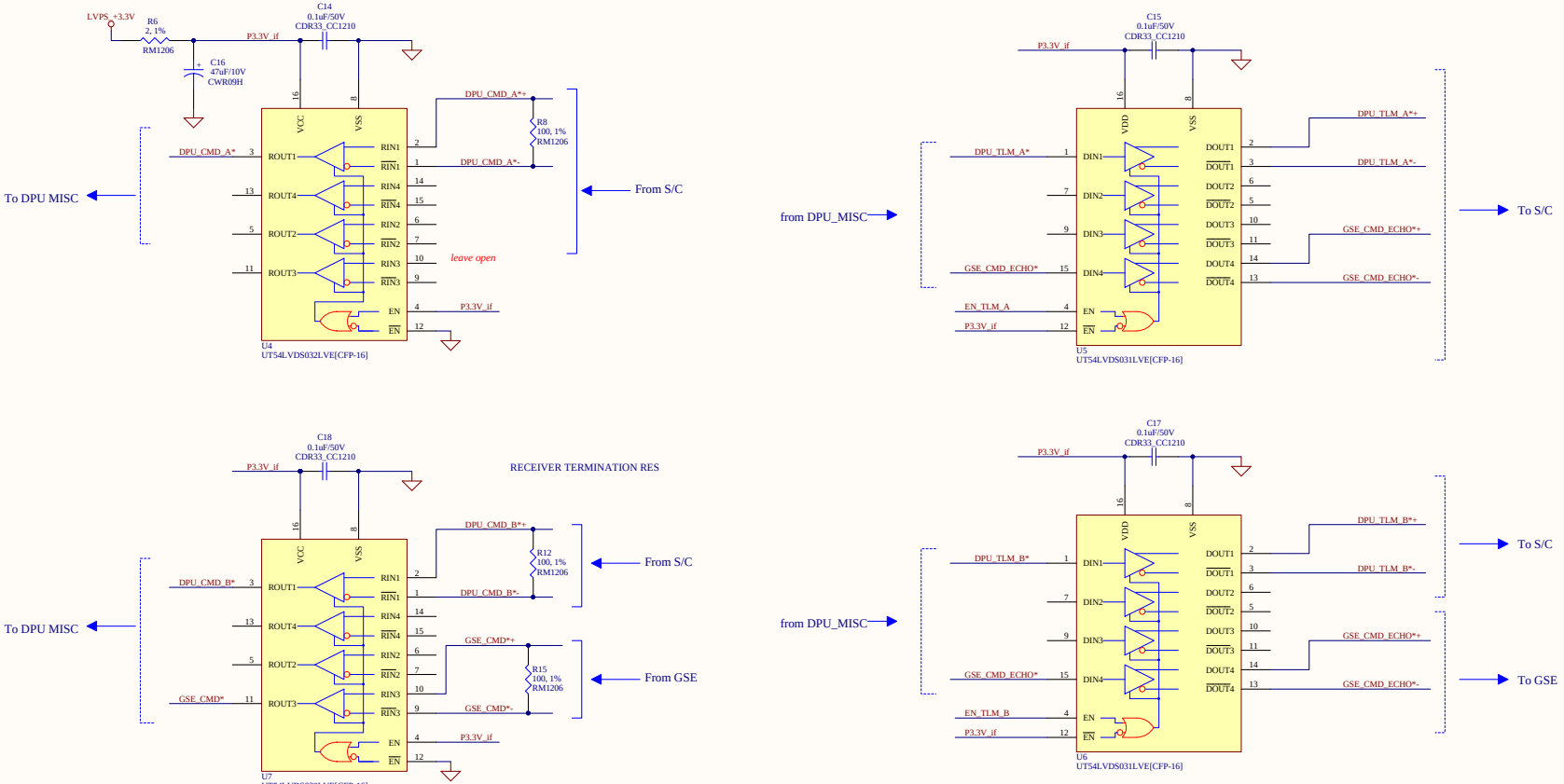

Approvals	Date	Title	
Drawn: J.Burnham	09-05-13	Solar Probe Schematic, DPU_SC_IF	
Checked:		Spacecraft Interface	
Approved:		Size: C	DWG. No. 500101 Revision: A Sheet 3 of 8
File:			

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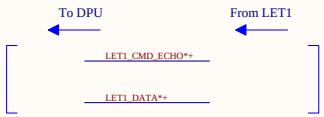
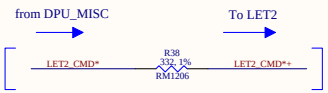
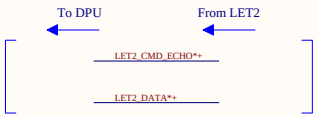
IF to LET1

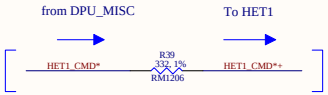


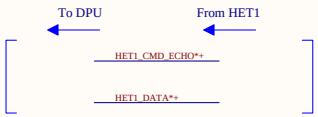
IF to LET2





IF to HET1





Approvals	Date	Title					
Drawn: J.Burnham	09-05-13	***Solar Probe***					
		Schematic, DPU_Telescope_IF					
Checked:		*Interface to LET1, LET2 and HET1*					
Approved:		Size: C	DWG. No. 500101	Revision: A	Sheet 4 of 8		
File:							

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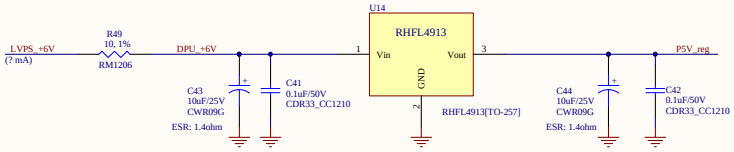

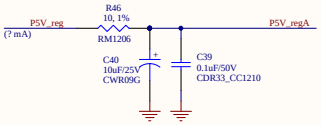

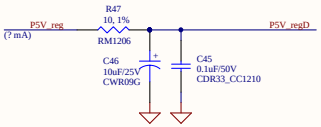

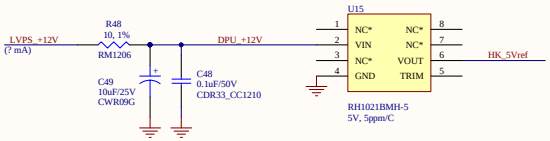

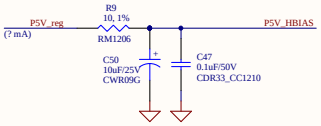

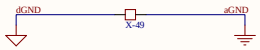

Approvals	Date	Title	
Drawn: J.Burnham	09-05-13	Solar Probe Schematic, DPU_FIXED_REG	
Checked:		Fixed +5V Regulator	
Approved:		Size: C	DWG. No. 500101 Revision: A Sheet 5 of 8
File:			

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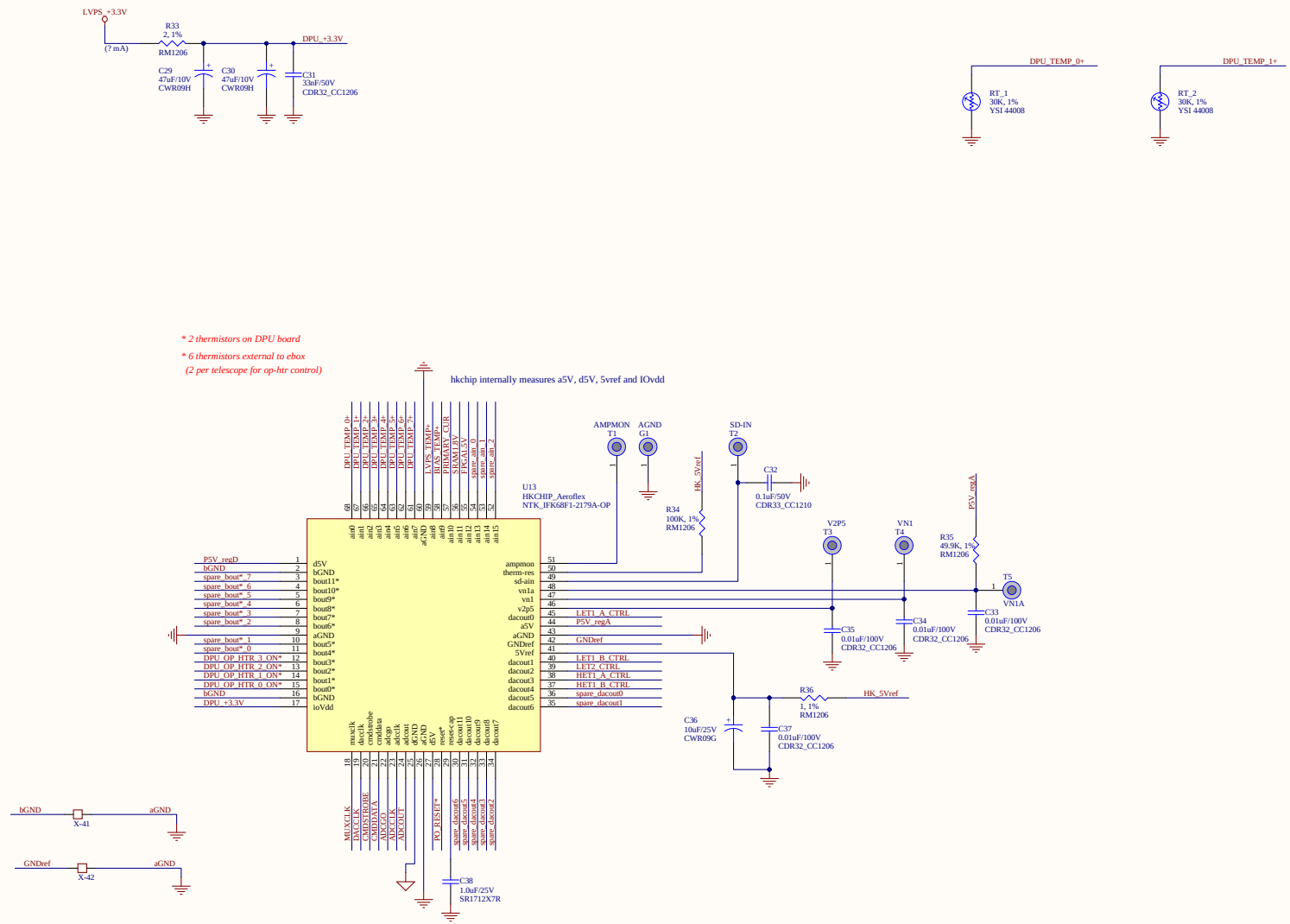

Approvals	Date	Title					
Drawn: J.Burnham	09-05-13	**Solar Probe**					
		Schematic, hkchip					
Checked:		Housekeeping ASIC					
Approved:		Size: C	DWG. No. 500101	Revision: A	Sheet 6 of 8		
File:							

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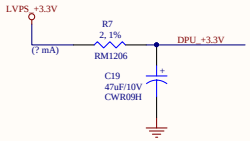
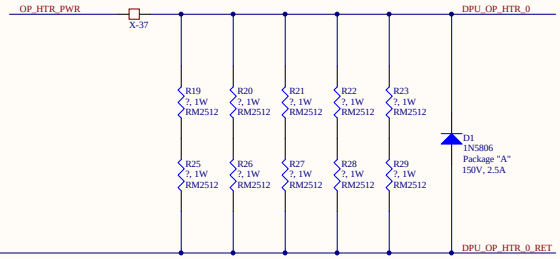
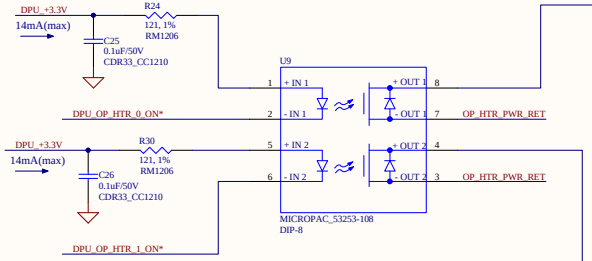


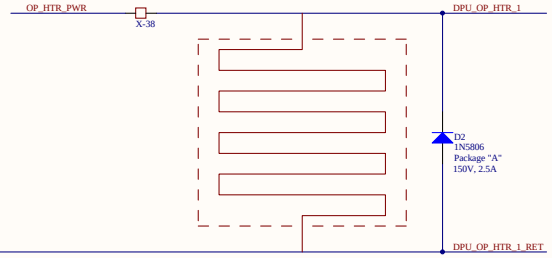
One internal OP heater on DPU board
3 external OP heaters (one per telescope)



Internal OP heater on DPU board

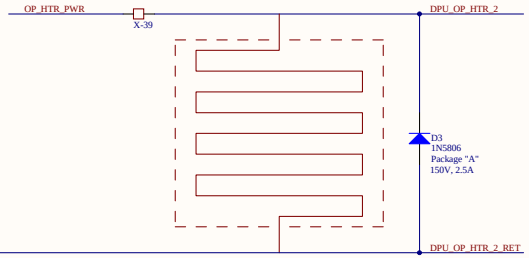
Board Mounted Resistors: ?Wmax @ 30V (~?ohm)





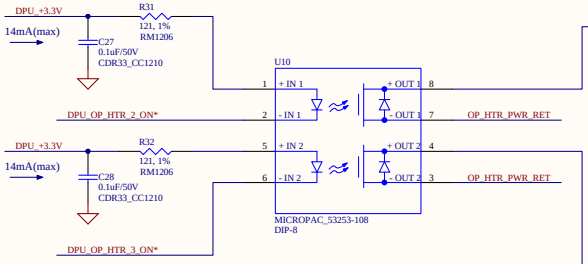
External Chassis OP heater

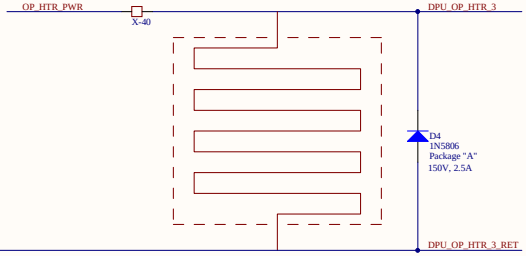
KAPTON HEATER: ?Wmax @ 30V (~?ohm)



External Chassis OP heater

KAPTON HEATER: ?Wmax @ 30V (~?ohm)





External Chassis OP heater

KAPTON HEATER: ?Wmax @ 30V (~?ohm)

Approvals	Date	Title	
Drawn: J.Burnham	09-05-13	***Solar Probe***	
Checked:		***Schematic, DPU_OP_HTR***	
Approved:		*Operational Heaters*	
File:		Size: C	DWG. No. 500101	Revision: A	Sheet 7 of 8

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SRL

ALL CONNECTOR DEFINITIONS
STILL TBD (PENDING RELEASE OF SPP to ISIS ICD)

Connector to Trinity LVPS

LVPS-P1

LVPS_+6V	1	27	aGND
LVPS_+6V	2	28	aGND
LVPS_+6V	3	29	aGND
LVPS_+6V	4	30	aGND
LVPS_+6V	5	31	aGND
LVPS_+12V	6	32	LVPS_-6V
LVPS_+12V	7	33	LVPS_-6V
LVPS_+12V	8	34	LVPS_-6V
+12V_PWR_RET	9	35	+12V_PWR_RET
LVPS_TEMP+	10	36	*LVPS_TEMP-*
LVPS_TEMP+	11	37	*LVPS_TEMP-*
LVPS_+1.5V	12	38	LVPS_+1.8V
LVPS_+1.5V	13	39	LVPS_+1.8V
LVPS_+1.5V	14	40	LVPS_+1.8V
dGND	15	41	LVPS_+3.3V
dGND	16	42	LVPS_+3.3V
dGND	17	43	LVPS_+3.3V
dGND	18	44	PRIMARY_CUR_RET
PRIMARY_CUR	19	45	PRIMARY_CUR_RET
PRIMARY_CUR	20	46	OP_HTR_PWR_RET
OP_HTR_PWR	21	47	OP_HTR_PWR_RET
OP_HTR_PWR	22	48	OP_HTR_PWR_RET
OP_HTR_PWR	23	49	OP_HTR_PWR_RET
OP_HTR_PWR	24	50	LVPS-J1-SPARE1
LVPS-J1-SPARE0	25	51	LVPS_SYNCH
LVPS_SYNCH	26		

X-8, X-9

Glenair 51-pos Nano TH ST Receptacle
891-007-51SA2-BST1J-429

Connector to BIAS

DPU-J1

LVPS_+12V	1	17	+12V_PWR_RET
LVPS_+12V	2	18	+12V_PWR_RET
P5V_HBIAS	3	19	LET2_CTRL
P5V_HBIAS	4	20	LET2_CTRL
LVPS_-6V	5	21	HET1_A_CTRL
LVPS_-6V	6	22	HET1_A_CTRL
aGND	7	23	HET1_B_CTRL
aGND	8	24	HET1_B_CTRL
LET1_A_CTRL	9	25	DPU-J1-SPARE0
LET1_A_CTRL	10	26	DPU-J1-SPARE1
LET1_B_CTRL	11	27	DPU-J1-SPARE2
LET1_B_CTRL	12	28	dGND
BIAS_TEMP+	13	29	dGND
BIAS_TEMP+	14	30	BIASCLK
BIAS_TEMP-	15	31	BIASCLK
BIAS_TEMP-	16		

X-2, X-3, X-5

Glenair 31-pos Nano TH RA Plug
891-008-31PA2-BRT1T-429

Connector to SC CMD/Data

EPH-J2

DPU_CMD_A*+	1	9	TLM_DATA_SHIELD
DPU_CMD_A*-	2	10	EPH-J2-SPARE0
DPU_CMD_B*+	3	11	GSE_CMD*+
DPU_CMD_B*-	4	12	GSE_CMD*-
DPU_TLM_A*+	5	13	GSE_CMD_ECHO*+
DPU_TLM_A*-	6	14	GSE_CMD_ECHO*-
DPU_TLM_B*+	7	15	dGND
DPU_TLM_B*-	8		

X-1, X-4

Glenair 15-pos TH RA Rec
MWDM2L-15SCBRR2-.110-429

Connector to External Thermal hardware

EPH-J3

DPU_TEMP_2+	1	12	aGND
DPU_TEMP_3+	2	13	aGND
DPU_TEMP_4+	3	14	aGND
DPU_TEMP_5+	4	15	aGND
DPU_TEMP_6+	5	16	aGND
DPU_TEMP_7+	6	17	aGND
EPH-J3-SPARE0	7	18	EPH-J3-SPARE2
EPH-J3-SPARE1	8	19	DPU_OP_HTR_1_RET
DPU_OP_HTR_1	9	20	DPU_OP_HTR_2_RET
DPU_OP_HTR_2	10	21	DPU_OP_HTR_3_RET
DPU_OP_HTR_3	11		

X-15, X-17, X-19

Glenair 21-pos TH RA Plug
MWDM2L-21PCBRR2-.110-429

Connector to LET1

LET1-P1

LVPS_+1.5V	1	14	LET1_CMD*+
LVPS_+1.5V	2	15	LET1_CMD*+
LVPS_+1.8V	3	16	LET1_CMD_ECHO*+
LVPS_+1.8V	4	17	LET1_CMD_ECHO*+
LVPS_+3.3V	5	18	LET1_DATA*+
LVPS_+3.3V	6	19	LET1_DATA*+
dGND	7	20	dGND
dGND	8	21	dGND
aGND	9	22	LVPS_+12V
aGND	10	23	LVPS_+12V
LVPS_-6V	11	24	LVPS_+6V
LVPS_-6V	12	25	LVPS_+6V
aGND	13		

Glenair 25-pos Nano TH ST Plug
891-006-25PA2-BST1J-429

Connector to LET2

LET2-P1

LVPS_+1.5V	1	14	LET2_CMD*+
LVPS_+1.5V	2	15	LET2_CMD*+
LVPS_+1.8V	3	16	LET2_CMD_ECHO*+
LVPS_+1.8V	4	17	LET2_CMD_ECHO*+
LVPS_+3.3V	5	18	LET2_DATA*+
LVPS_+3.3V	6	19	LET2_DATA*+
dGND	7	20	dGND
dGND	8	21	dGND
aGND	9	22	LVPS_+12V
aGND	10	23	LVPS_+12V
LVPS_-6V	11	24	LVPS_+6V
LVPS_-6V	12	25	LVPS_+6V
aGND	13		

Glenair 25-pos Nano TH ST Plug
891-006-25PA2-BST1J-429

Connector to HET1

HET-P1

LVPS_+1.5V	1	14	HET1_CMD*+
LVPS_+1.5V	2	15	HET1_CMD*+
LVPS_+1.8V	3	16	HET1_CMD_ECHO*+
LVPS_+1.8V	4	17	HET1_CMD_ECHO*+
LVPS_+3.3V	5	18	HET1_DATA*+
LVPS_+3.3V	6	19	HET1_DATA*+
dGND	7	20	dGND
dGND	8	21	dGND
aGND	9	22	LVPS_+12V
aGND	10	23	LVPS_+12V
LVPS_-6V	11	24	LVPS_+6V
LVPS_-6V	12	25	LVPS_+6V
aGND	13		

Glenair 25-pos Nano TH ST Plug
891-006-25PA2-BST1J-429

Approvals	Date	Title	*Solar Probe*
Drawn: J.Burnham	09-05-13		***Schematic, DPU_Connectors***
Checked:			*Connectors, Filters*
Approved:		Size: C	DWG. No. 500101 Revision: A Sheet 8 of 8
File:			

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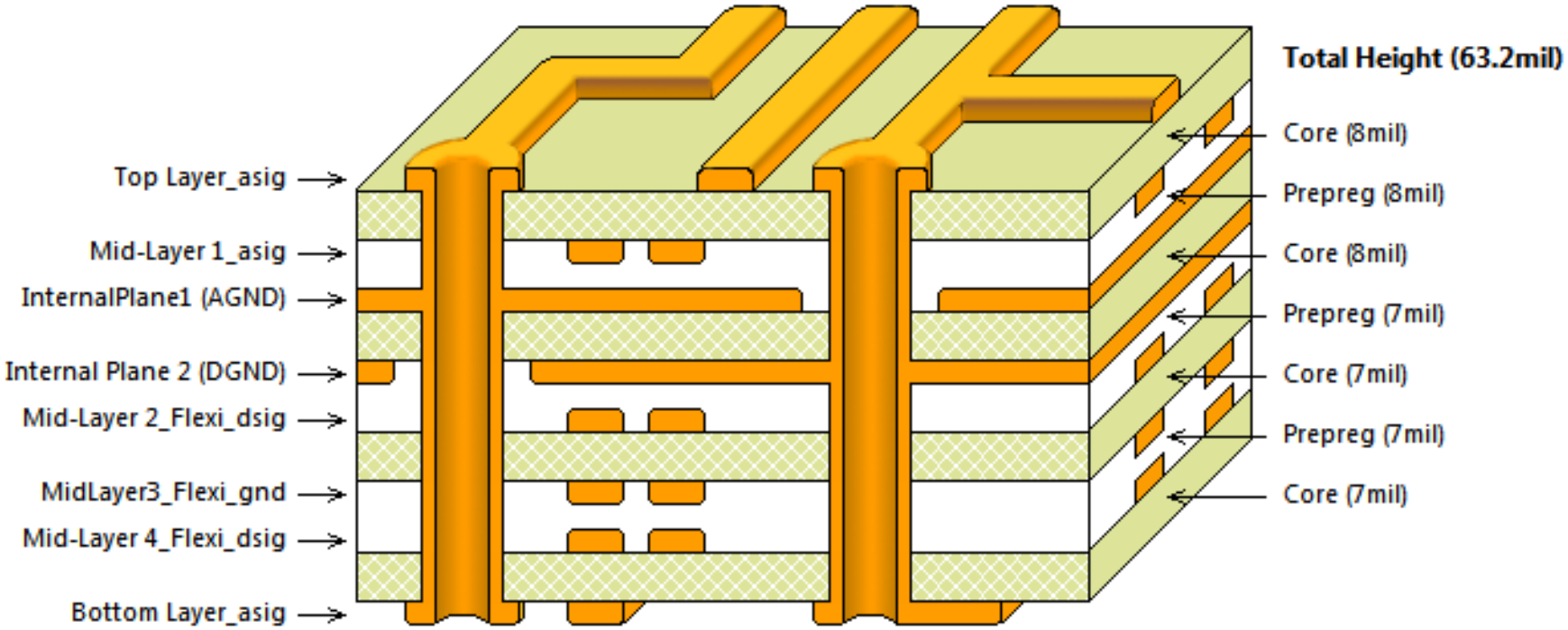
Comment	Description	Procurement P/N	Footprint	Quantity
Glenair 25-pos Nano TH ST Plug	Glenair 25-pos Nano TH ST Plug Jackscrew	891-006-25PA2-BST1J-429	891-006-25PSBST1J	3
Glenair 51-pos Nano TH ST Receptacle	Glenair 51-pos Nano TH ST Receptacle Jackscrew	891-007-51SA2-BST1J-429	891-007-51SSBST1J	1
Glenair 31-pos Nano TH RA Plug	Glenair 31-pos Nano TH RA Plug	891-008-31PA2-BRT1T-429	891-008-31PSBRT	1
RHFL4913[TO-257]	Radhard, Positive 5V, Fixed Voltage Regulator	5962F0253602QZC	TO-257	1
UT8R128K32	Aeroflex SRAM 128K x 32, 4MSRAM's	5962R0323601QXC	UT8R128K32[LCQFP-68]	1
UT8MR2M8[CDFP-40_Y]	Aeroflex Non-volatile MRAM 2M x 8, 16M	5962R1222701QYC	CDFP-40_Y	1
UT54LVDS031LVE[CFP-16]	Aeroflex, Radiation Hardened 3.3V Quad LVDS Line Driver	5962R9865105VYC	CFP-16	2
UT54LVDS032LVE[CFP-16]	Aeroflex, Radiation Hardened 3.3V Quad LVDS Line Receiver	5962R9865205VYC	CFP-16	2
MICROPAC_53253-108	Rad Tolerant Dual Power MOSFET Optocouplers, 90V - 0.8A, MIL-PRF38534	53253-108	MICROPAC_[DIP-8]	2
0.01uF/100V	Capacitor, CDR32, 10%, 100V	CDR32BX103BKUS	CDR32_CC1206	5
33nF/50V	Capacitor, CDR32, 10%, 50V	CDR32BX333AKUS	CDR32_CC1206	1
0.1uF/50V	Capacitor, CDR33, 10%, 50V	CDR33BX104AKUS	CDR33_CC1210	28
HKCHIP_Aeroflex	Aeroflex Housekeeping Chip	Custom	NTK_IFK68F1-2179A-OP	1
47uF/10V	Capacitor, CWR09, 10%, 10V	CWR09FC476KCB	CWR09H	7
10uF/25V	Capacitor, CWR09, 10%, 25V	CWR09KC106KCB	CWR09G	8
1, 1%	Resistor, RM, 1%, 100ppm/C, 250mW	D55342K07B1D00S	RM1206	2
2, 1%	Resistor, RM, 1%, 100ppm/C, 250mW	D55342K07B2D00S	RM1206	6
10, 1%	Resistor, RM, 1%, 100ppm/C, 250mW	D55342K07B10D0S	RM1206	5
10K, 1%	Resistor, RM, 1%, 100ppm/C, 250mW	D55342K07B10E0S	RM1206	3
49.9K, 1%	Resistor, RM, 1%, 100ppm/C, 250mW	D55342K07B49E9S	RM1206	1
100, 1%	Resistor, RM, 1%, 100ppm/C, 250mW	D55342K07B100DS	RM1206	3
100K, 1%	Resistor, RM, 1%, 100ppm/C, 250mW	D55342K07B100ES	RM1206	1
121, 1%	Resistor, RM, 1%, 100ppm/C, 250mW	D55342K07B121DS	RM1206	4
332, 1%	Resistor, RM, 1%, 100ppm/C, 250mW	D55342K07B332DS	RM1206	3
AX250-PQ208	EM-Axcelerator AX250 FPGA, 115 User I/Os, 208-Pin PQFP device-wYAMAICHI PQ208 SOCKET	EM: AX250-PQ208 FLIGHT: RTAX250SL-CQ208B	AX250-PQ208_wSOCKET	1
1N5806	150V , 2.5A UltraFast Recovery Glass Rectifier diode	JANTXV1N5806	1N5806[BODY_A]	4
?, 1W	Power Resistor, RM, 1%, 100ppm/C, 1W	M55342K09BxxxD	RM2512	10
MWDM-15SCBR	Micro-D SCBR 15-pin Connector	MWDM2L-15SCBRR2-.110-429	MWDM-15SCBR	1
MWDM2L-21PCBRR2.-110-429	Micro-D CBR 21-pin Connector	MWDM2L-21PCBRR2-.110-429	MWDM-21PCBR	1
QT188L6S-58.9824MHz	Hybrid Crystal Oscillator, B+ Series, QTech	QT188L6S-58.9824MHz	QT188[SOJ-4]	1
5V, 5ppm/C	Precision 5V Reference	RH1021BMH-5	RH1021BMH-5	1
30K, 1%	Thermistor, 30k, 1% @ -55C to +90C, 10.72 Resistance ratio, 32AWG Tinned coated solid wire	S311P18-09S7R6	YSI THERMISTOR [SMD]	2
1.0uF/25V	Presidio, X7R 1712, Cap, Ceramic, 1.0uF, 10%, 25V, MIL-PRF-123	SR1712X7R105K1NT95#M123	SR1712X7R105K1NT90#M123	1
Terminals	JPL, LAT/D-CEMO, PCB 62mils Thickness, Bifurcated Terminal, Hole=62mils, Pad=94mils	ST11204-803	Term-62	6



DPU Board Example Layerstack

EPI–Hi Block Diagram

BK 5/5/13

LET 1

A

B

PHASIC

x 3

(40 channels)

MISC

(FPGA,
SRAM,
clock osc)

LV bias

HK chip

LET 2

PHASIC

x 2

(24 channels)

MISC

(FPGA,
SRAM,
clock osc)

LV bias

HK chip

HET

A

B

PHASIC

x 3

(36 channels)

MISC

(FPGA,
SRAM,
clock osc)

HK chip

DPU

MRAM

MISC

(FPGA,
SRAM,
clock osc)

HK chip

Spacecraft I/F

side A & B

(LVDS drvr & rcvr)

Command

Data

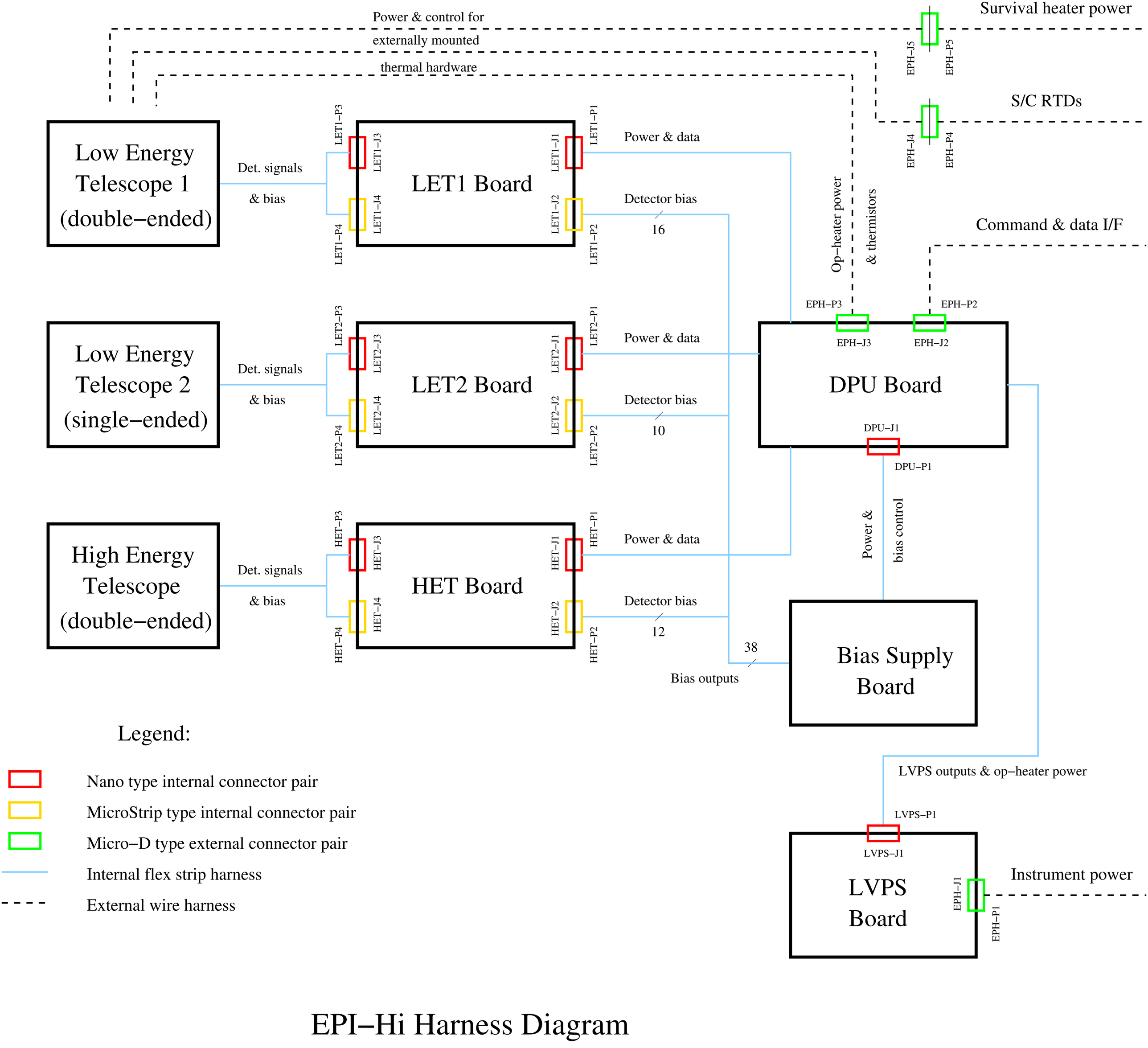
Op–heater
control

Bias Supply

(HV bias x 5
& 25V tap)

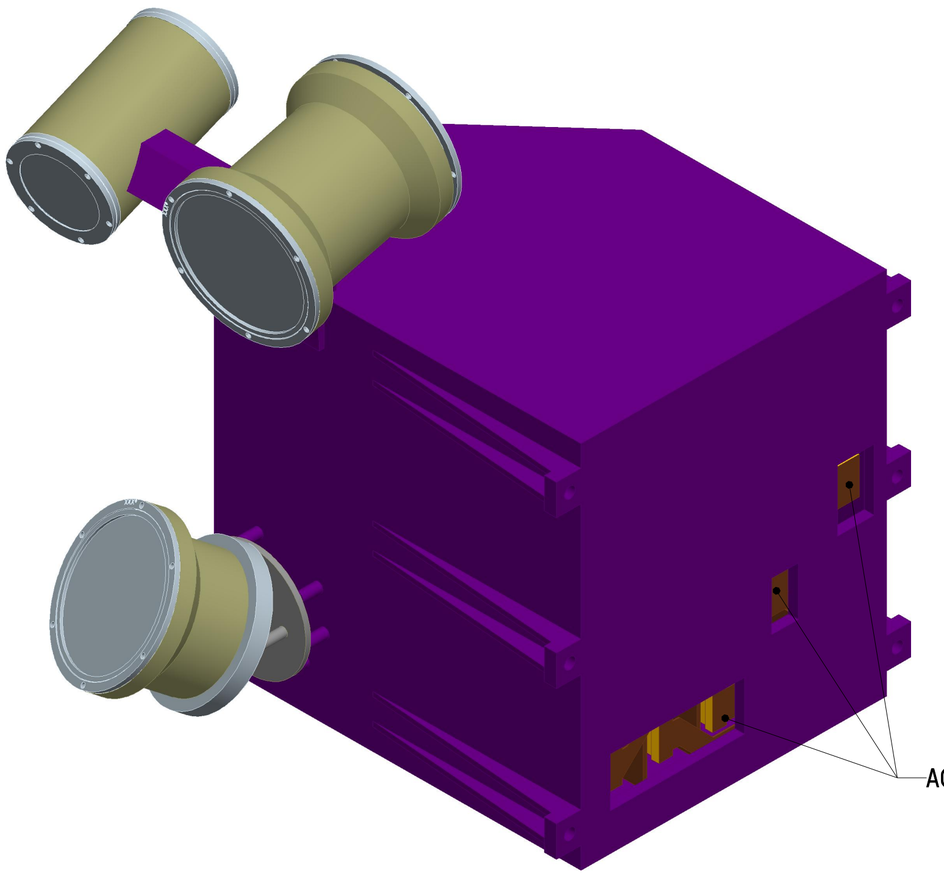
LVPS

28V from S/C

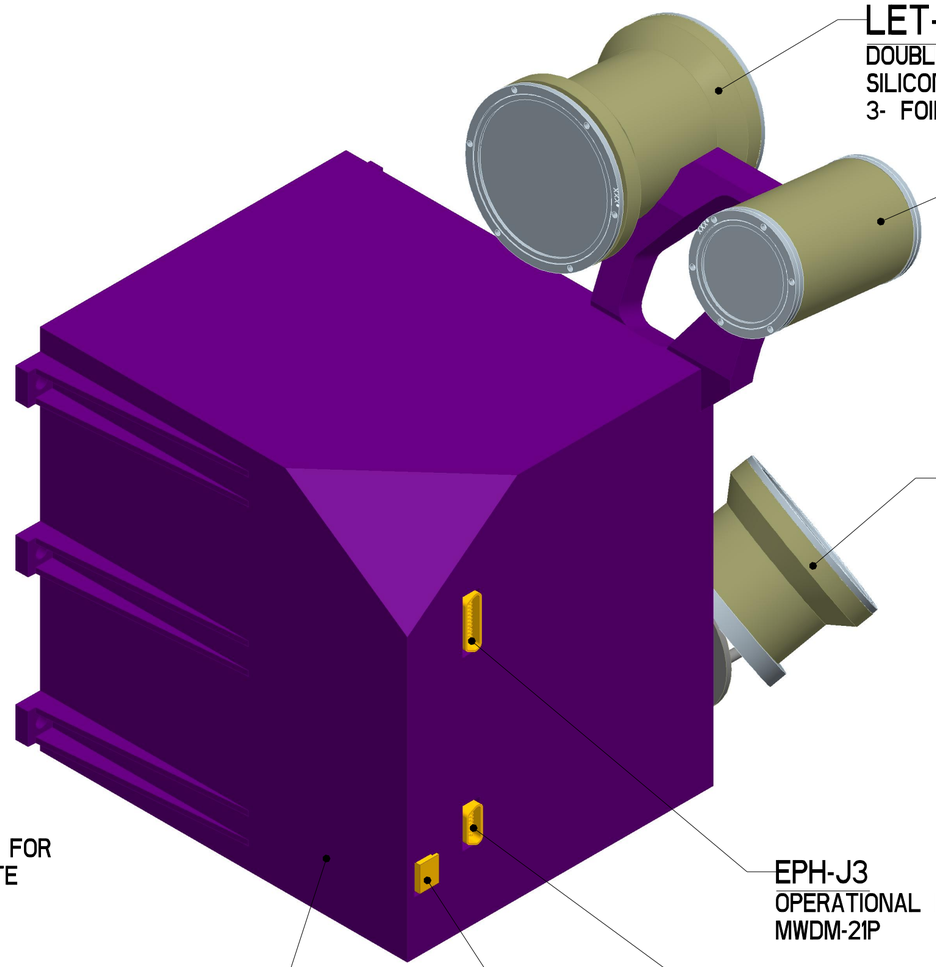


EPI–Hi Harness Diagram

BK 5/12/13



ACCESS COVERS FOR
MATE/DEMATE



LET-1 TELESCOPE
DOUBLE-ENDED APERTURE
SILICON DETECTOR STACK
3- FOILS EACH END

HET TELESCOPE
DOUBLE-ENDED APERTURE
SILICON DETECTOR STACK
2- FOILS EACH END

LET-2 TELESCOPE
SINGLE-ENDED APERTURE
SILICON DETECTOR STACK
3- FOILS ONE END ONLY

EPH-J3
OPERATIONAL HEATER
MWDM-21P

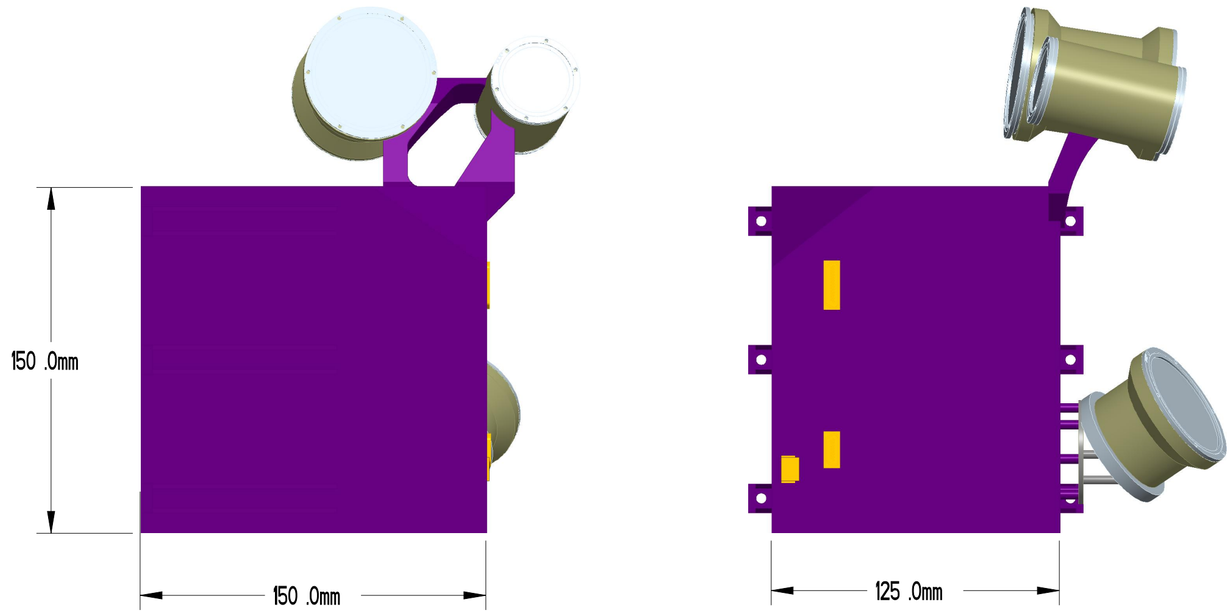
EPH-J2
S/C COMMAND & DATA
MWDM-15S

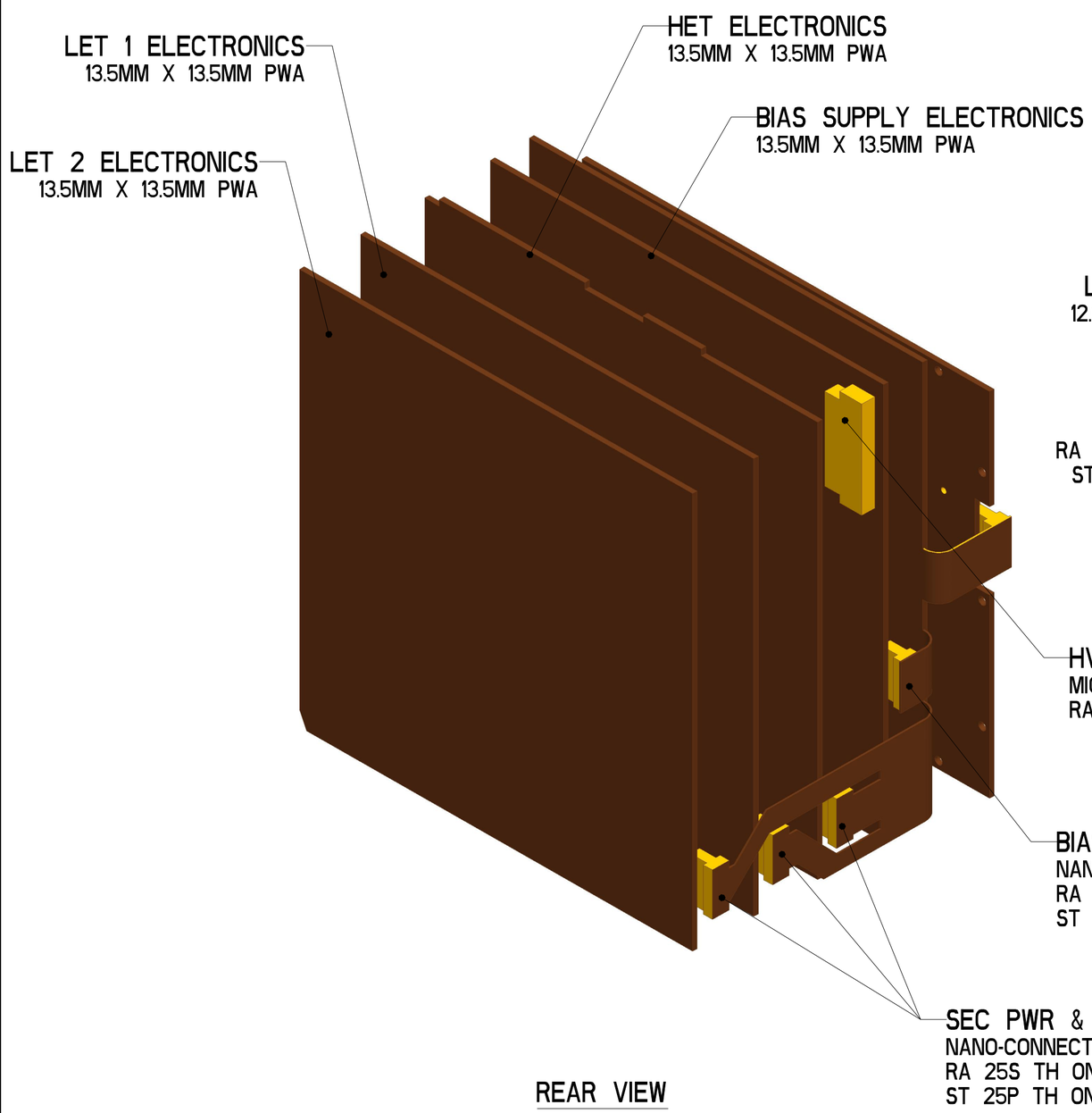
EPI-HI ELECTRONICS
ENCLOSURE- ALUMINUM
6 MOUNTING FEET
MOUNTS TO ISIS BRKT

EPH-J1
S/C POWER
MWDM-9S

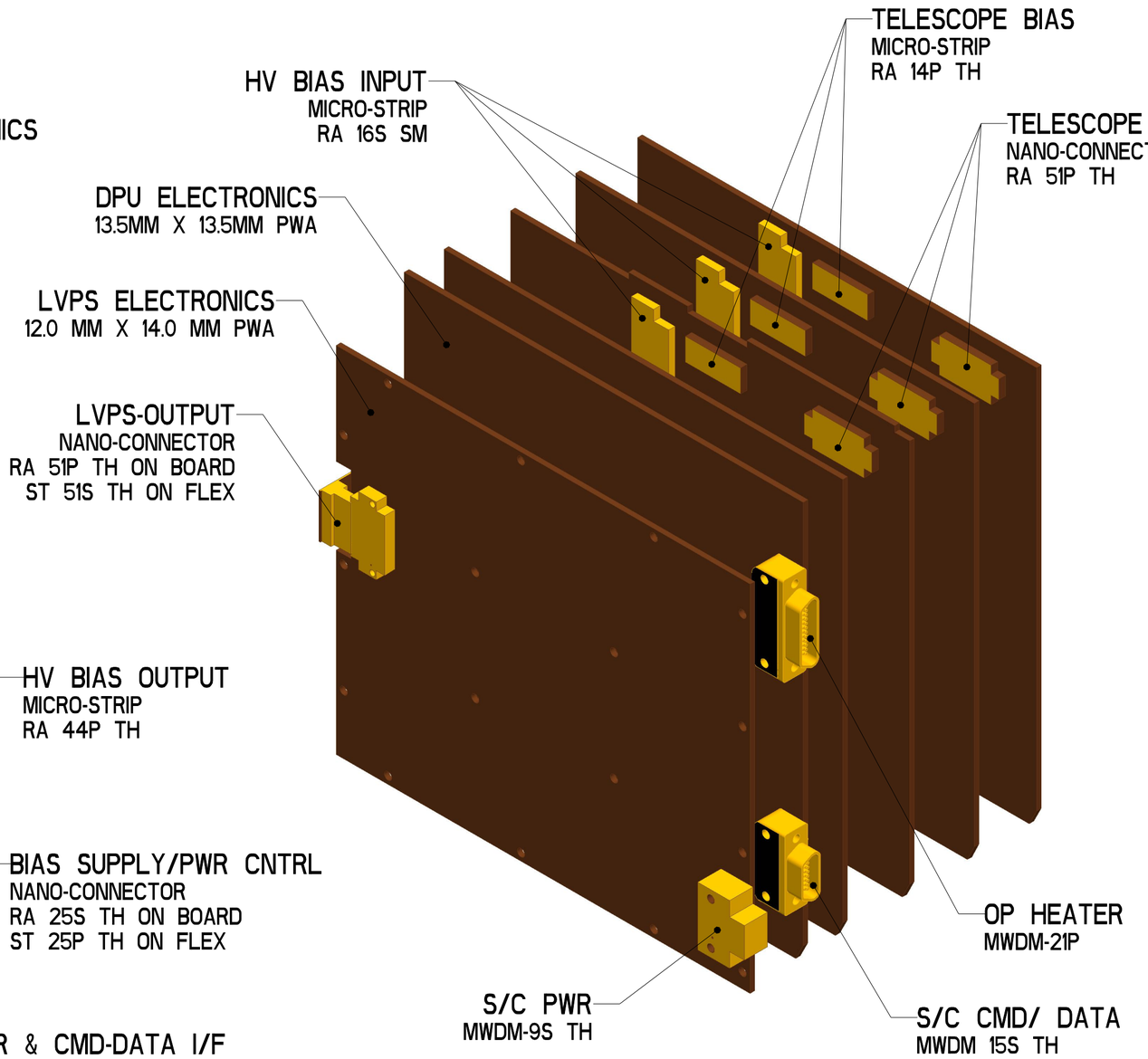
EPI-HI INSTRUMENT CONFIGURATION

09-MAY-2013





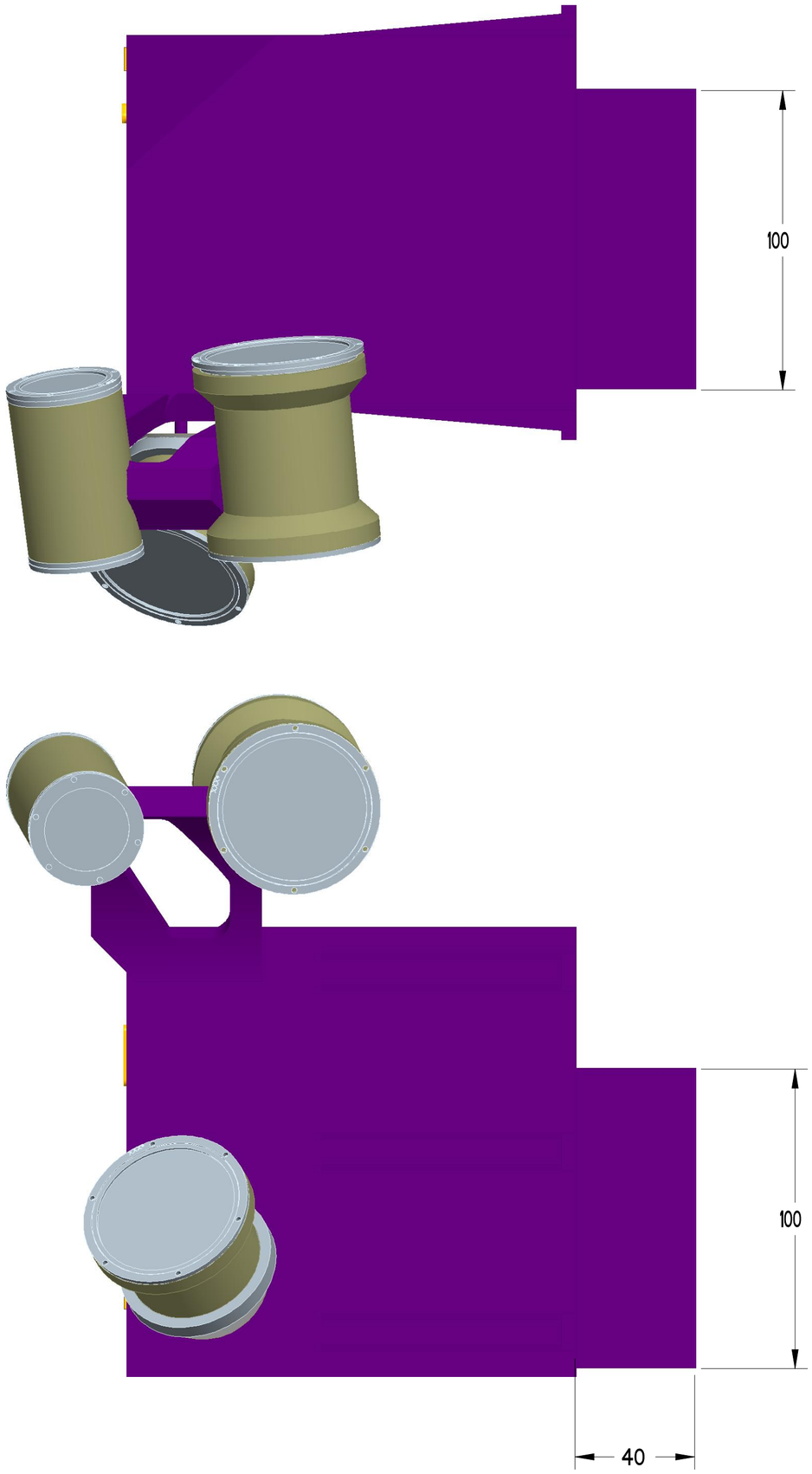
REAR VIEW

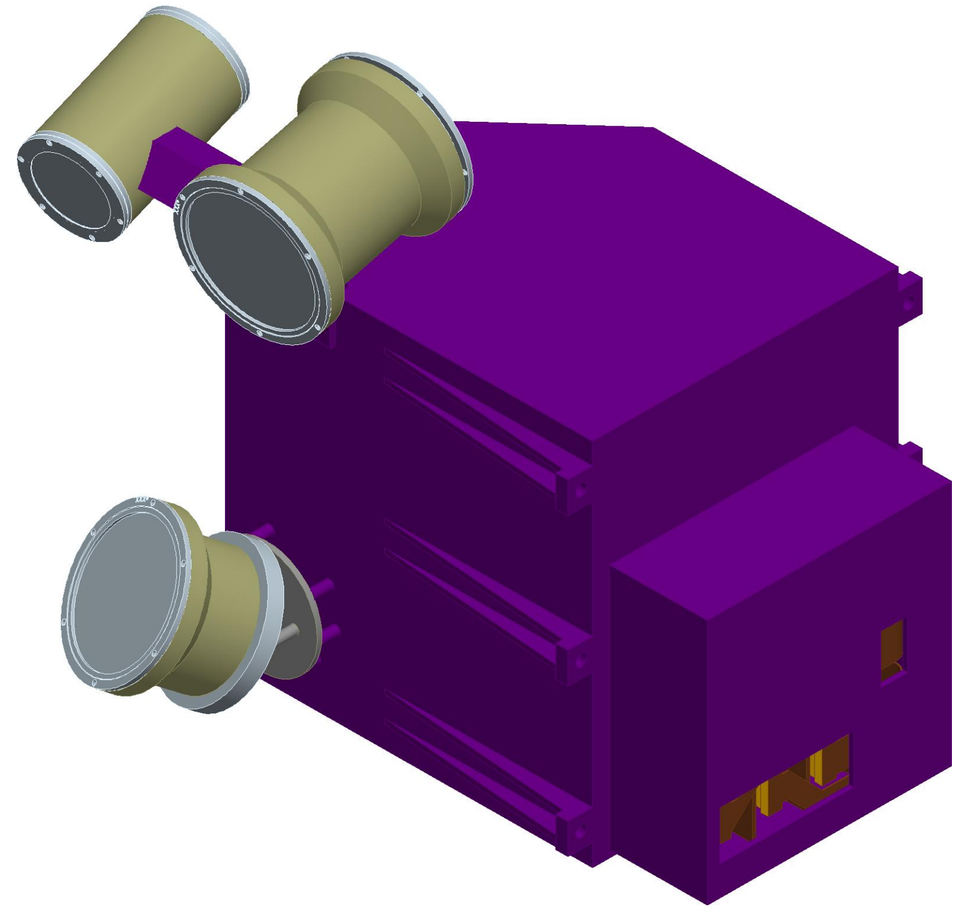


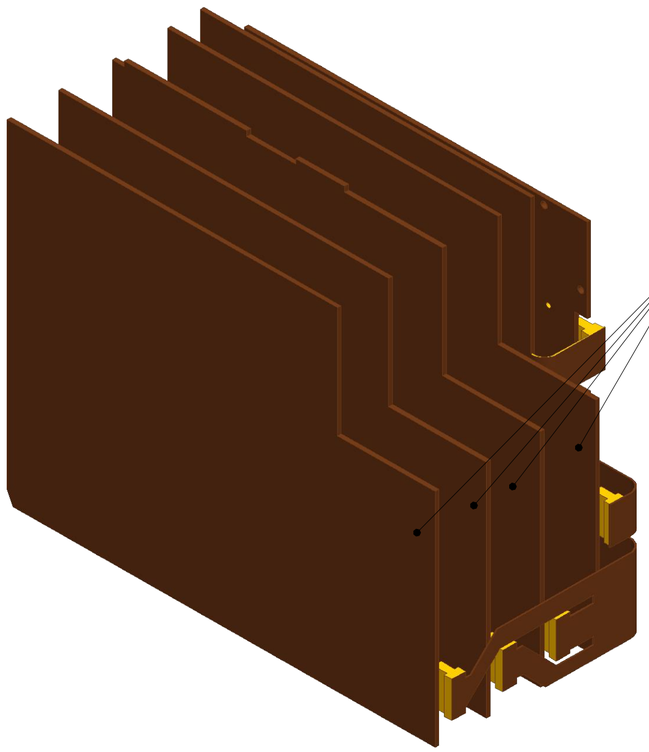
FRONT VIEW

EPI-HI INSTRUMENT CONFIGURATION

09-MAY-2013



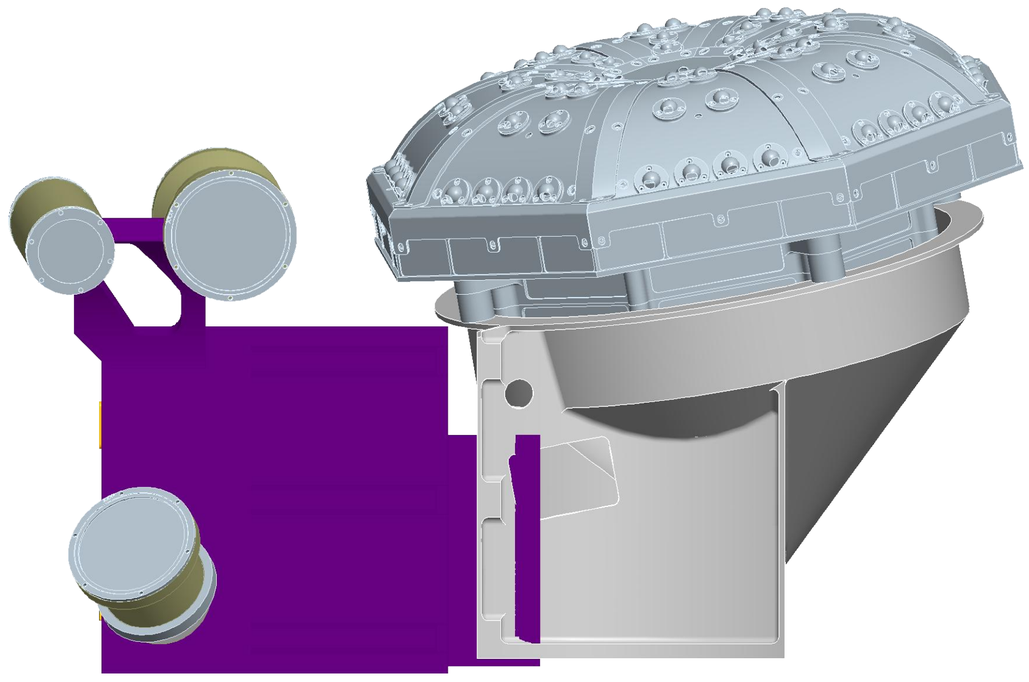


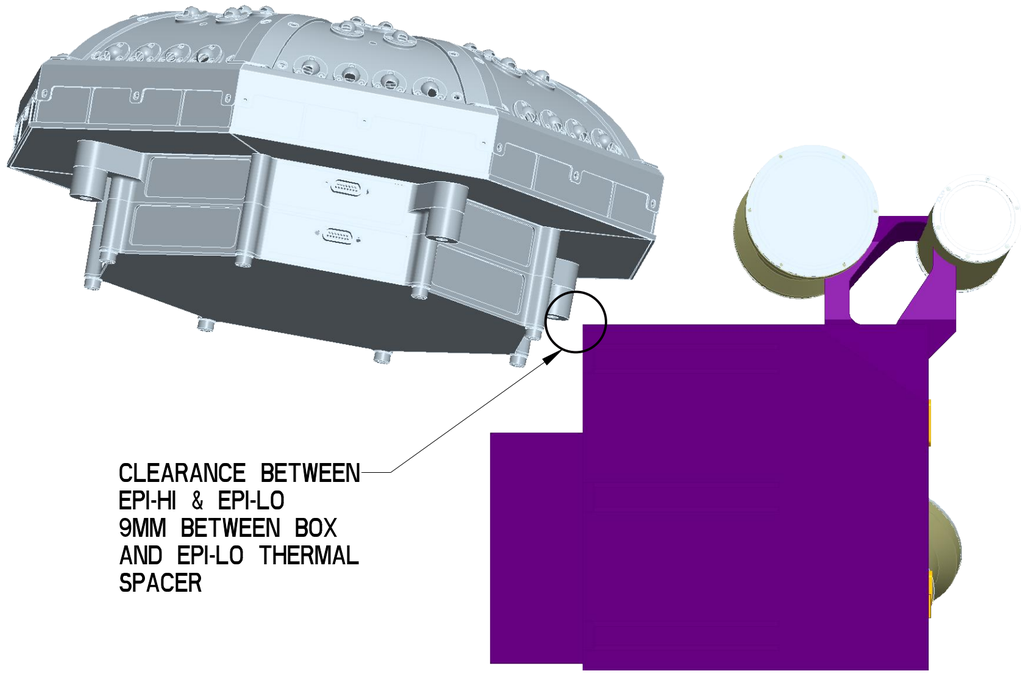


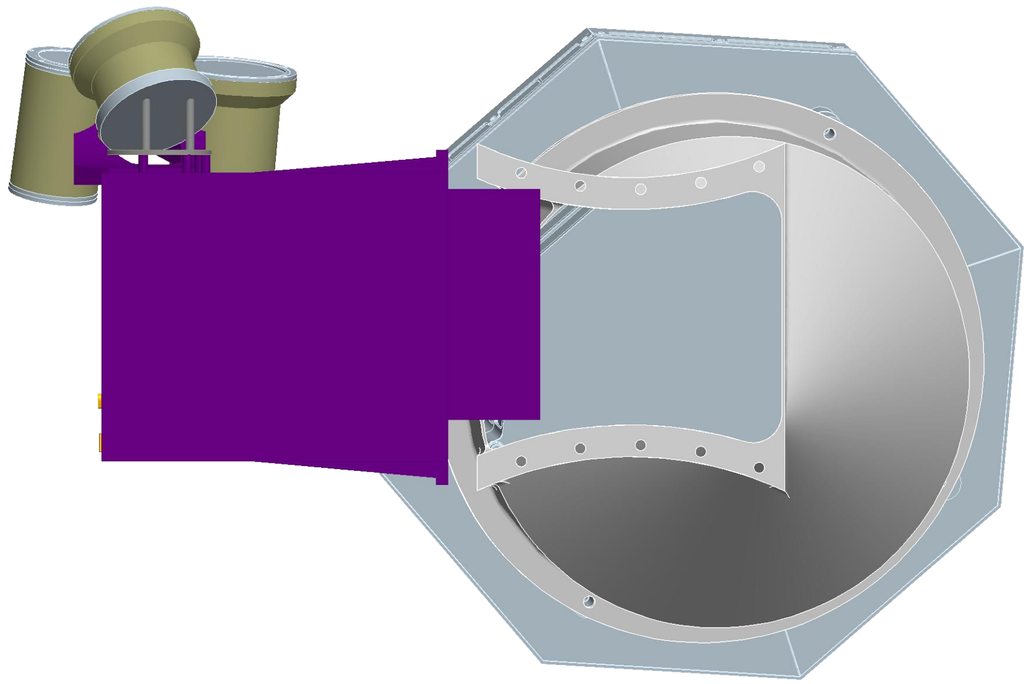
ADDITIONAL 36CM^2 AREA
ON TELESCOPE BDS
& BIAS BOARD

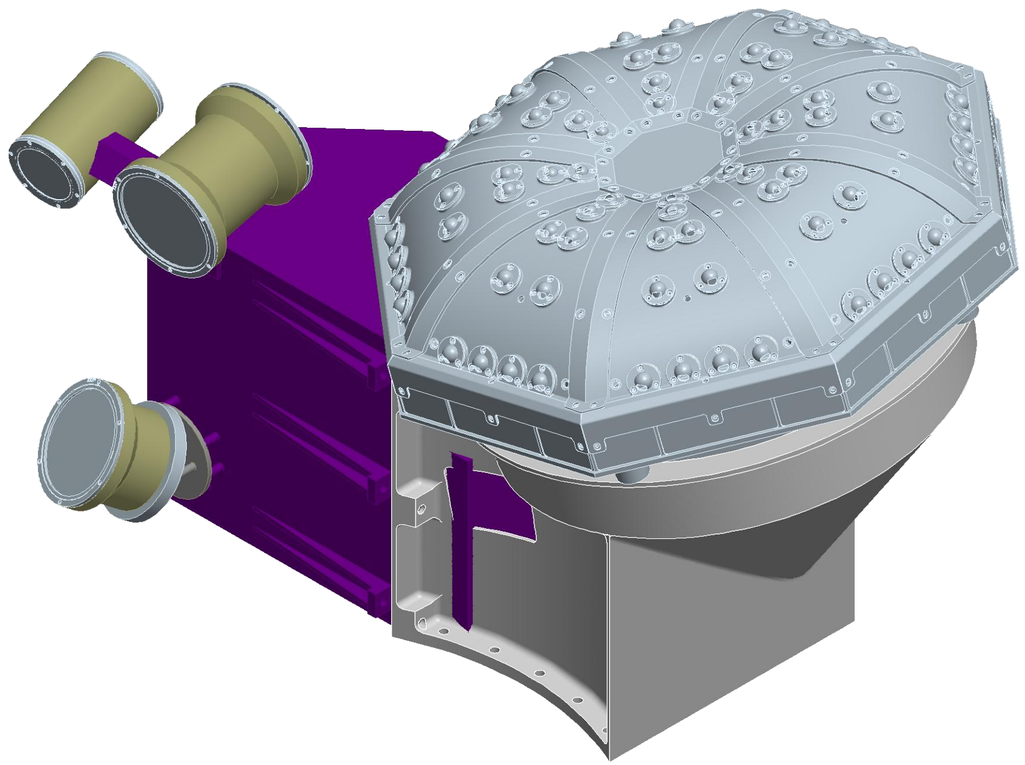
EPI-HI PROPOSED BOARD INCREASE

09-MAY-2013









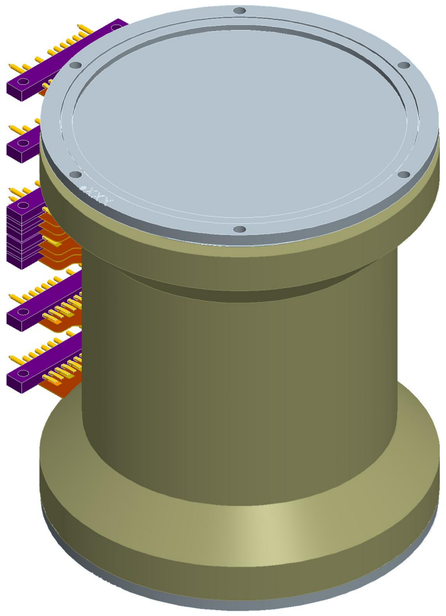
EPI-HI PROPOSED BOARD INCREASE

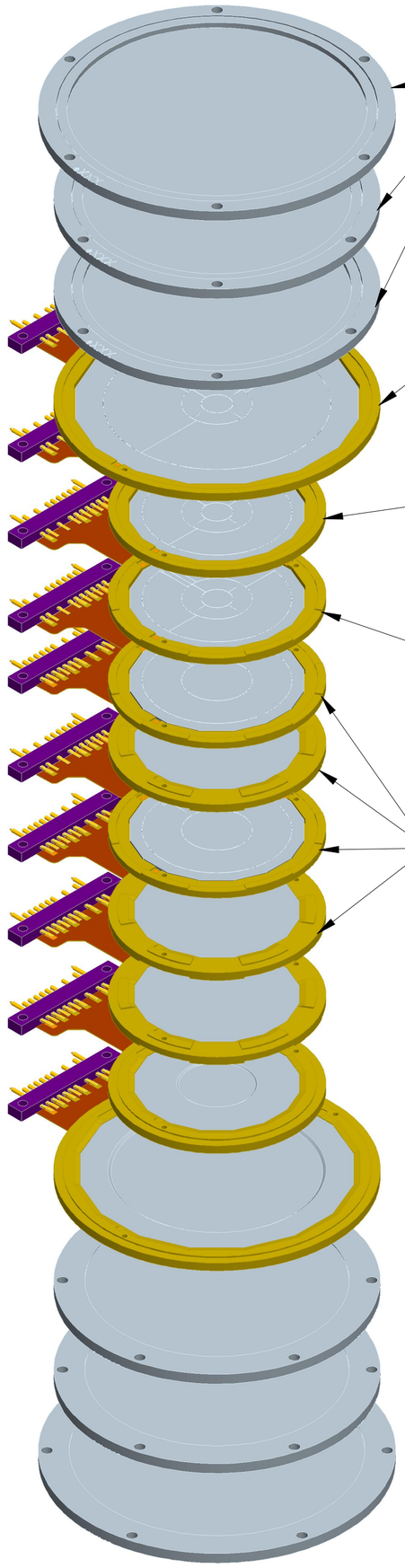
09-MAY-2013

LET TELESCOPE CONFIGURATION 02-MAY-2013

LET 2	LET 1
L0	L0A
L1	L1A
L2	L2A
L3	L3A
L4	L4A
L5	L4B
L6	L3B
	L2B
	L1B
	L0B

DETECTORS BELOW LINE ARE FLIPPED OVER W/ SEGMENTATION FACING REVERSE DIRECTION





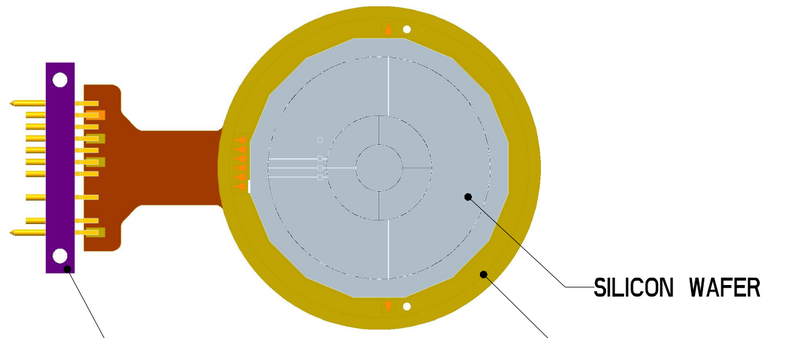
PROTECTIVE FOILS
1.0 MICRON POLYIMIDE OVER
95% OPEN POLYIMIDE MESH
(BOTH ENDS)

L0 DETECTOR
INNER ACTIVE ∅5.0MM X 0.01 THK
SEGMENTED ACTIVE ∅11.3MM X 0.01 THK
OUTER ACTIVE ∅34.0MM X 0.01 THK
HANDLE INACTIVE ∅45.5MM X 0.30 THK

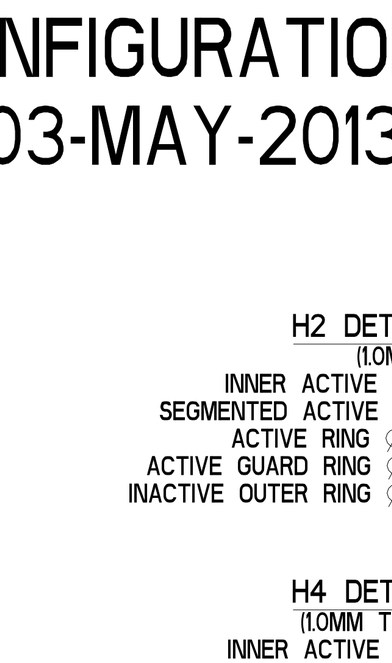
L1 DETECTOR
INNER ACTIVE ∅5.0MM X 0.025MM THK
SEGMENTED ACTIVE ∅11.3MM X 0.025MM THK
HANDLE INACTIVE ∅28.0MM X 0.5MM THK

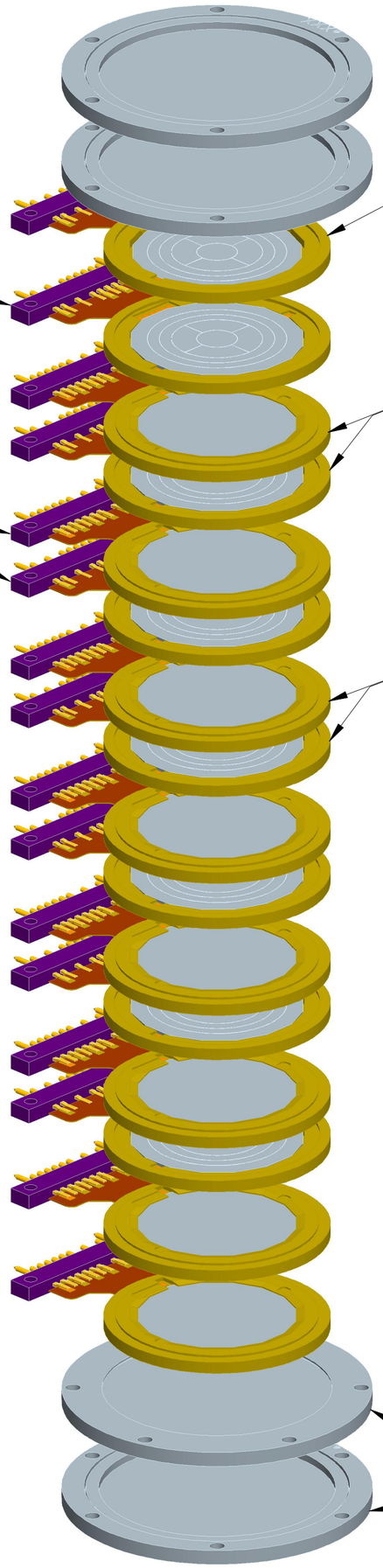
L2 DETECTOR
INNER ACTIVE ∅5.0MM X 0.50MM THK
SEGMENTED ACTIVE OUTER ∅11.3MM X 0.50MM THK
OUTER ACTIVE ∅24.0MM X 0.50MM THK
WAFER INACTIVE OUTER ∅28.00 X 0.50MM THK

L3, L4, L5 & L6 DETECTOR
INNER ACTIVE ∅11.3MM X 1.0MM THK
OUTER ACTIVE ∅24.0MM X 1.0MM THK
WAFER INACTIVE OUTER ∅28.0MM X 1.0MM THK



HET TELESCOPE CONFIGURATION 03-MAY-2013





H1 DETECTOR
(0.5MM THK)
INNER ACTIVE ∅5.0MM
SEGMENTED ACTIVE ∅11.3MM
ACTIVE RING ∅14.3MM
ACTIVE RING ∅17.3MM
INACTIVE OUTER RING ∅21.3MM

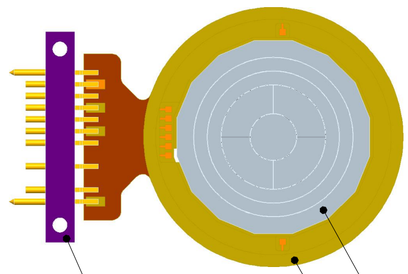
H2 DETECTOR
(1.0MM THK)
INNER ACTIVE ∅5.0MM
SEGMENTED ACTIVE ∅11.3MM
ACTIVE RING ∅14.3MM
ACTIVE GUARD RING ∅17.3MM
INACTIVE OUTER RING ∅21.3MM

H3 DETECTOR
(1.0MM THK X 2)
INNER ACTIVE ∅11.3MM
ACTIVE GUARD RING ∅14.3MM
ACTIVE GUARD RING ∅17.3MM
INACTIVE OUTER RING ∅21.3MM

H4 DETECTOR
(1.0MM THK X 2)
INNER ACTIVE ∅11.3MM
ACTIVE GUARD RING ∅14.3MM
ACTIVE GUARD RING ∅17.3MM
INACTIVE OUTER RING ∅21.3MM

H5 DETECTOR
(1.0MM THK X 2)
INNER ACTIVE ∅11.3MM
ACTIVE GUARD RING ∅14.3MM
ACTIVE GUARD RING ∅17.3MM
INACTIVE OUTER RING ∅21.3MM

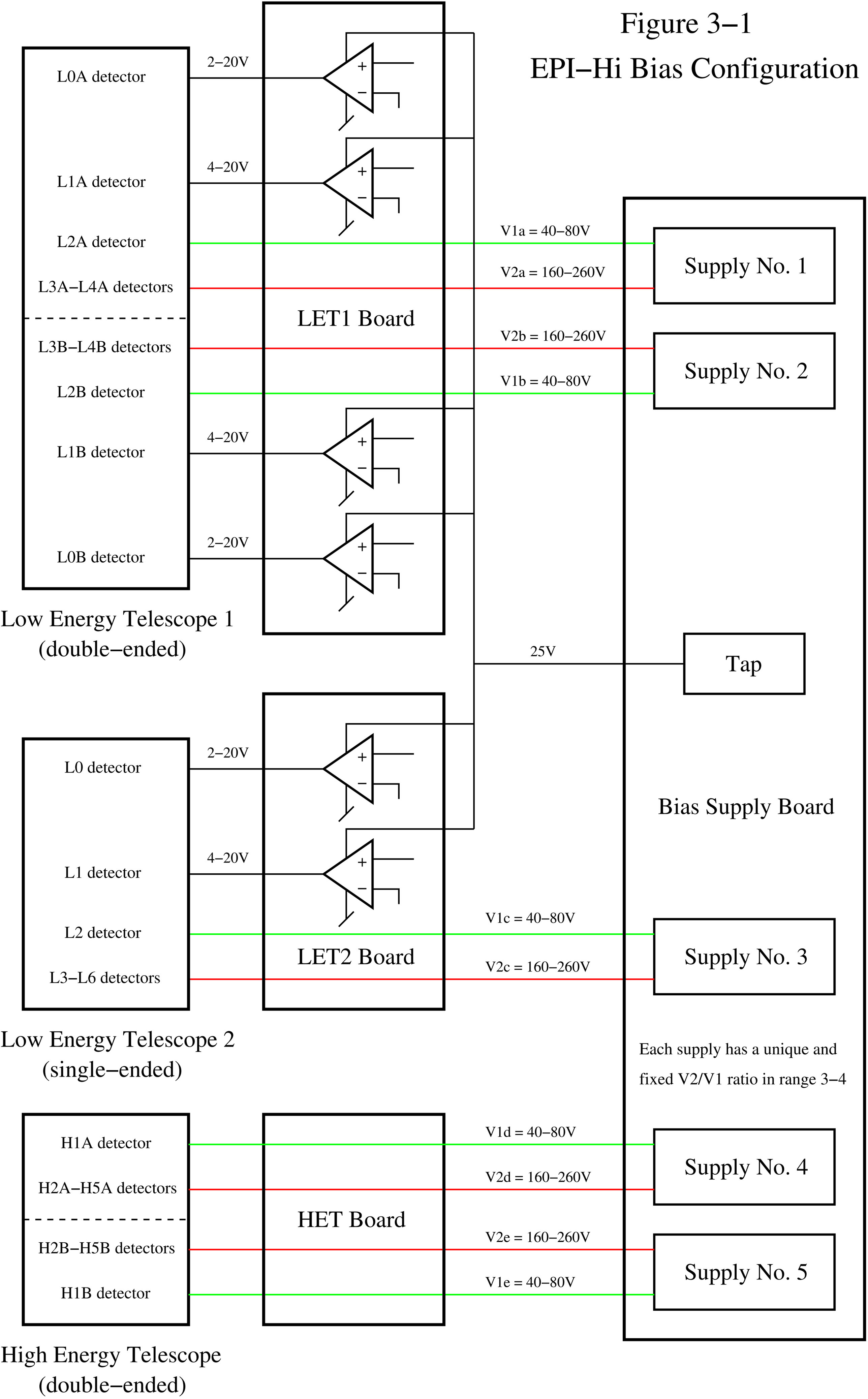
H1A
H2A
H3A1
H3A2
H4A1
H4A2
H5A1
H5A2
H5B2
H5B1
H4B2
H4B1
H3B2
H3B1
H2B
H1B

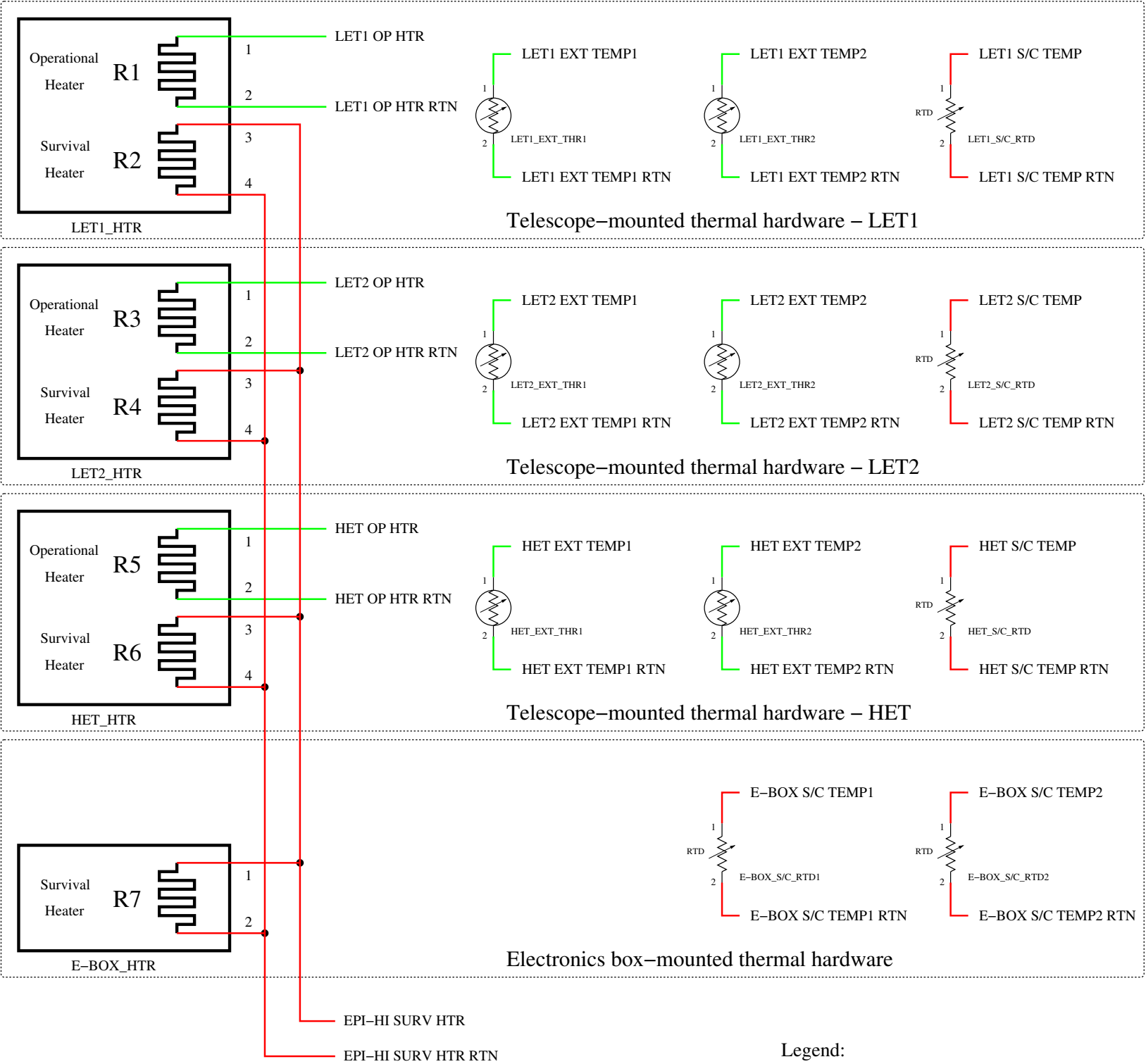


SILICON DETECTOR
RIGID/FLEX MOUNT
GLENAIR MICRO STRIP CONNECTOR

PROTECTIVE FOILS
0.5 MIL KAPTON FOIL
(BOTH ENDS)

Figure 3–1
EPI–Hi Bias Configuration





Legend:

Exterior harness for thermal hardware used in operational heater control.
Terminated by MDM21S connector and mated to EPI−Hi Electronics Box.
Pinout and connector P/N info found in EPI−Hi Harness Spec.
Each operational heater independently software−controlled by EPI−Hi.

Exterior harness for thermal hardware used in survival heater control.
Terminated by MDM9S (survival heater) and MDM15S (S/C RTDs).
Both mated to S/C simulator during EPI−Hi I&T; can be pig−tailed for mating with S/C harness to save mass.
All four survival heaters together software−controlled by S/C (1 switch).

EPI−Hi Thermal Harness Diagram

BK 3/28/13

EPI_Hi_CBE_power_16-BK-worksheet.xlsx

EPI-Hi Power Estimate

8/6/13

8/5/13 17:00	Add min power mode when all PHASIC channels disabled, re-estimate Iq for +5V LDO, Is for +5Vref, HKchip consumption (BK)
7/16/13 11:00	Set LVPS outputs to the target values (BK)
6/27/13 16:00	Updated PHASIC consumption (12mW/ch) (BK)
5/1/13 14:00	Added redundant S/C I/F driver/receiver, and set LVPS outputs to 0.1V above nominal value (BK)
1/25/13 17:00	Updated Bias Supply consumption, added 3 op-heater control switches and the combined op-heater power for all 3 telescopes (BK)
11/15/12 11:00	Reverted rad-hard clock oscillator power to 15mA @ 3.3V with load (in MISC/OSC/SRAM contribution), corrected sourcing of +25V which is from Bias Supply, not LVPS (BK)
11/2/12 19:30	Updated PHASIC consump (11mW/ch) & individual MISC contrib, added rad-hard clock oscillator delta & Hot Case, deleted references to high rates, corrected some equations (BK)
8/1/12 10:06	Fixed regulator power, new op-amps added (JAB)

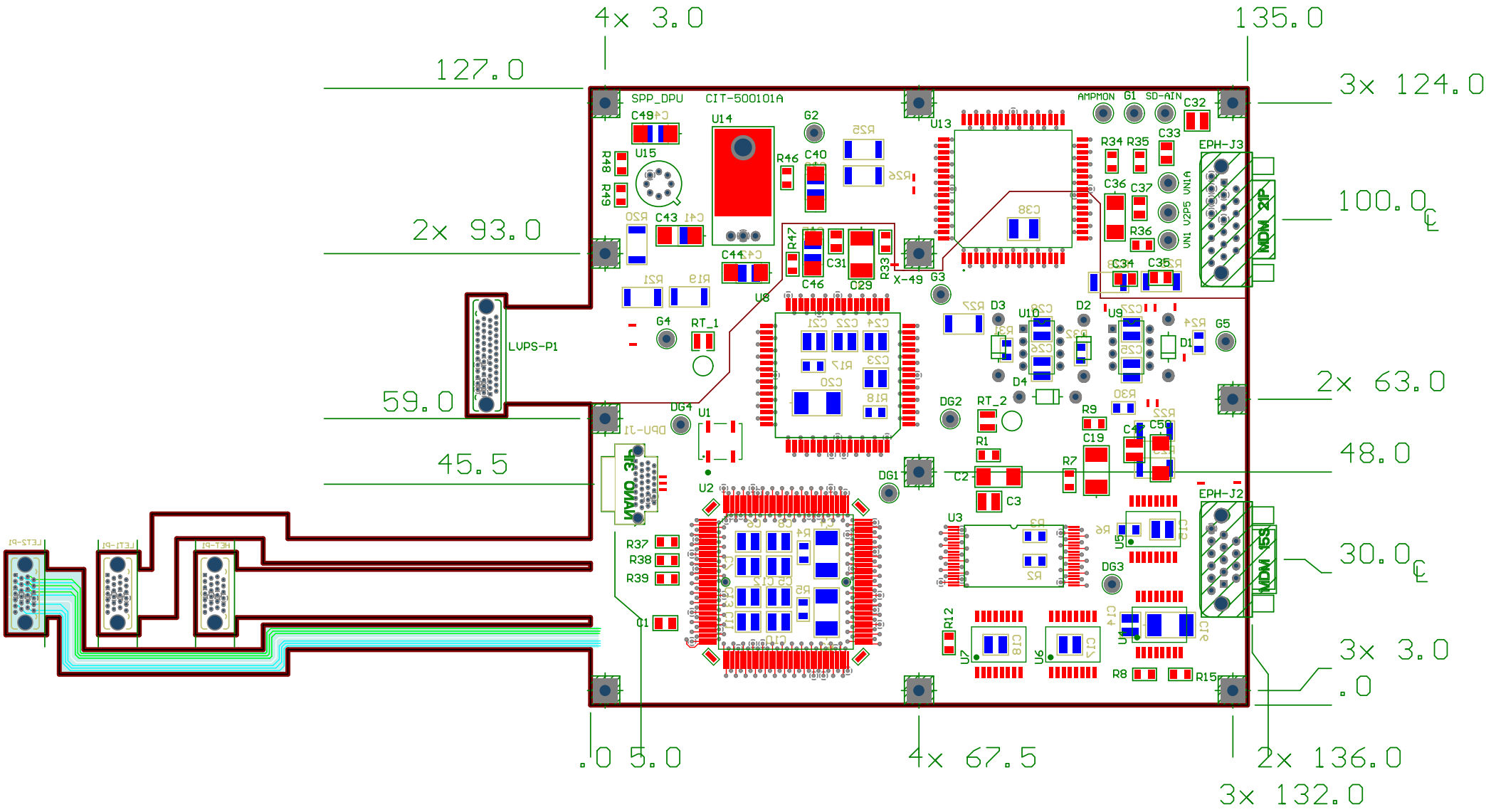
LVPS nominal outputs		Boards ->	HET	LET1	LET2	DPU	BIAS BOL	BIAS EOL	LVPS BOL	LVPS EOL	TOTALS:	BOL Current (mA)	BOL Power (mW)	EOL Current (mA)	EOL Power (mW)
		# PHASICs	3	3	2										
		# channels	36	40	24										
			mA	mA	mA	mA	mA	mA	mA	mA					
+6VA	PHASIC +5VR		101.40	111.00	67.60						6	338.2	2029.0	338.2	2029.0
	P5V post-regulator (Iq)		12.50	13.00	11.00	4.00									
	N5V post-regulator		0.85	0.85	0.85										
	HK chip		1.03	5.03	3.03	6.03									
-6VA	PHASIC N5V		3.30	3.30	2.20						-6	12.6	75.3	12.6	75.3
	N5V post-regulator		0.85	0.85	0.85										
	LV bias (<20V)						0.20	0.20							
	HV bias (40 - 260V)						1.00	1.00							
+12VA	5V precision reference (Is)		1.20	1.20	1.20	1.20					12	16.0	192.4	63.0	756.4
	LV bias (<20V)						1.01	1.01							
	HV bias (40 - 260V)						8.00	55.00							
+3.3VD	MISC/OSC/SRAM		48.00	48.00	48.00	95.00					3.41	287.0	978.7	287.0	978.7
	Interface					30.00									
	MRAM					0.00									
	Op-heater control (3 switches, 50% duty-cycle)					18.00									
+1.5VD	MISC		25.00	25.00	25.00	25.00					1.53	100.0	153.0	100.0	153.0
+1.8VD	SRAM		10.00	10.00	10.00	10.00					1.82	40.0	72.8	40.0	72.8
	+25V from Bias Supply for LV bias			0.71	0.36										
												Min Pwr	Nom Pwr		Peak Pwr
	Secondary power by board (mW)		954.11	1056.46	756.59	618.66	115.38	679.38			Secondary (mW)	1944.2	3501.2		4065.2
	Primary power losses in LVPS (mW)								1500.51	1742.22	Primary (mW)	2777.4	5001.7		5807.4
	Combined op-heater power for all 3 EPI-Hi telescopes per thermal analysis of 11/13/2012 (Trade 12) (mW)											330.0	330.0		330.0
											EPI-Hi total power w/ op-heaters (mW)	3107.4	5331.7		6137.4
	Min Pwr Mode on telescope boards (mW)		396.71	438.46	374.99										
	All PHASIC channels disabled, LDO reg. Iq 5-6 mA														
	Primary power losses in LVPS in Min Pwr Mode (mW)								833.22						

EPI-Hi resources: Mass [g]	**4/27/11**	**6/1/12**	**2/12/13**	**4/5/13**	**8/14/13**	**8/27/13**	
Component	**Baseline**	**Past**	**Past**	**Intermed.**	**Intermed.**	**Present**	Uncertainty
LET1 det. & housing	225	225	225	225	225	225	20%
LET1 electronics	257	238	221	240	258	258	20%
LET1 subtotal:	**482**	**463**	**446**	**465**	**483**	**483**	20%
LET2 det. & housing	145	145	145	145	145	145	20%
LET2 electronics	235	209	190	214	233	233	20%
LET2 subtotal:	**380**	**354**	**335**	**359**	**378**	**378**	20%
HET det. & housing	120	120	120	120	120	120	20%
HET electronics	235	238	221	231	250	250	20%
HET subtotal:	**355**	**358**	**341**	**351**	**370**	**370**	20%
Elec. box & hardware	1091	1000	1050	1100	1335	1335	20%
Shielding	0	0	0	0	0	100	20%
DPU board	279	247	198	197	197	197	20%
Bias Supply	228	228	228	286	354	354	20%
LVPS	292	292	260	260	260	260	20%
Central elec. subtotal:	**1890**	**1767**	**1736**	**1843**	**2146**	**2246**	20%
EPI-Hi subtotal:	**3107**	**2942**	**2859**	**3019**	**3377**	**3477**	20%
Thermal hardware	0	0	50	50	50	50	20%
Thermal blankets	34	34	100	100	100	100	C
EPI-Hi total:	**3141**	**2976**	**3009**	**3169**	**3527**	**3627**	20%

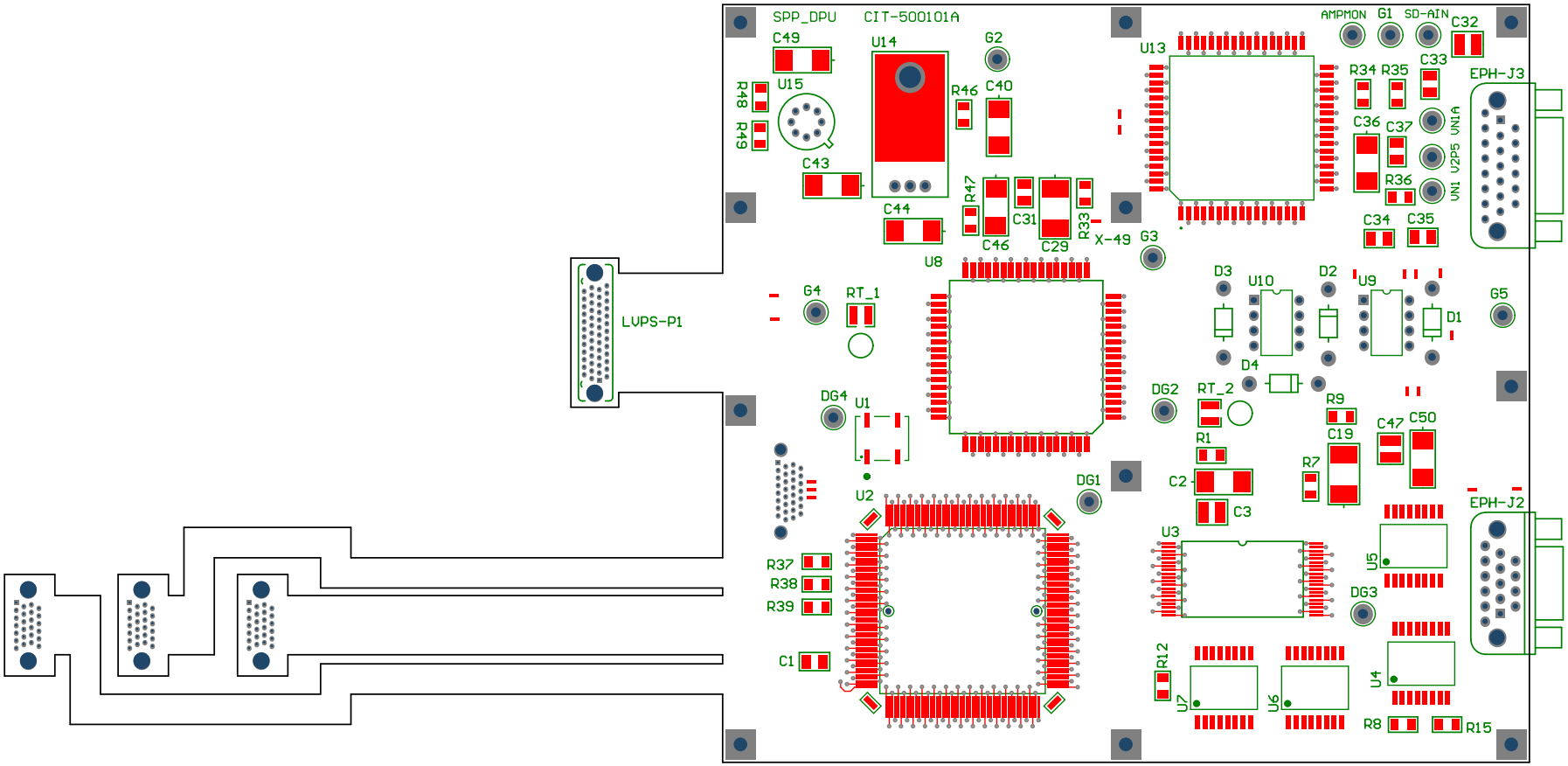
Resource history: Mass [g]	**4/27/11**	**6/1/12**	**2/12/13**	**4/5/13**	**8/14/13**	**8/27/13**	
Component	**Baseline**	**Past**	**Past**	**Intermed.**	**Intermed.**	**Present**	Uncertainty
LET1 det. & housing	225	225	225	225	225	225	20%
Proposal MEL - Rounded up							
2/23/10 MEW memo	225	225	225	225	225	225	C
LET1 electronics	257	238	221	240	258	258	20%
6/18/13 BK update - the requested increase in LET1 board area has been approved by the Project							
5/1/13 BK update - requested 20% increase in LET1 board area for risk reduction (adding 9cm x 4cm extension; 0.51 g/cm2)					18	18	C
4/5/13 BK update - board area 85% populated; comp, staking, conf coat; 0.95 g/cm2				147	147	147	C
4/5/13 BK update - LET1 blank board 13.5cm x 13.5cm; 0.51 g/cm2				93	93	93	C
2/13/13 BK update - board area 80% populated; comp, staking, conf coat; 0.95 g/cm2							C
2/12/13 BK update - LET1 blank board 15cm x 13.5cm; 0.51 g/cm2							C
2/7/13 BK update - board area 90% populated; comp, staking, conf coat; 0.95 g/cm2			139				C
2/7/13 BK update - LET1 blank board 12cm x 13.5cm; 0.51 g/cm2			83				C
5/28/12 BK update w/ HKchip; board area 70% populated; comp, staking, conf coat;		135					C
LET1 has 3 PHASIC hybrids as before							C
5/28/12 BK update - LET1 blank board 15cm x 15cm w/ corner cutout 9cm & 5cm; (		103					C
4/14/11 MEW memo	257						C
2/23/10 MEW memo							C
----------	------	------	------	------	------	------	
LET1 subtotal:	**482**	**463**	**446**	**465**	**483**	**483**	20%
LET2 det. & housing	145	145	145	145	145	145	20%
Proposal MEL - Rounded up							
2/23/10 MEW memo	145	145	145	145	145	145	C
LET2 electronics	235	209	190	214	233	233	20%
6/18/13 BK update - the requested increase in LET2 board area has been approved by the Project							
5/1/13 BK update - requested 20% increase in LET2 board area for risk reduction (adding 9cm x 4cm extension; 0.51 g/cm2)					18	18	C
4/5/13 BK update - board area 70% populated; comp, staking, conf coat; 0.95 g/cm2				121	121	121	C
4/5/13 BK update - LET2 blank board 13.5cm x 13.5cm; 0.51 g/cm2				93	93	93	C
2/13/13 BK update - board area 60% populated; comp, staking, conf coat; 0.95 g/cm2							C
2/12/13 BK update - LET2 blank board 15cm x 13.5cm; 0.51 g/cm2							C
2/7/13 BK update - board area 70% populated; comp, staking, conf coat; 0.95 g/cm2			108				C
2/7/13 BK update - LET2 blank board 12cm x 13.5cm; 0.51 g/cm2			83				C
5/28/12 BK update w/ HKchip; board area 55% populated; comp, staking, conf coat;		106					C
LET2 has 2 PHASIC hybrids as before							C
5/28/12 BK update - LET2 blank board 15cm x 15cm w/ corner cutout 9cm & 5cm; (		103					C
4/14/11 MEW memo	235						C
2/23/10 MEW memo							C
----------	------	------	------	------	------	------	
LET2 subtotal:	**380**	**354**	**335**	**359**	**378**	**378**	20%

HET det. & housing	120	120	120	120	120	120	20%
2/23/10 MEW memo	120	120	120	120	120	120	C
HET electronics	235	238	221	231	250	250	20%
6/18/13 BK update - the requested increase in HET board area has been approved by the Project							
5/1/13 BK update - requested 20% increase in HET board area for risk reduction (adding 9cm x 4cm extension; 0.51 g/cm2)					18	18	C
4/5/13 BK update - board area 80% populated; comp, staking, conf coat; 0.95 g/cm2				139	139	139	C
4/5/13 BK update - HET blank board 13.5cm x 13.5cm; 0.51 g/cm2				93	93	93	C
2/13/13 BK update - board area 80% populated; comp, staking, conf coat; 0.95 g/cm2							C
2/12/13 BK update - HET blank board 15cm x 13.5cm; 0.51 g/cm2							C
2/7/13 BK update - board area 90% populated; comp, staking, conf coat; 0.95 g/cm2			139				C
2/7/13 BK update - HET blank board 12cm x 13.5cm; 0.51 g/cm2			83				C
5/28/12 BK update w/ HKchip; board area 70% populated; comp, staking, conf coat;		135					C
5/28/12 HET now has 3 PHASIC hybrids							C
5/28/12 BK update - HET blank board 15cm x 15cm w/ corner cutout 9cm & 5cm; 0.		103					C
4/14/11 MEW memo (HET has 2 PHASIC hybrids)	235						C
2/23/10 MEW memo (HET has 2 PHASICs)							C
----------	------	------	------	------	------	------	
HET subtotal:	**355**	**358**	**341**	**351**	**370**	**370**	20%
Elec. box & hardware	1091	1000	1050	1100	1335	1335	20%
6/18/13 BK update - the requested increases in E-box size and telescope bracket mass have been approved by the Project							
5/1/13 BK update - requested 100% increase in telescope bracket mass for risk reduction					80	80	C
5/1/13 BK update - requested 20% increase in board area for risk reduction (adding 9cm x 4cm extension) requires more hardware/spacers					30	30	C
5/1/13 BK update - requested 20% increase in board area for risk reduction (adding 9cm x 4cm extension) requires bigger box					125	125	C
4/5/13 BK update - Elec box 14cm x 14cm x 15cm				800	800	800	C
2/11/13 Sandy update - Hardware, spacers, connections			220	220	220	220	C
2/11/13 Sandy update - Telescope brackets			80	80	80	80	C
2/11/13 Sandy update - Elec box 13cm x 14cm x 15cm			750				C
6/1/11 Radiation shielding not needed since PHASIC will be rad-hard		0					C
4/14/11 MEW memo - Hardware	177	177					C
4/14/11 MEW memo - Radiation shielding	91						C
4/14/11 MEW memo - Telescope brackets	58	58					C
4/14/11 MEW memo - Elec box 16cm x 16cm x 10.4cm	765	765					C
Proposal & DPU/LVPS increments - Hardware							C
Proposal & DPU/LVPS increments - Elec box							C
2/23/10 MEW memo - Hardware							C
2/23/10 MEW memo - Elec box							C
2/23/10 MEW memo - Extra Board Area							C
Shielding	0	0	0	0	0	100	20%
8/27/13 Adopted from Project's mass allocation to ISIS						100	C
DPU board	279	247	198	197	197	197	20%
7/8/13 Sandy update - DPU board height reduced by 0.8cm to accommodate chamfer on the E-box; new board dims 13.5cm x 12.7cm							
4/5/13 BK update - board area 60% populated; comp, staking, conf coat; 0.95 g/cm2				104	104	104	C
4/5/13 BK update - DPU blank board 13.5cm x 13.5cm; 0.51 g/cm2				93	93	93	C
2/7/13 BK update - board area 75% populated; comp, staking, conf coat; 0.95 g/cm2			115				C
2/7/13 BK update - DPU blank board 12cm x 13.5cm; 0.51 g/cm2			83				C
5/28/12 BK update w/ HKchip; board area 65% populated; comp, staking, conf coat;		119					C

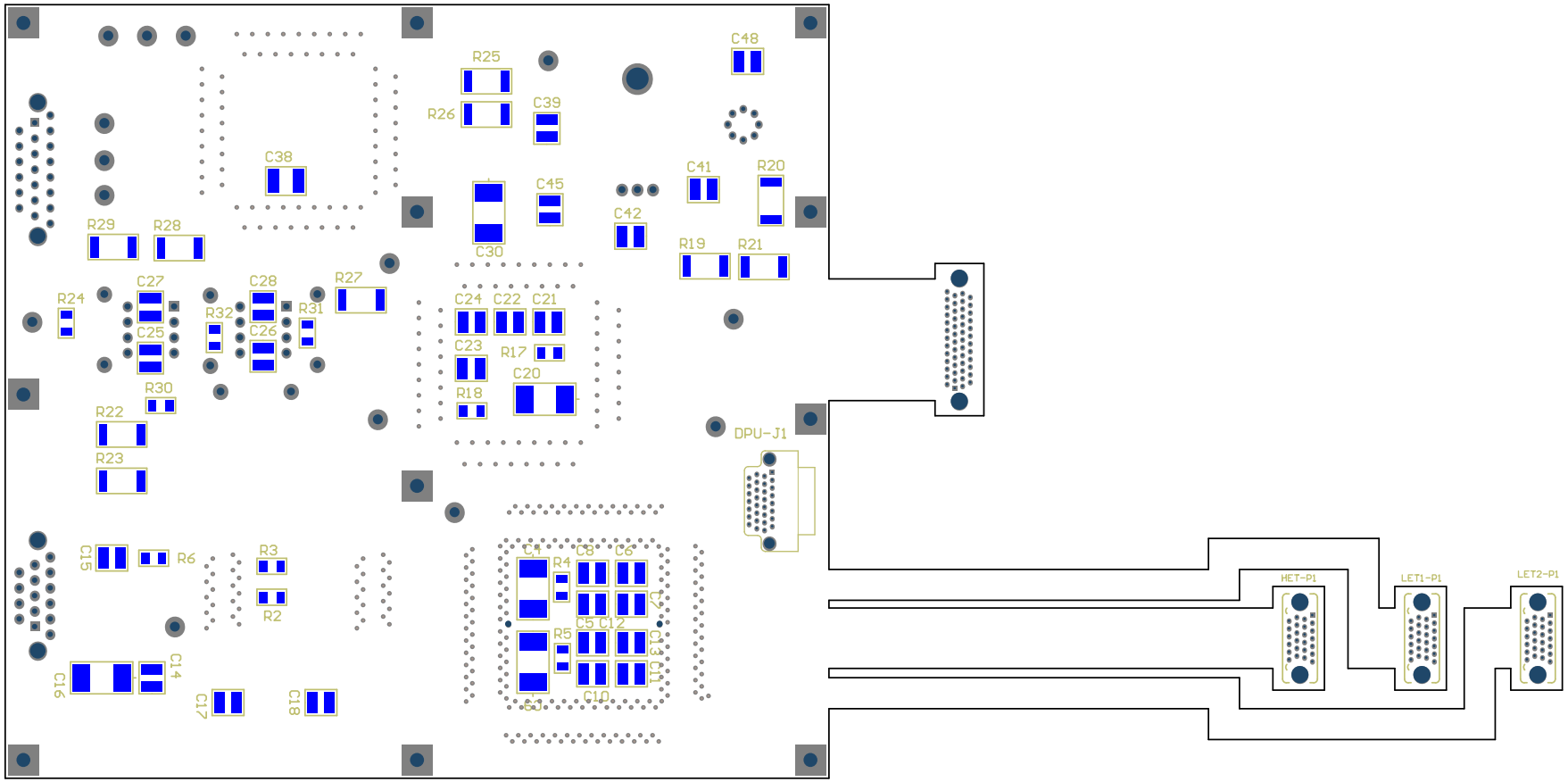
Component area now 4.9" x 3.5" w/ HKchip, which makes 25% reduction							C
DPU board has MDM connector and MCM SRAM		30					C
DPU board has flexi-strip cutouts of approximately 10cm2							C
5/28/12 BK update - DPU blank board 15cm x 15cm w/ corner cutout 9cm & 5cm; 0.		98					C
4/14/11 MEW memo (component area 4.9" x 4.7" per JAB l	279						C
Proposal DPU increment							C
2/23/10 MEW memo							
Bias Supply	228	228	228	286	354	354	20%
6/18/13 BK update - the requested increase in Bias Supply board area has been approved by the Project							
5/1/13 BK update - requested 20% increase in Bias Supply board area for risk reduction (adding 9cm x 4cm extension; 0.51 g/cm2)					18	18	C
5/1/13 BK update - if 20% increase approved, DPU and Bias Supply boards will be swapped in the stack; the latter will need an extra RF shield; both shields will be					130	130	C
5/1/13 Dean Aalami update for RF shield 0.030" thick					54	54	C
4/5/13 Dean Aalami update for board heavily populated; comp, staking, conf coat				127	127	127	C
4/5/13 Dean Aalami update for blank board area 13.5cm x 13.5cm (2.78 g/sq.in)				79	79	79	C
4/5/13 Dean Aalami update for RF shield 0.050" thick				80			C
2/12/13 BK update - Bias Supply blank board 15cm x 13.5cm; 0.51 g/cm2							C
4/14/11 MEW memo - Shield	82	82	82				C
4/14/11 MEW memo - Board	146	146	146				C
Proposal MEL - Board & Shield							C
2/23/10 MEW memo - Shield							C
2/23/10 MEW memo - Board							C
LVPS	292	292	260	260	260	260	20%
7/29/13 Sandy update - LVPS board height reduced by to accommodate chamfer on the E-box; new board dims 14cm x 10.8cm							
2/7/13 Reid Gurnee update - based on similar design and board size for another project			160	160	160	160	C
2/7/13 BK update - estimate for top RF shield			100	100	100	100	C
Proposal LVPS increment	292	292					
2/23/10 MEW memo							
----------	------	------	------	------	------	------	
Central elec. subtotal:	**1890**	**1767**	**1736**	**1843**	**2146**	**2246**	20%
----------	------	------	------	------	------	------	
EPI-Hi subtotal:	**3107**	**2942**	**2859**	**3019**	**3377**	**3477**	20%
Thermal hardware	0	0	50	50	50	50	20%
2/12/13 BK update - estimate for heaters, thermistors, thermal harness			50	50	50	50	C
Thermal blankets	34	34	100	100	100	100	20%
2/7/13 BK update - estimate for all blankets			100	100	100	100	C
4/14/11 MEW memo	34	34	34	34	34	34	C
2/23/10 MEW memo							
----------	------	------	------	------	------	------	
EPI-Hi total:	**3141**	**2976**	**3009**	**3169**	**3527**	**3627**	20%



DPU Board Composite Drawing



DPU Board TOP Layer



DPU Board Bottom Layer

Total MISC I/O available = 115
Total MISC I/O used = 115
53 + 51 + 11 = 115

MISC (53)

address lines (19)
data lines (24)
sram ctrl (2)
parity (7)
clk(1)

PHASIC (51)*

cmd-data-in
cmd-clk-in
token-in
adc-read-sel
cmd-strobe
cmd-reset*
ctr-reset
pha-reset
clg
pha-clk
pha-clk
test-pulse
read-reset
read-clk-in
token-out

gor0-PH0
gor1-PH0
gor2-PH0
lop-PH0
mdn-PH0
gor0-PH1
gor1-PH1
gor2-PH1
lop-PH1
mdn-PH1
gor0-PH2
gor1-PH2
gor2-PH2
lop-PH2
mdn-PH2

data-0
data-1
data-2
data-3
data-4
data-5
data-6
data-7
data-8
data-9
data-10
data-11

data-12
data-13
data-14
data-15
data-16
data-17
data-18
data-21
data-22

**does not include these four signals*
cmd-data-out
pha-reset*
clg*
test-pulse*

DPU I/F & HKchip (11)

DPU I/F (3)

LET1_CMD*
LET1_CMD_ECHO*
LET1_DATA*

HKchip (8)

ADCOUT
ADCCLK
DACCLK
MUXCLK
ADCGO
CMDDATA
CMDSTROBE
PO_RESET*

U1
NC
VCC
GND
OUTPUT
58.8 MHz clock oscillator
QT188L6S-58.8000MHz
C1
0.01uF/100V
CDR32_CC1206
MISC3.3V
CLK_IN

U10
RTAX250SL-CQ208B
Actel/Microsemi
Rad-Tolerant FPGA
RTAX250SL-CQ208B

MD[0..23]
MA[0..20]

LVPS_+1.8V
(10 mA)
R3
2, 1%
RM1206
C2
47uF/10V
CWR09H
C5
0.1uF/50V
CDR33_CC1210
C6
0.1uF/50V
CDR33_CC1210
SRAM1.8V
C3
0.1uF/50V
CDR33_CC1210
C4
0.1uF/50V
CDR33_CC1210

U2
UT8CR512K32
5962R0422701QXC
AEROFLEX
512K x 32-Bit
SRAM
UT8CR512K32
LCQFP-68

R4
10k, 1%
RM1206

LVPS_+1.5V
(25 mA)
R5
1, 1%
RM1206
C7
47uF/10V
CWR09H
C8
0.1uF/50V
CDR33_CC1210
C9
0.1uF/50V
CDR33_CC1210
C10
0.1uF/50V
CDR33_CC1210
C11
0.1uF/50V
CDR33_CC1210

LVPS_+3.3V
(48 mA)
R6
2, 1%
RM1206
C12
47uF/10V
CWR09H
C13
0.1uF/50V
CDR33_CC1210
C14
0.1uF/50V
CDR33_CC1210
C15
0.1uF/50V
CDR33_CC1210
C16
0.1uF/50V
CDR33_CC1210

Approvals	Date	Title
Drawn: B. Keeman	09-06-13	Solar Probe Schematic, LET1 MISC
Checked: J. Burnham		MISC, OSC, SRAM
Approved: Rick Cook		Size: C DWG. No. CIT-500201 Revision: A Sheet 1 of 9
File:		

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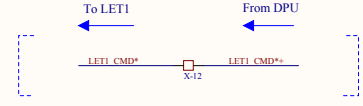
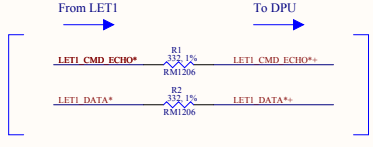
I/F to DPU





Approvals	Date	Title	*Solar Probe*				
Drawn: B. Kecman	09-06-13		***Schematic, LET1 DPU I/F***				
Checked: J. Burnham			*Interface to DPU*				
Approved: Rick Cook		Size: C	DWG. No. CIT-500201	Revision: A	Sheet 2 of 9		
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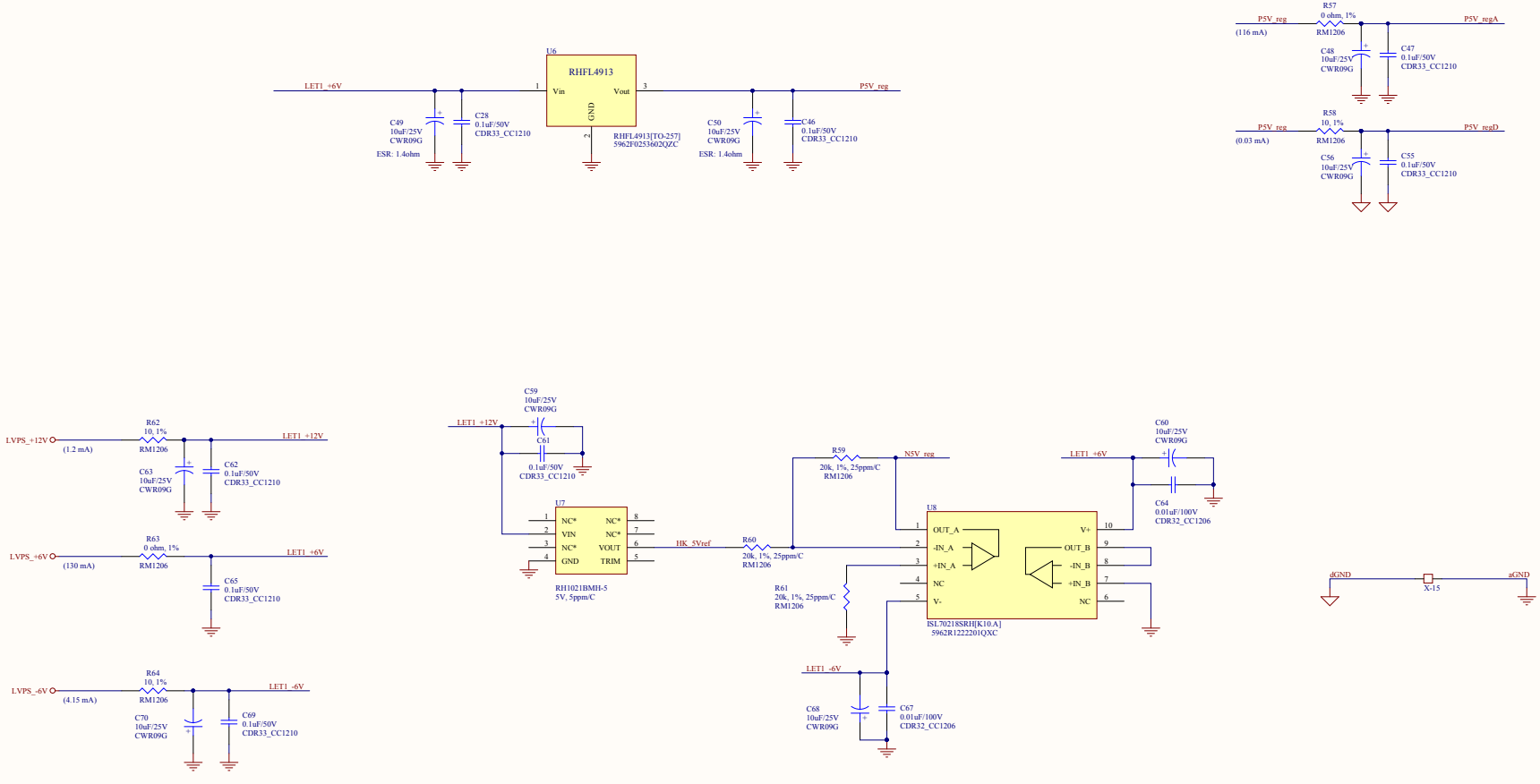

Approvals	Date	Title	
Drawn: B. Keeman	09-06-13	Solar Probe Schematic, LET1 REG Regulators	
Checked: J. Burnham			
Approved: Rick Cook		Size: C	DWG. No. CIT-500201 Revision: A Sheet 3 of 9
File:			

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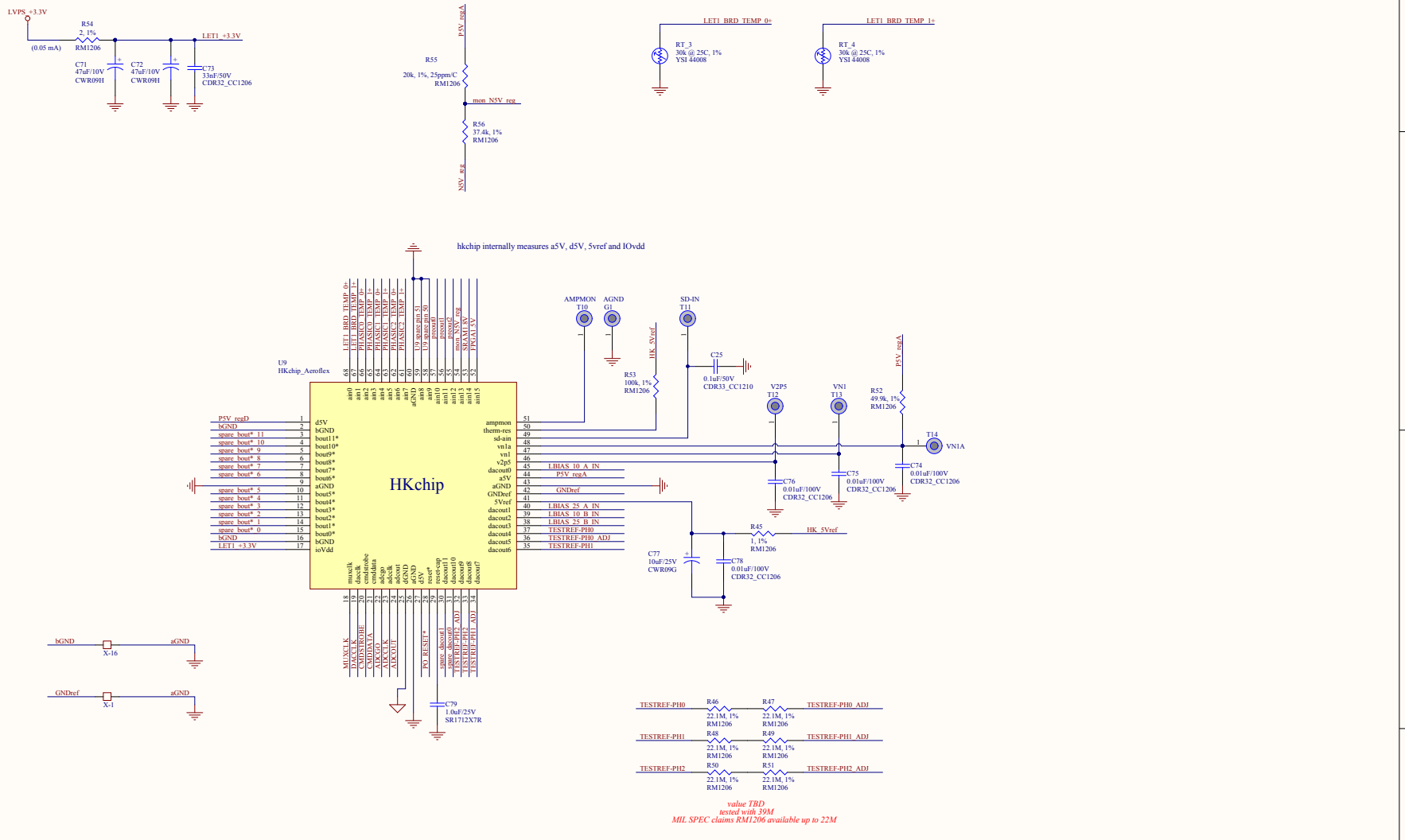

Approvals	Date	Title	
Drawn: B. Kecman	09-06-13	Solar Probe Schematic, LET1 HKchip	
Checked: J. Burnham		Housekeeping ASIC	
Approved: Rick Cook		Size: C DWG. No. CIT-500201 Revision: A Sheet 4 of 9	
File:			

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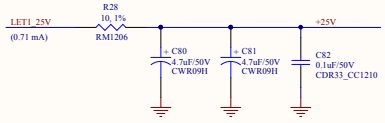
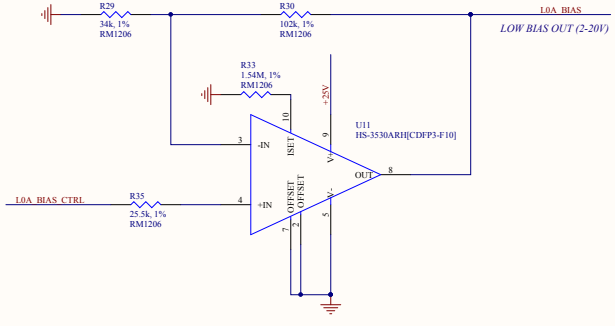
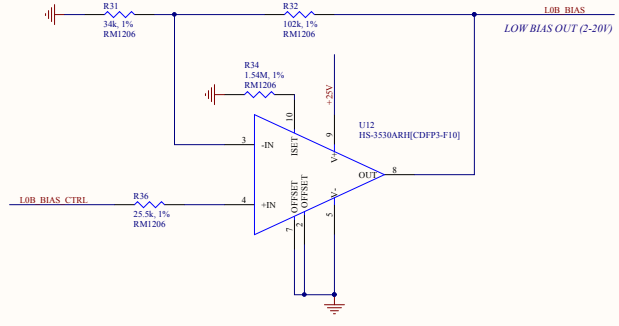
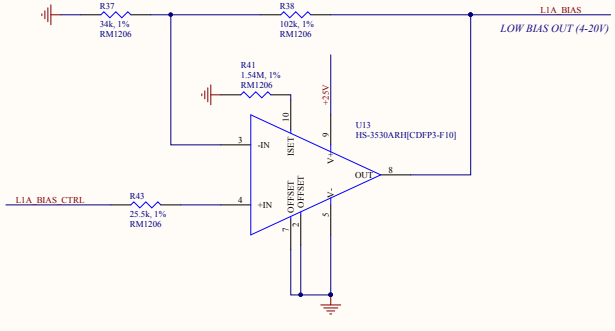
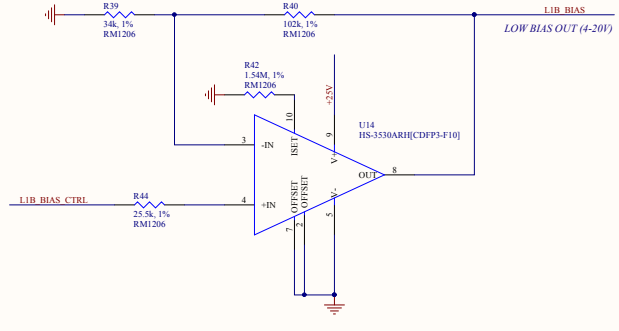


currently set all low bias for gain =4 i.e. 0-20V out









Approvals	Date	Title	Solar Probe Plus / EPI-Hi / LET1 Board
Drawn: B. Keeman	09-06-13		Schematic, LET1 Low Bias
Checked: J. Burnham			Low Detector Bias Voltages
Approved: Rick Cook		Size: C	DWG. No. CIT-500201 Revision: A Sheet 5 of 9
File:			

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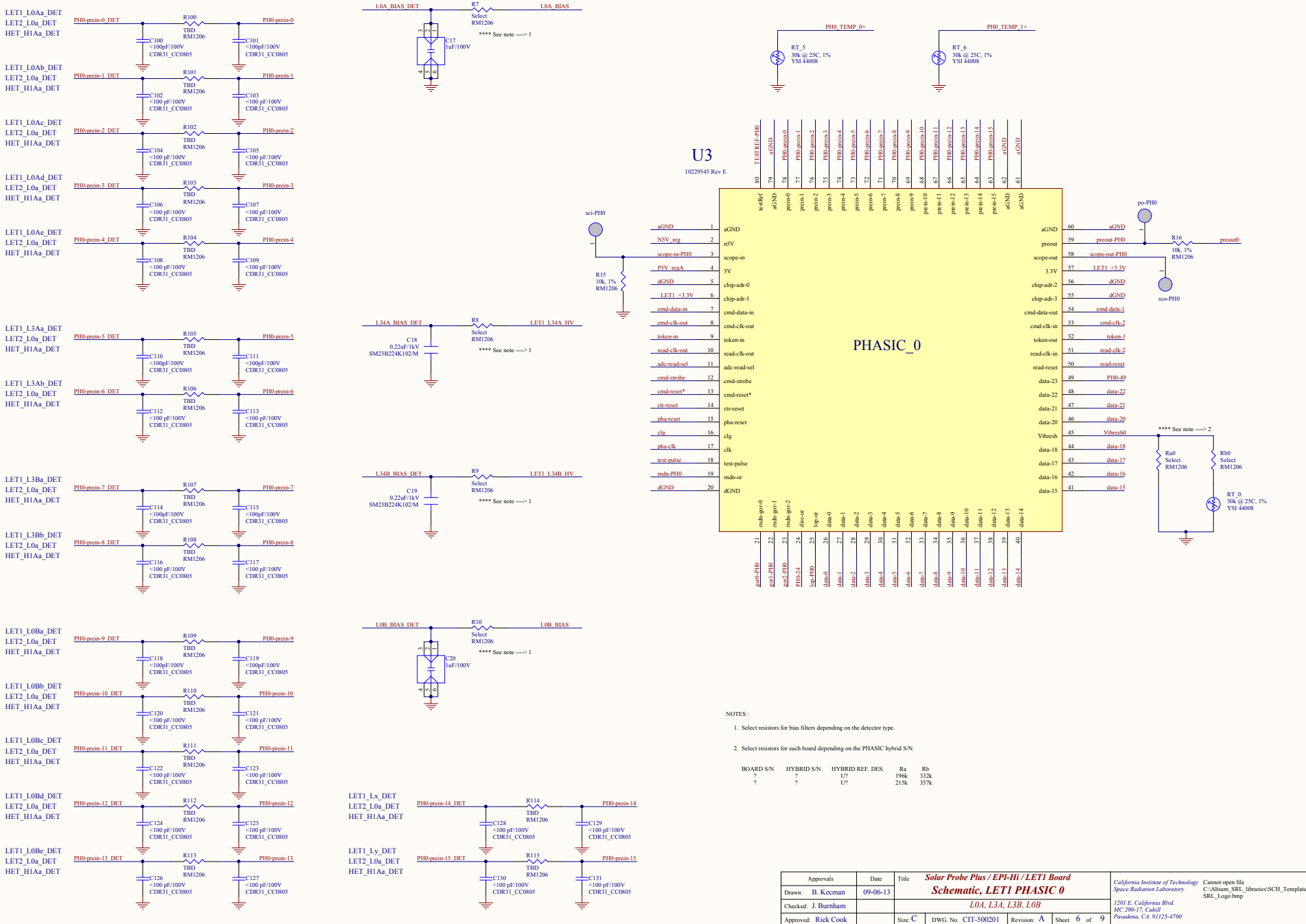

NOTES :

1. Select resistors for bias filters depending on the detector type.

2. Select resistors for each board depending on the PHASIC hybrid S/N.

BOARD S/N	HYBRID S/N	HYBRID REF. DES.	Ra	Rb
?	?	U?	196k	332k
?	?	U?	215k	357k

Approvals	Date	Title
Drawn: B. Keeman	09-06-13	Solar Probe Plus / EPI-Hi / LET1 Board
Checked: J. Burnham		Schematic, LET1 PHASIC 0
Approved: Rick Cook		L0A, L3A, L3B, L0B

Size: C | DWG. No. CIT-500201 | Revision: A | Sheet 6 of 9

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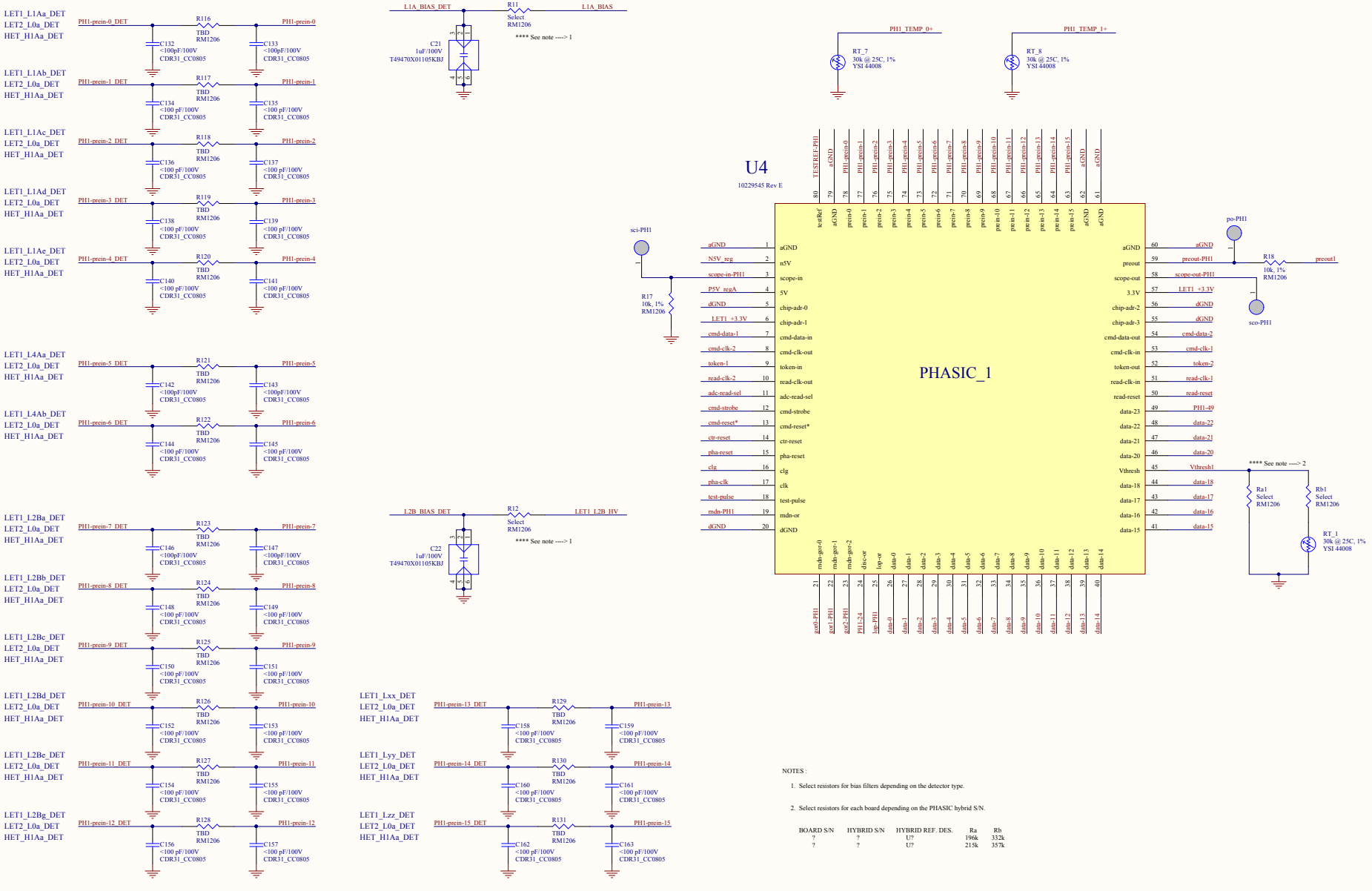

NOTES :

1. Select resistors for bias filters depending on the detector type.

2. Select resistors for each board depending on the PHASIC hybrid S/N.

BOARD S/N	HYBRID S/N	HYBRID REF. DES.	Ra	Rb
?	?	U?	196k	332k
?	?	U?	215k	357k

Approvals	Date	Title	
Drawn: B. Keeman	09-06-13	*Solar Probe Plus / EPI-Hi / LET1 Board*	
Checked: J. Burnham		*Schematic, LET1 PHASIC 1*	
Approved: Rick Cook		*L1A, L4A, L2B*	
File:		Size: C	DWG. No. CIT-500201 Revision: A Sheet 7 of 9

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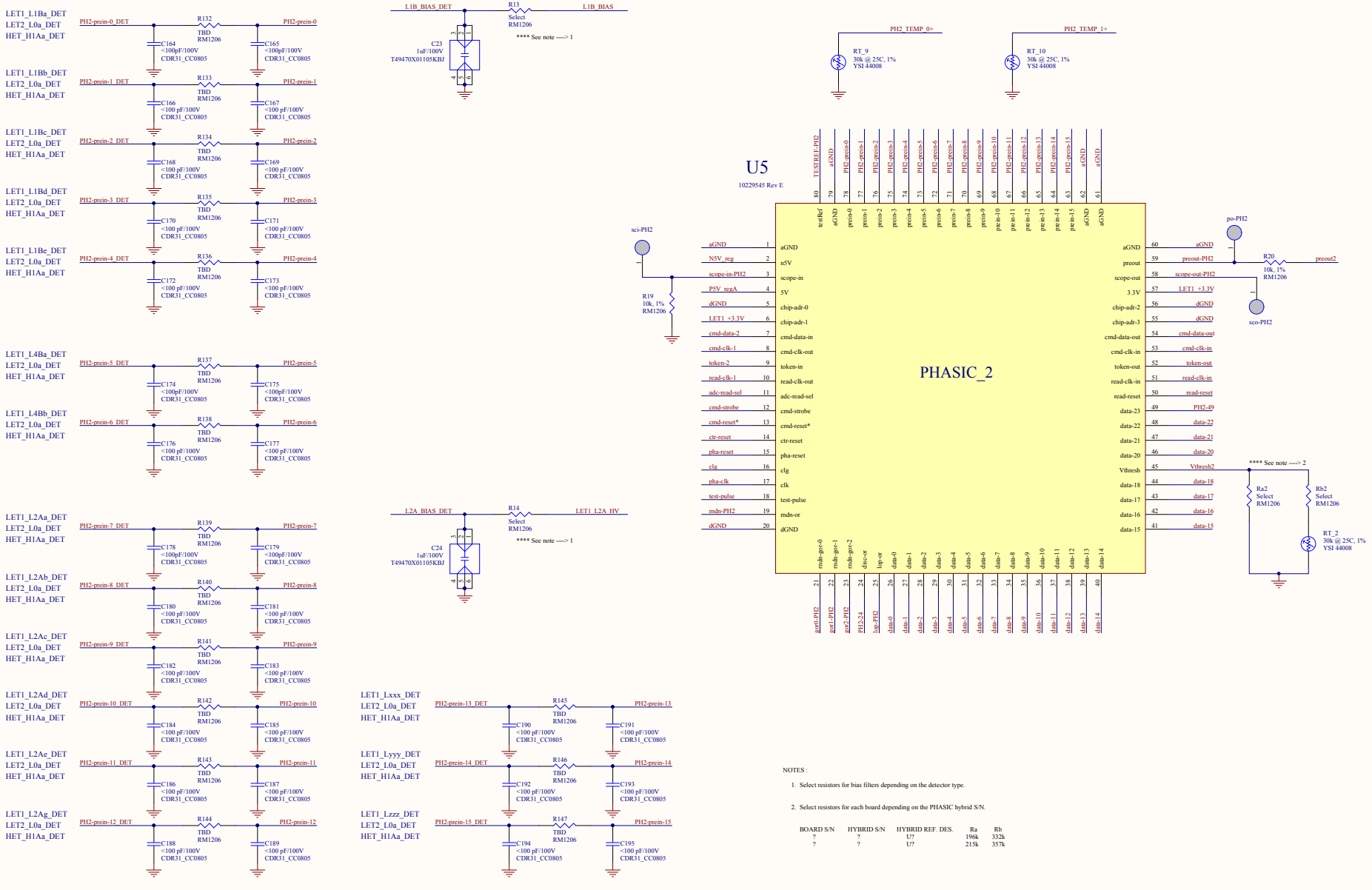

NOTES :

1. Select resistors for bias filters depending on the detector type.

2. Select resistors for each board depending on the PHASIC hybrid S/N.

BOARD S/N	HYBRID S/N	HYBRID REF. DES.	Ra	Rb
?	?	U?	196k	332k
?	?	U?	215k	357k

Approvals	Date	Title	
Drawn: B. Kecman	09-06-13	Solar Probe Plus / EPI-Hi / LET1 Board	
Checked: J. Burnham		Schematic, LET1 PHASIC 2	
Approved: Rick Cook		L1A, L4A, L2B	
File:		Size: C DWG. No. CIT-500201 Revision: A Sheet 8 of 9	

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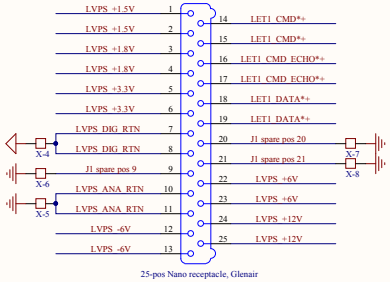
DPU interface

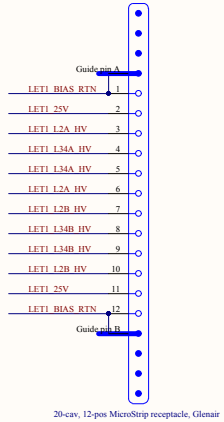
LET1-J1



25-pos Nano receptacle, Glenair
891-009-25SA2-BRT1T-429

Bias Supply interface

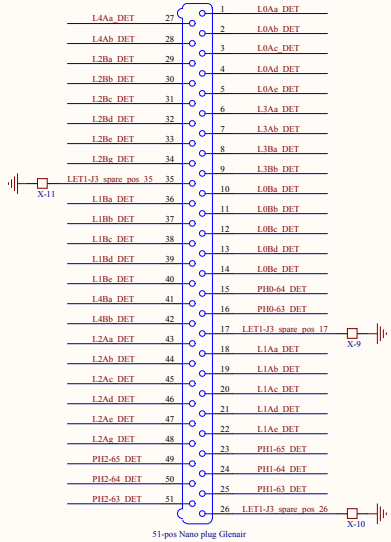
LET1-J2



20-cav, 12-pos MicroStrip receptacle, Glenair
171-008-20S-PBMH-429*

Telescope signal interface

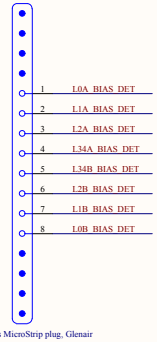
LET1-J3



51-pos Nano plug Glenair
891-008-51PA2-BRT1T-429

Telescope bias interface

LET1-J4



16-cav, 8-pos MicroStrip plug, Glenair
171-008-16P-PBMH-429

Approvals	Date	Title	
Drawn: B. Keeman	09-06-13	*Solar Probe Plus / EPI-Hi / LET1 Board*	
Checked: J. Burnham		***Schematic, LET1 Connectors***	
Approved: Rick Cook		*Connectors*	
File:		Size: C / DWG. No. CIT-500201 / Revision: A / Sheet 9 of 9	

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Bill of Materials, SPP LET1 Board, Assy P/N CIT-500203A 9/6/13

Item	Comment	Description	Procurement P/N	Footprint	Quantity
1	Connector	16-cav, 8-pos MicroStrip plug, Glenair	171-008-16P-PBMH-429	16P-SMD	1
2	Connector	20-cav, 12-pos MicroStrip recept, Glenair	171-008-20S-PBMH-429*	20S-SMD	1
3	Connector	25-position Nano receptacle, Glenair	891-009-25SA2-BRT1T-429	25S-Nano TH	1
4	Connector	51-position Nano plug, Glenair	891-008-51PA2-BRT1T-429	51P-Nano TH	1
5	UT8CR512K32	Aeroflex SRAM 512K x 32, 16M	5962R0422701QXC	CQFP-68	1
6	TBD <100pF/100V	Capacitor, CDR31, 5%, 100V	CDR31BP??DetNet??	CDR31_CC0805	96
7	33nF/50V	Capacitor, CDR32, 10%, 50V	CDR32BX333AKUS	CDR32_CC1206	1
8	0.01uF/100V	Capacitor, CDR32, 10%, 100V	CDR32BX103BKUS	CDR32_CC1206	7
9	0.1uF/50V	Capacitor, CDR33, 10%, 50V	CDR33BX104AKUS	CDR33_CC1210	22
10	47uF/10V	Capacitor, CWR09, 10%, 10V	CWR09FC476KCB	CWR09H	5
11	10uF/25V	Capacitor, CWR09, 10%, 25V	CWR09KC106KCB	CWR09G	10
12	4.7uF/50V	Capacitor, CWR09, 10%, 50V	CWR09NC475KCB	CWR09H	2
13	0.22uF/1kV	Ceramic HV capacitor	SM23B224K102/M	SM23	2
14	HKchip_Aeroflex	Housekeeping Chip	TBD	CQFP-68	1
15	ISL70218SRH[K10.A]	Intersil, Radhard Dual Rail-to-Rail Opamp	5962R1222201QXC	ISL70218[K10.A]	1
16	HS-3530ARH	Intersil, Radhard, Rail-to-Rail Op Amp	5962F9568701QXC	CDFP3-F10	4
17	PHASIC_0, 1, 2	PHASIC Hybrid	10229545 Rev E	Kovar QFP-80	3
18	5V, 5ppm/C	Precision 5V Reference	RH1021BMH-5	8-pin can	1
19	1.0uF/25V	Presidio, Cap, Ceramic, 1.0uF, 10%, 25V	SR1712X7R105K1NT95#M123	CC1712	1
20	1uF/100V	Presidio High Voltage CAP, 1uF/100V	T49470X01105KBJ	J-CASE-5	6
21	58.8 MHz clock oscillator	Q-Tech Rad-hard Crystal Oscillator	QT188L6S-58.8000MHz	QT188[SOJ-4]	1
22	RHFL4913[TO-257]	Rad-hard, +5V, Fixed Voltage Regulator	5962F0253602QZC	TO-257	1
23	20k, 1%, 25ppm/C	Resistor, RM, 1%, 25ppm/C, 250mW	D55342E07B20E0S	RM1206	4
24	0 ohm, 1%	Resistor, RM, 1%, 100ppm/C, 250mW	M32159B07M	RM1206	2
25	1, 1%	Resistor, RM, 1%, 100ppm/C, 250mW	D55342K07B1D00S	RM1206	2
26	1.54M, 1%	Resistor, RM, 1%, 100ppm/C, 250mW	D55342K07B1F54S	RM1206	4
27	10, 1%	Resistor, RM, 1%, 100ppm/C, 250mW	D55342K07B10D0S	RM1206	4
28	100k, 1%	Resistor, RM, 1%, 100ppm/C, 250mW	D55342K07B100ES	RM1206	1
29	102k, 1%	Resistor, RM, 1%, 100ppm/C, 250mW	D55342K07B102ES	RM1206	4
30	10k, 1%	Resistor, RM, 1%, 100ppm/C, 250mW	D55342K07B10E0S	RM1206	7
31	2, 1%	Resistor, RM, 1%, 100ppm/C, 250mW	D55342K07B2D00S	RM1206	3
32	22.1M, 1%	Resistor, RM, 1%, 100ppm/C, 250mW	D55342K07B22F1S	RM1206	6
33	25.5k, 1%	Resistor, RM, 1%, 100ppm/C, 250mW	D55342K07B25E5S	RM1206	4
34	332, 1%	Resistor, RM, 1%, 100ppm/C, 250mW	D55342K07B332DS	RM1206	2
35	34k, 1%	Resistor, RM, 1%, 100ppm/C, 250mW	D55342K07B34E0S	RM1206	4
36	37.4k, 1%	Resistor, RM, 1%, 100ppm/C, 250mW	D55342K07B37E4S	RM1206	1
37	49.9k, 1%	Resistor, RM, 1%, 100ppm/C, 250mW	D55342K07B49E9S	RM1206	1
38	Select	Resistor, RM, 1%, 100ppm/C, 250mW	D55342K07??BiasFilter??	RM1206	8
39	Select	Resistor, RM, 1%, 100ppm/C, 250mW	D55342K07B??Vthresh??	RM1206	6
40	TBD	Resistor, RM, 1%, 100ppm/C, 250mW	D55342K07B??DetNet??	RM1206	48
41	RTAX250SL-CQ208B	RTAX250 FPGA, 115 user I/Os	RTAX250SL-CQ208B	CQFP-208	1
42	30k @ 25C, 1%	Thermistor, 30k @ 25C, 1%	S311P18-09S7R6	2-pin SMD	11