9Sept13EPI-Hi_PeerReview

Monday, September 09, 2013
11:01 AM

DPU Peer Review
Attendees: Kecman, Burnham, Dickinson, Weidner, Angold, Ken Erickson, Bill Crain

Bill: avoid large dead/non-active areas; can lead to surface leakage
- Guard rings around active pixels helps
- Perhaps take up later in the review
- **Caltech AI: provide mask for review**
- Is there a field plate in the detectors from Micron?
- Runaway, over-time with bias, can be a problem w/Micron detectors
- Field plate was added to avoid this
- **Caltech AI: describe detector screening and what they will do to avoid leakage**

Bill: concerns with rigid flex through coupon testing (made by Advanced Circuits, Circuit Express, Accurate)
- **Caltech AI: Leave adequate time for coupon testing**
  - Can do coupon testing on EM boards
- NASA publishes a list of good PCB vendors

Bill: concerned with pulling socketed FPGAs off FM boards
Bill: Recommends 33Ohm resistor on every FPGA I/O
- Can be 0402

Bill: consider putting 1.5V supply right next to FPGAs
- Consider performing a Hyperlynx Analysis

Bill AI: Provide information as to whether or not this will be a concern for SPP
Provide details of Aerospace Actel Lifetime testing configuration
Requirement on Actel FPGA Core: 1.425 - 1.575V
Dickinson AI: Take this up with Rick Conde:
- Does Actel require 33 Ohm series resistor on every I/O?
- Does the FPGA core regulation have to be at the FPGA
- Is a Hyperlynx analysis required

Weidner: Is there a ceramic capacitor next to every power supply pin on the FPGA
- **Caltech AI: Provide demonstration of this; 0.1 uF ceramic**

Weidner: Is simultaneous switching (adjacent pins) a problem
- Could be mitigated by Hyperlynx analysis

[Dickinson] Caltech AI: Provide series resistor at all clock drivers; consider snubber termination at source
Dickinson AI: Double check the control signal termination scheme matches HIS/EPI-Lo
- EPI-Lo pulls up ZZ signal as well; otherwise, the same

[Dickinson] Caltech AI: Provide information on MRAM memory mapping in MISC
[Weidner] Caltech AI: Terminate unused inputs to the drivers (U6,U5)
Caltech AI: Move the brackets on sheet 3 on the right
[Weidner] Caltech AI: Add series resistors on LVDS inputs
[Dickinson] Caltech AI: Justify brown-out conditions for HK POR function
- Is there a hole in the architecture that could make us vulnerable to brown-out conditions?

Does the LVPS need to be monitoring all core voltages to make sure they are disabled if they go out of spec? Consider POR circuit for 1.5V core also.

Dickinson AI: Explore the power-supply sequencing/monitoring problem with LVPS; avoid failure modes

What happens with the Actel when the core voltage drop?

[Bill] Caltech AI: Clocks need to be stable XX amount of time prior to CPU operation

Perform an analysis - required at CDR

Bill: Preliminary number for FPGA utilization

Caltech AI: Prepare FPGA, memory, code utilization numbers for PDR

[Brief absence of Weidner, Dickinson, Angold]

Caltech AI: Check on the full range of the current monitor provided by the LVPS

HK Chip: 35 input mux

[Weidner] Caltech AI: Consider high-side switching on the operational heaters

Also ensures the heater is never a large floating conductor

It is safer to route ground around the instrument; with high-side, heater is always grounded when not in use (better for DDD)

Caltech to recall justification of low-side switching

Actions from EPI-Hi Telescope boards review: Caltech 09/09/13

Caltech AI: provide detector noise analysis and worst case threshold/noise ratios.
Provide expected livetime vs. deadtime

Caltech AI: evaluate (by CDR) the need to use LVDS on data line from telescope to DPU.

Caltech AI: investigate potential case of a failure in one telescope causing failure in others.

Bill AI: provide details of regulator with FPGAs that resulted in no failures over millions of hours of testing.

Caltech AI: change R61 resistor value from 20k ohm to 10k ohm.

Caltech AI: Are we implementing autonomous of balancing of the leakage current? If so, provide a description.

Caltech AI: consider connecting HV bias bypass capacitor to pre-amp 5V rather than to ground

Caltech AI: provide table 3 in PHASIC handbook.

Caltech AI: after low noise setup is complete, do we meet the 0.2% crosstalk spec and under what input and threshold conditions?