EPI Hi bias supply review

I wanted to give you my analysis of the EPI Hi bias supply.

Some simulations have been included below for your reference.

# Oscillator

The “oscillator” section of the supply schematic is shown in Figure 0‑1 below. The “oscillator” does not appear to oscillate on its own in SPICE simulations. A SPICE model schematic of the circuit is shown in Figure 0‑2. Refer to the results of the simulation plotted in Figure 0‑3. It shows that the “oscillator” output to the primary MOSFET switch (orange circle) does not do anything unless the sync signal is present (red circle).



Figure ‑ EPI Hi bias supply “oscillator” schematic

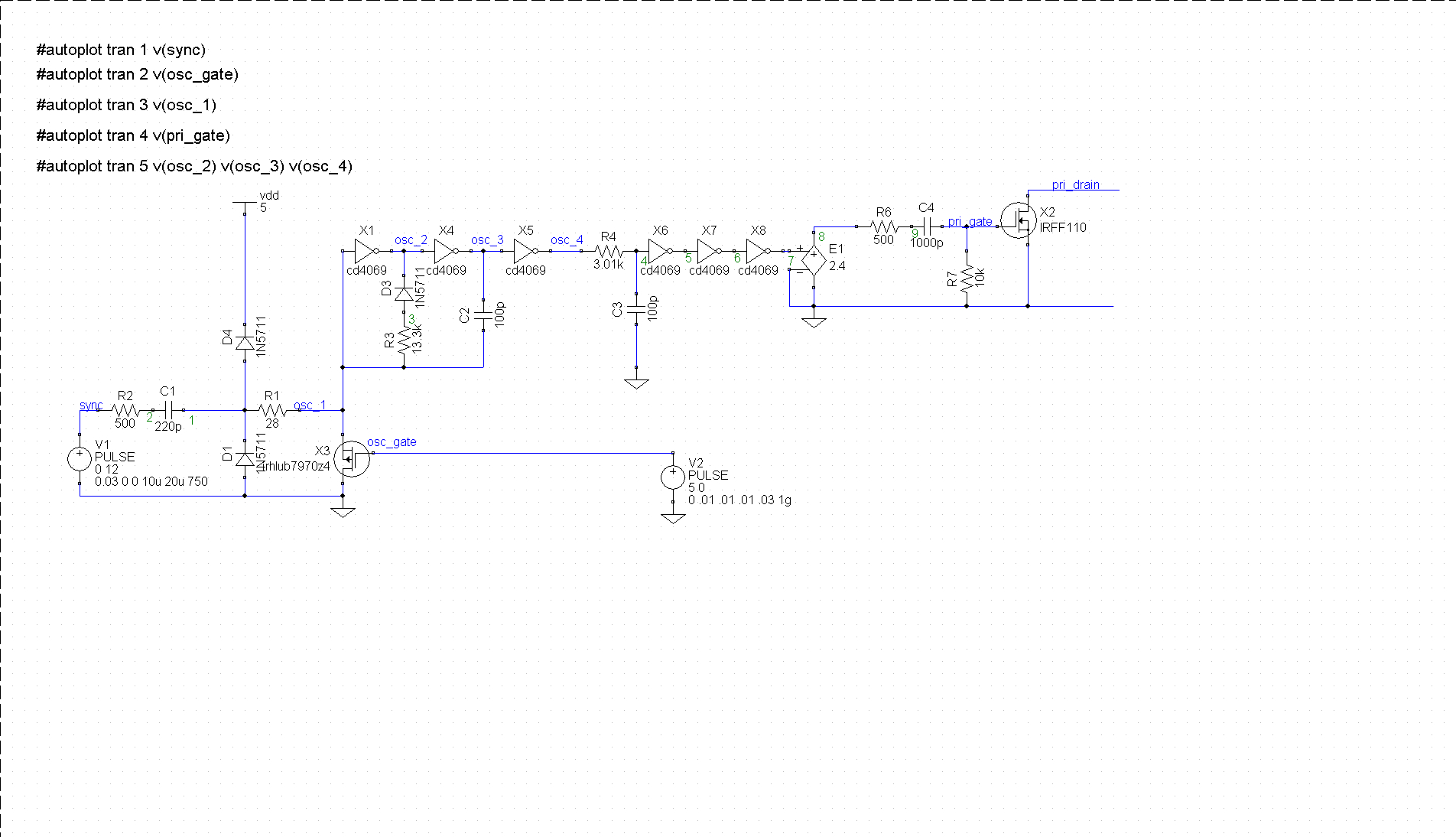


Figure ‑ SPICE schematic of “oscillator”

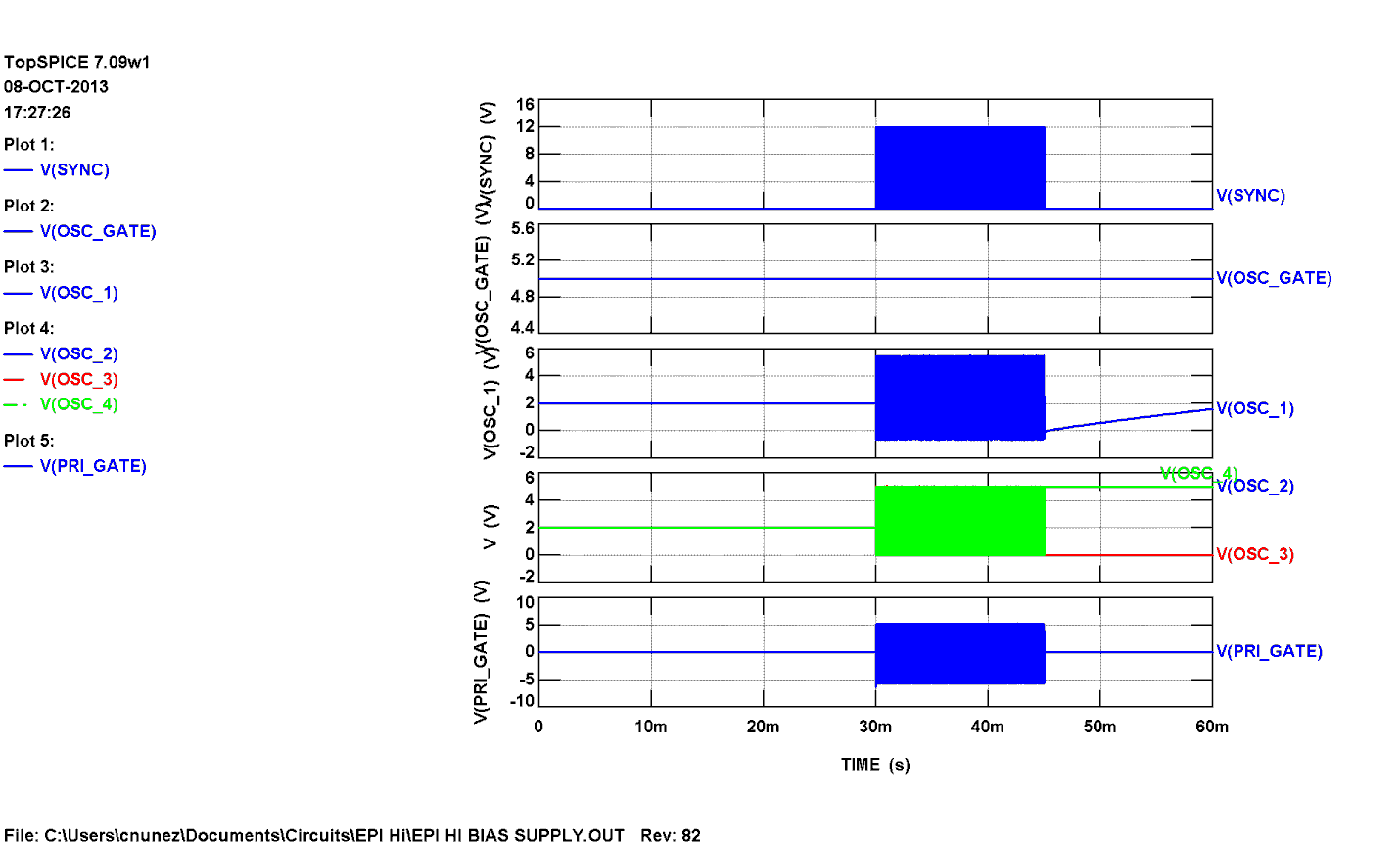


Figure ‑ SPICE simulation of “oscillator”

# Pulse Width Modulation

Without the oscillator function of this circuit block the other function it should perform is pulse-width-modulation (PWM). Figure 0‑1 below shows that the circuit does not modulate the pulse width but rather disables the pulses to the primary MOSFET (orange circle) as the gate voltage of the oscillator MOSFET (red circle) is decreased.

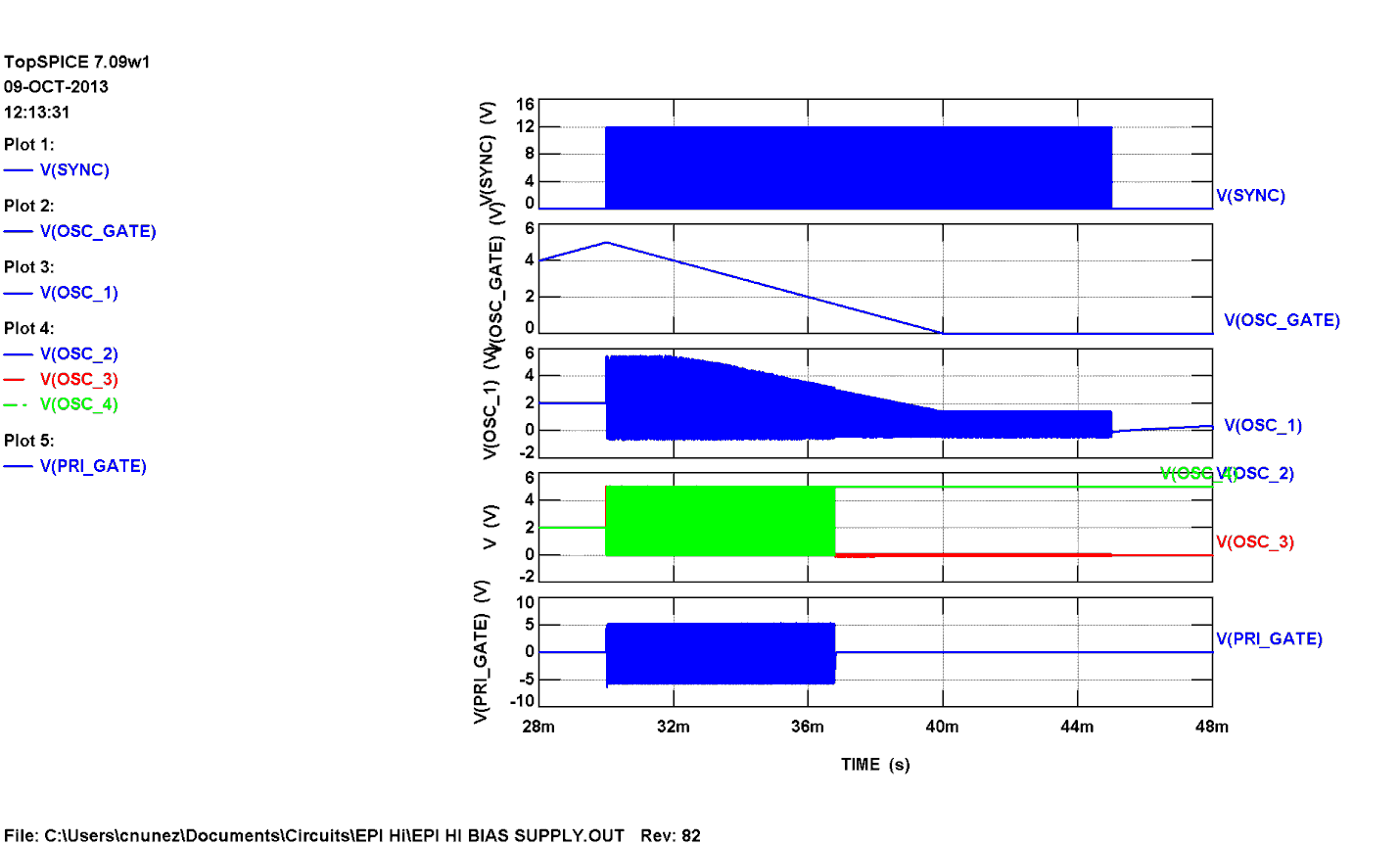


Figure ‑ SPICE simulation of PWM function

Figure 0‑2 below zooms in on the aforementioned simulation to show that the circuit does not modulate the pulse width but rather disables the pulses to the primary MOSFET (orange circle) as the gate voltage of the oscillator MOSFET (red circle) is decreased.

If this circuit block does not oscillate or modulate the pulse width, then it regulates the high voltage output as a “ripple” regulator or “bang-bang” regulator. When the output voltage is too high the pulses turn off to let the output float down. As the output voltage then gets too low, the pulses are turned back on to charge the output. The upside of such a regulator is that energy saved when the pulses are off, thus improving efficiency. The downside is that the output ripple will be at a variable frequency that is lower than the sync frequency. The amplitude of the output ripple should be higher than that of a converter using PWM. Since the HV converter is low power, these low frequency current spikes it will draw from the LVPS that feeds it may not pose an EMI problem. It must be noted that each HV converter will probably have a different overall operating frequency that may not be synchronized to the others and will be load dependent.

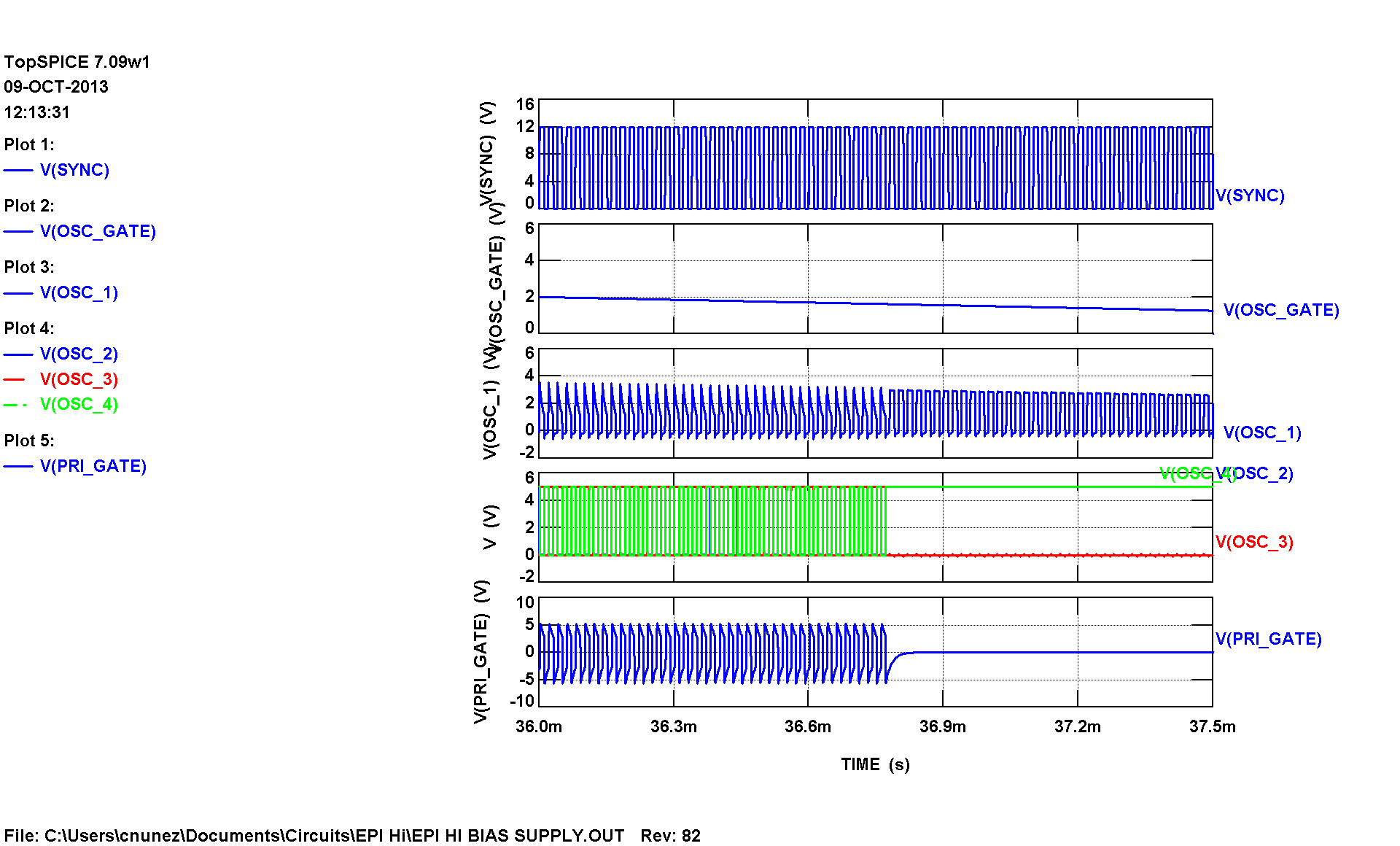


Figure ‑ SPICE simulation of PWM function (zoomed in)

## Circuit Simplification

One could argue that the circuit could be simplified if it is true that it doesn’t oscillate and doesn’t modulate the pulse width. One, two-input gate with one input tied to the sync signal and the other tied to the error amplifier output (It may be better to use a comparator instead of an op amp in this case) could perform the same function as shown in Figure 0‑3 and Figure 0‑4 below. This would reduce the number of parts and thus improve the reliability. They seemed to reference this methodology a lot during the review meeting.

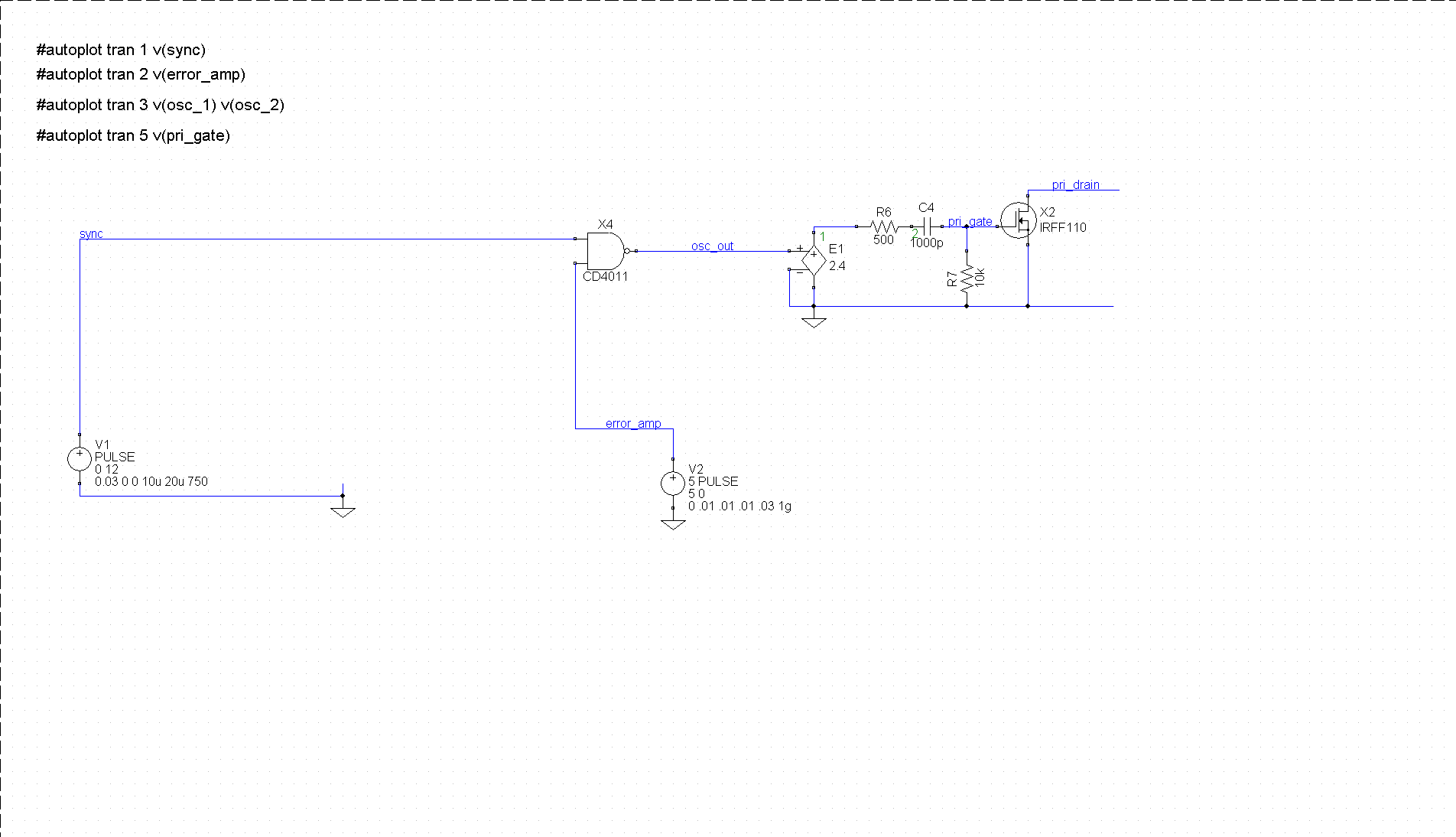


Figure ‑ Simplified circuit schematic

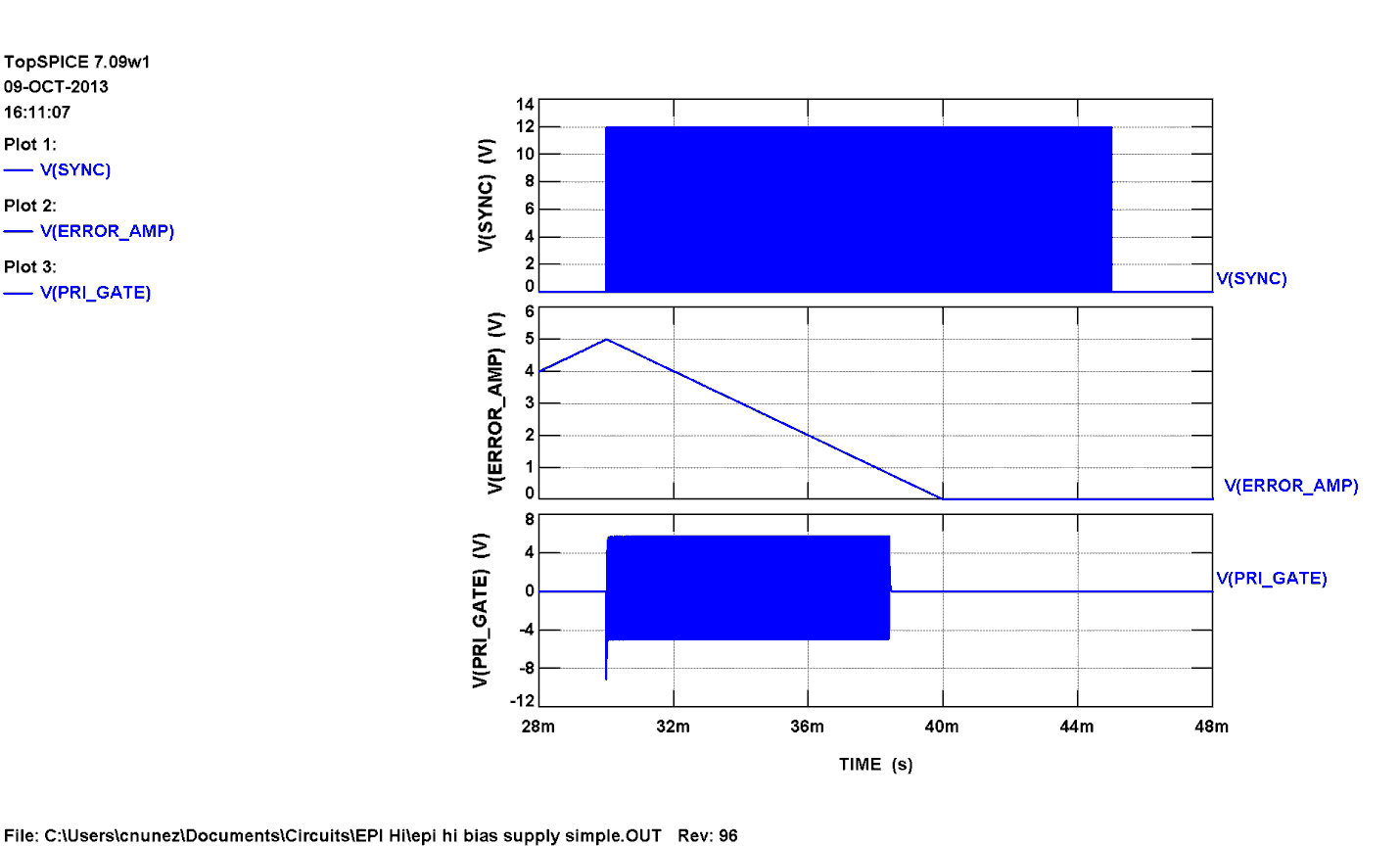


Figure ‑4 Simplified circuit simulation

One entire converter was also modeled using SPICE. The simulation results are shown in the figures described below.

Figure 0‑5 shows the control (pgm) voltage ramping up slowly (100mS) and the HV output following the control signal with a little bit of overshoot.

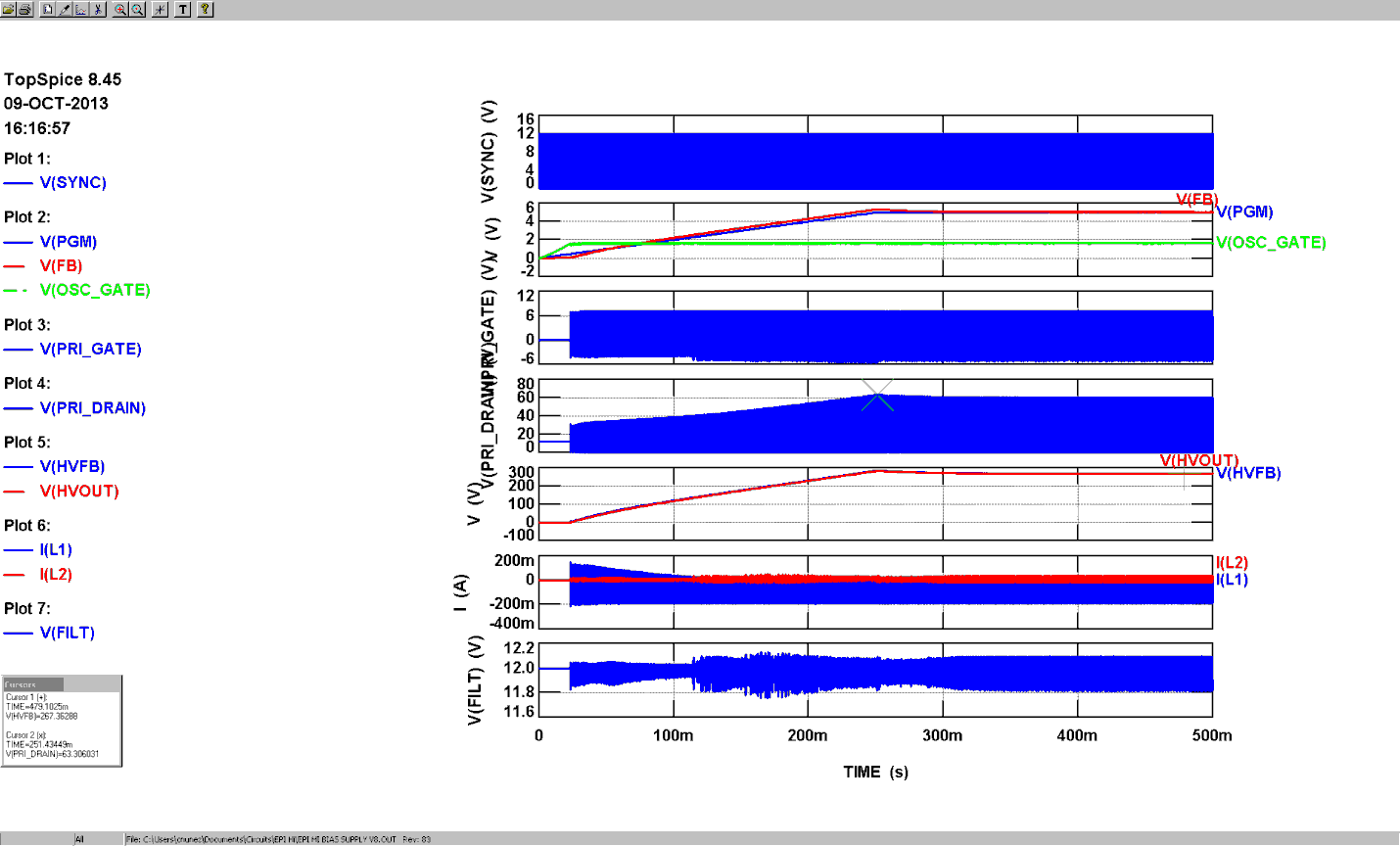


Figure ‑ Converter simulation results

Figure 0‑6 shows that the pulses to the primary MOSFET gate become more frequent as the control signal and output voltage increase. A normal PWM converter would show just as many pulses at the primary MOSFET gate (orange circle) as there are pulses coming from the sync signal (red circle).

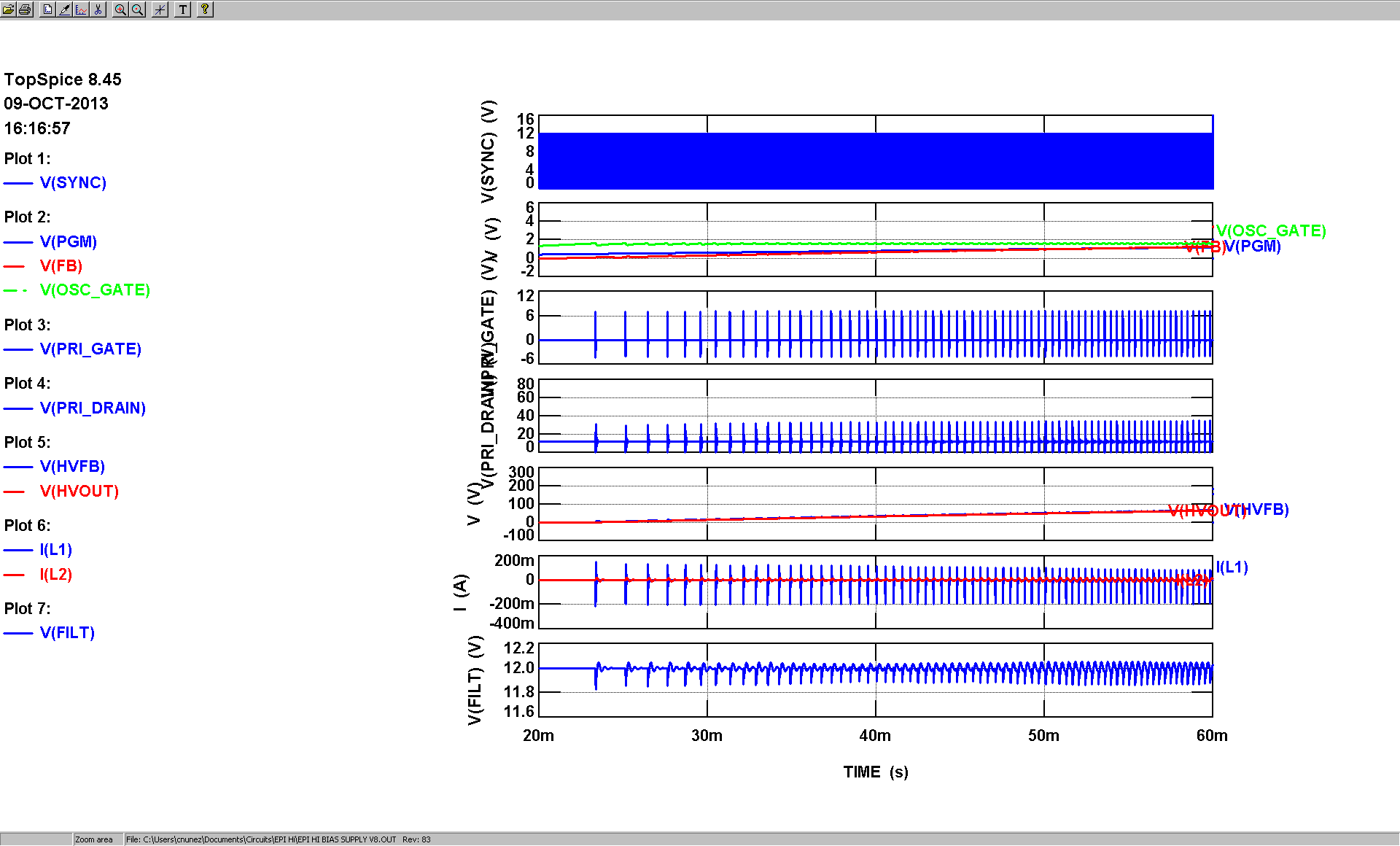


Figure ‑ Converter simulations results (zoomed on beginning)

Figure 0‑7 shows how the converter regulates the output by “skipping” pulses (red circle). The output ripple is filtered down to about 50mV after the final stage of output filter caps. The ripple frequency seen on the 12V input power is ~3kHz at this particular load (180uA).

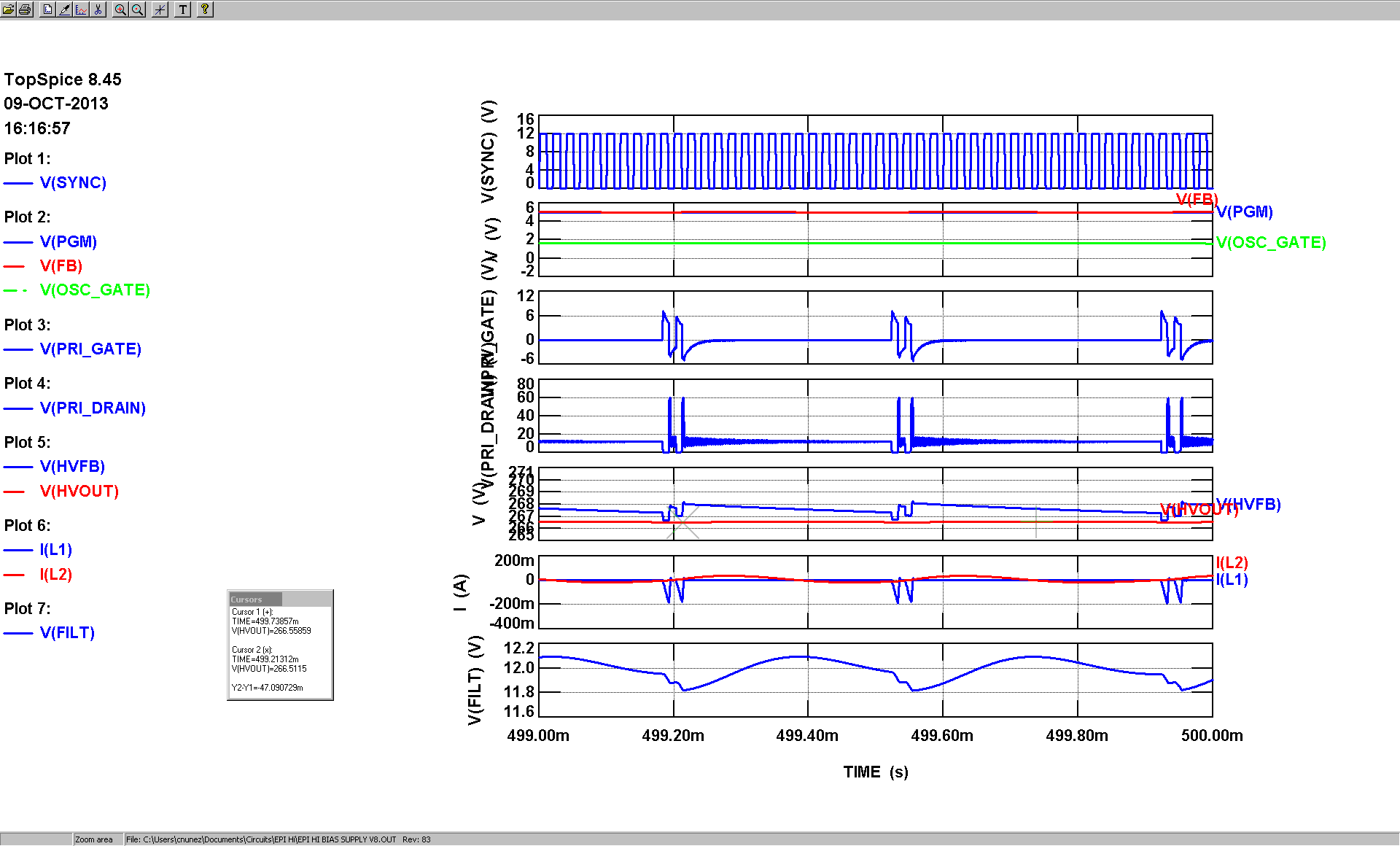


Figure ‑ Converter simulation results (zoomed on end)

# LV Converter

The low voltage output that uses this converter should have the same operating characteristics mentioned above as shown in the simulation below.

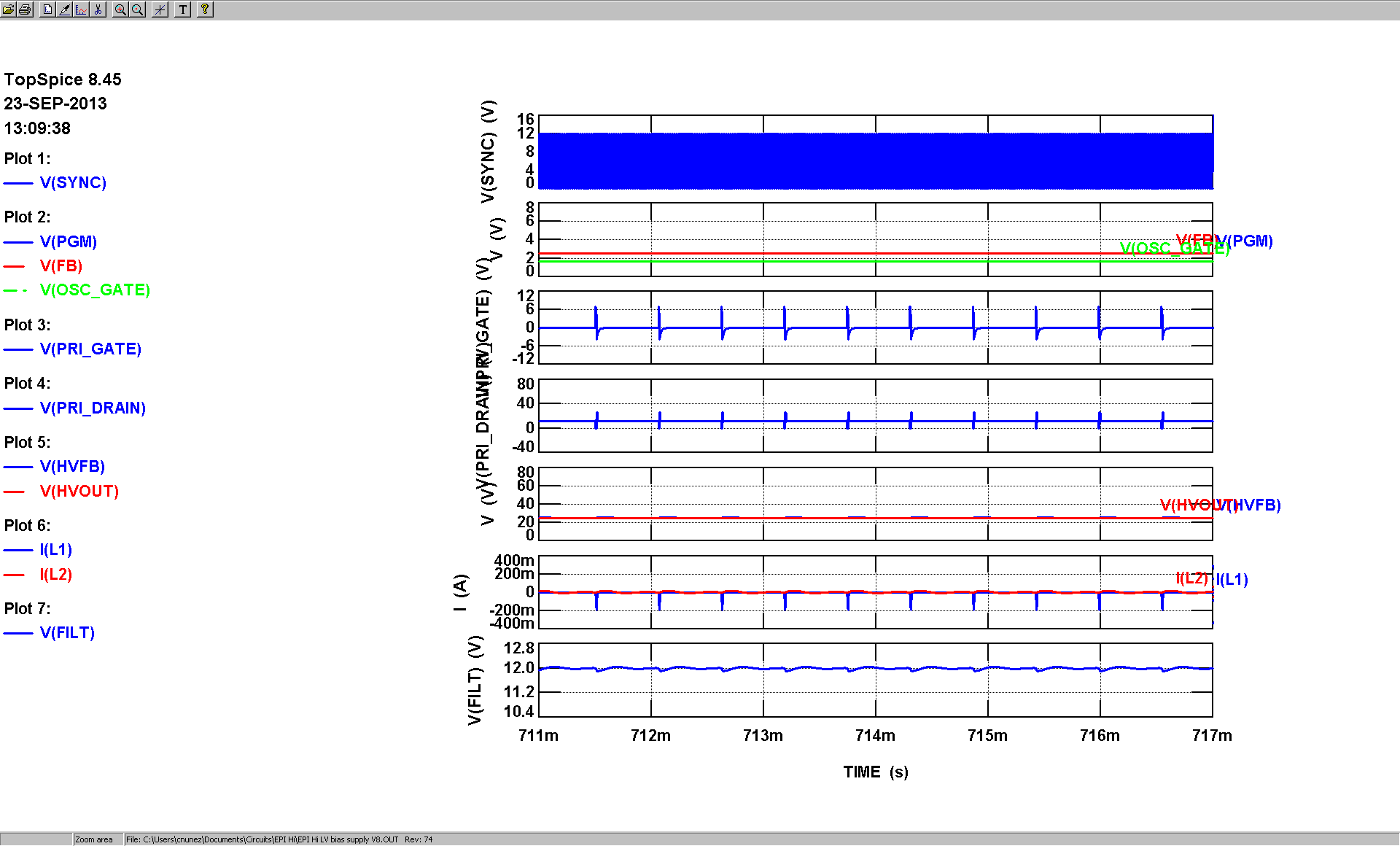


Figure ‑1 LV converter simulation

It should also be noted that the voltage on the primary MOSFET drain went up as high as 80V (red circle in Figure 0‑2) when the converter was turned on with the control voltage previously applied due to initial overshoot at LV output. While this voltage is not high enough to damage the MOSFET according to the data sheet, it appears that the voltage may have been limited by breakdown current through the part. Care must be taken to avoid this type of situation. Simulations of the HV converter under similar conditions do not show this problem.

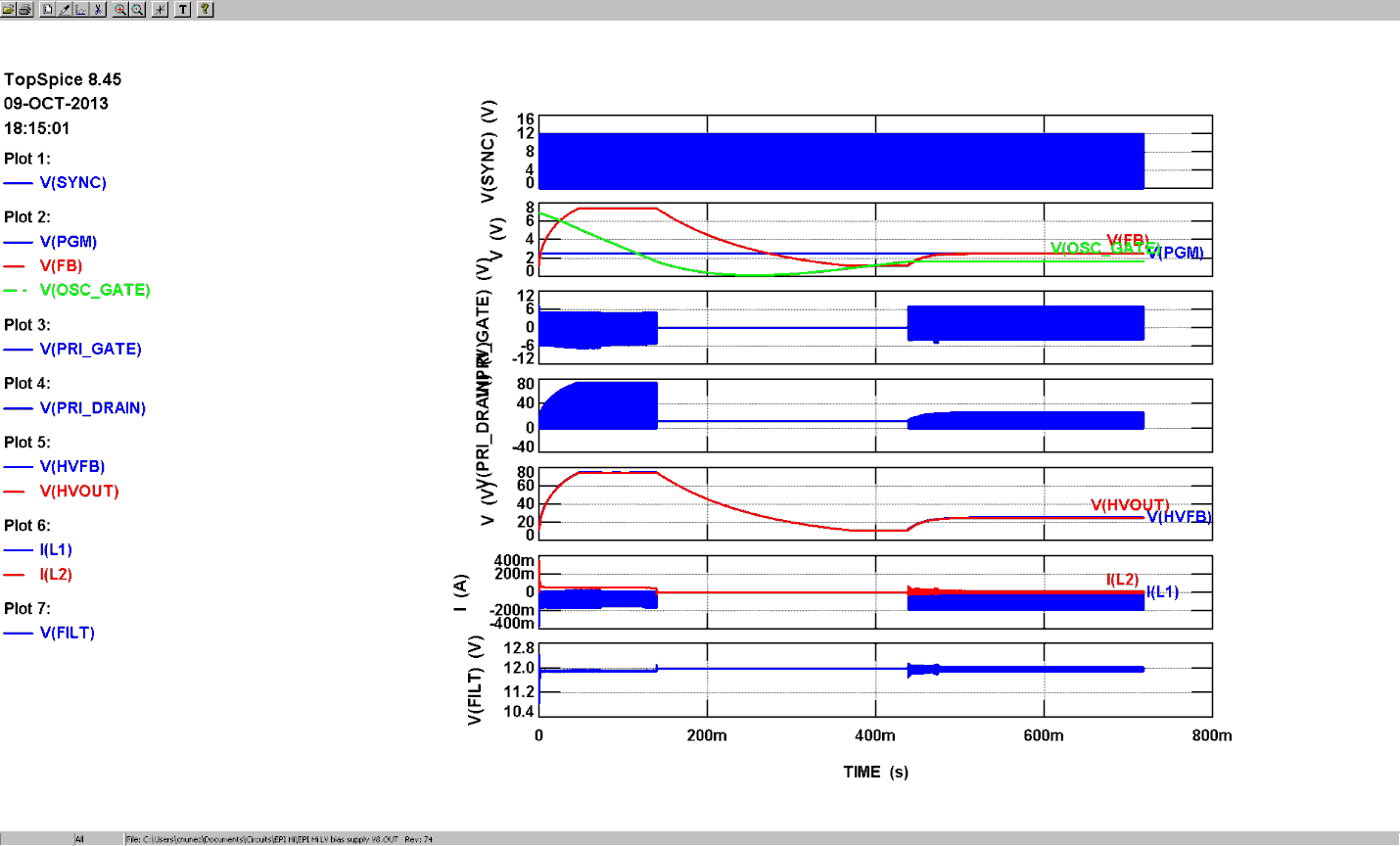


Figure ‑2 LV converter simulation at turn-on

# HV Linear Regulator

Simulations of the linear regulator shown in Figure 0‑1 below show that the output voltage settles in several seconds while the converter HV output settles much faster. This may or may not be a problem depending on the system requirements.



Figure ‑1 HV Linear regulator

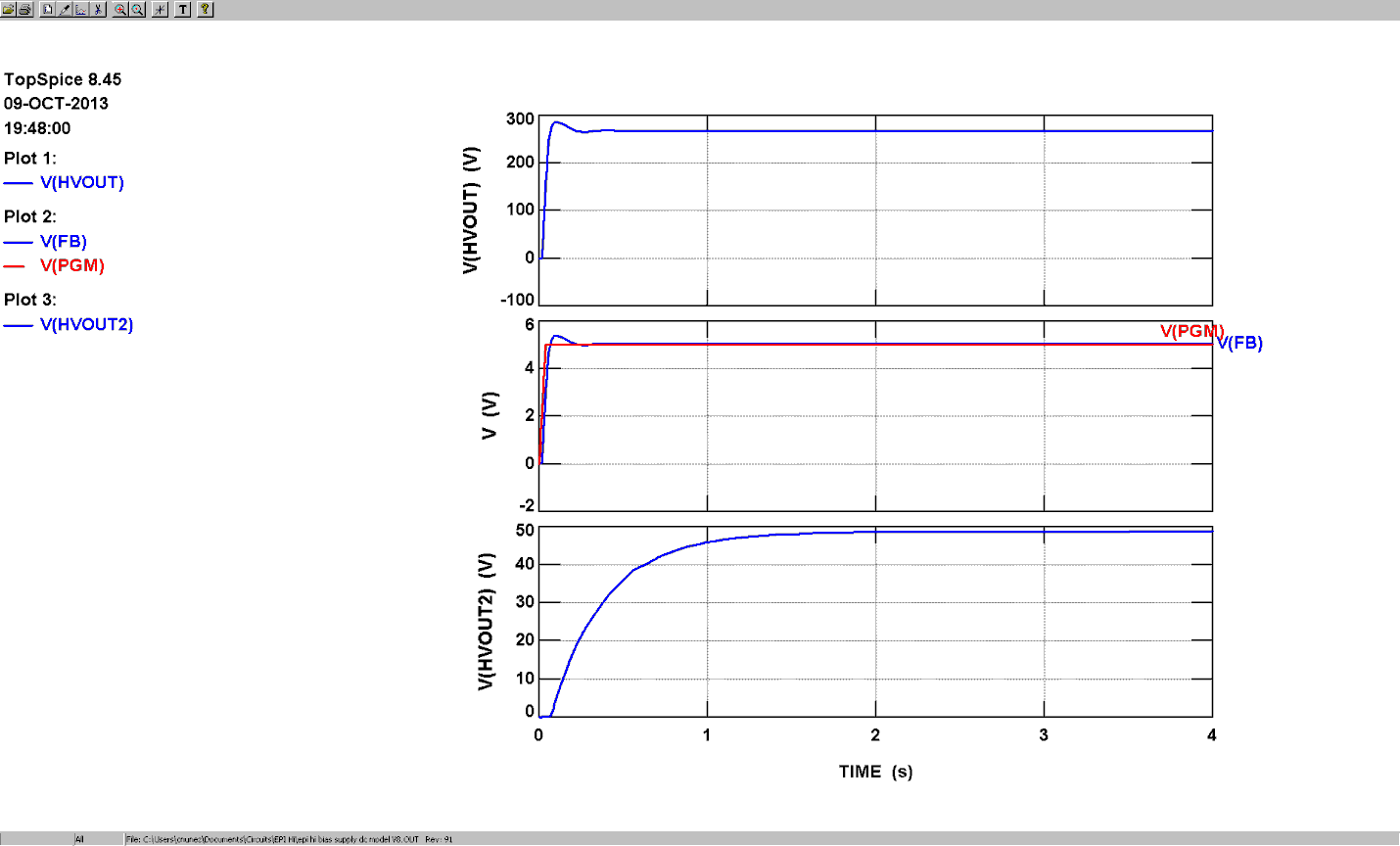


Figure ‑2 HV linear regulator simulation