EPI-Hi

Bias Supply

Requirements Specification

Revision B

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Approval Signatures

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Alan Cummings, Caltech Date

Document Revision Record

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	Aug. 23, 2012	Draft version	Rick Cook
A	Nov. 26, 2012	Updated all sections	Rick Cook
B	Sep. 17, 2013	Updated harness diagram, connector pinouts & P/Ns, mechanical and detector figures, grounding section. Added instrument block diagram and board outline.	Rick Cook

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1. Introduction

The Energetic Particles Instrument for High Energy (EPI-Hi), part of ISIS suite of cosmic-ray instruments on Solar Probe Plus spacecraft, comprises two Low Energy Telescopes (LET1 and LET2), High Energy Telescope (HET), and supporting electronics as shown in Figure 1-1.

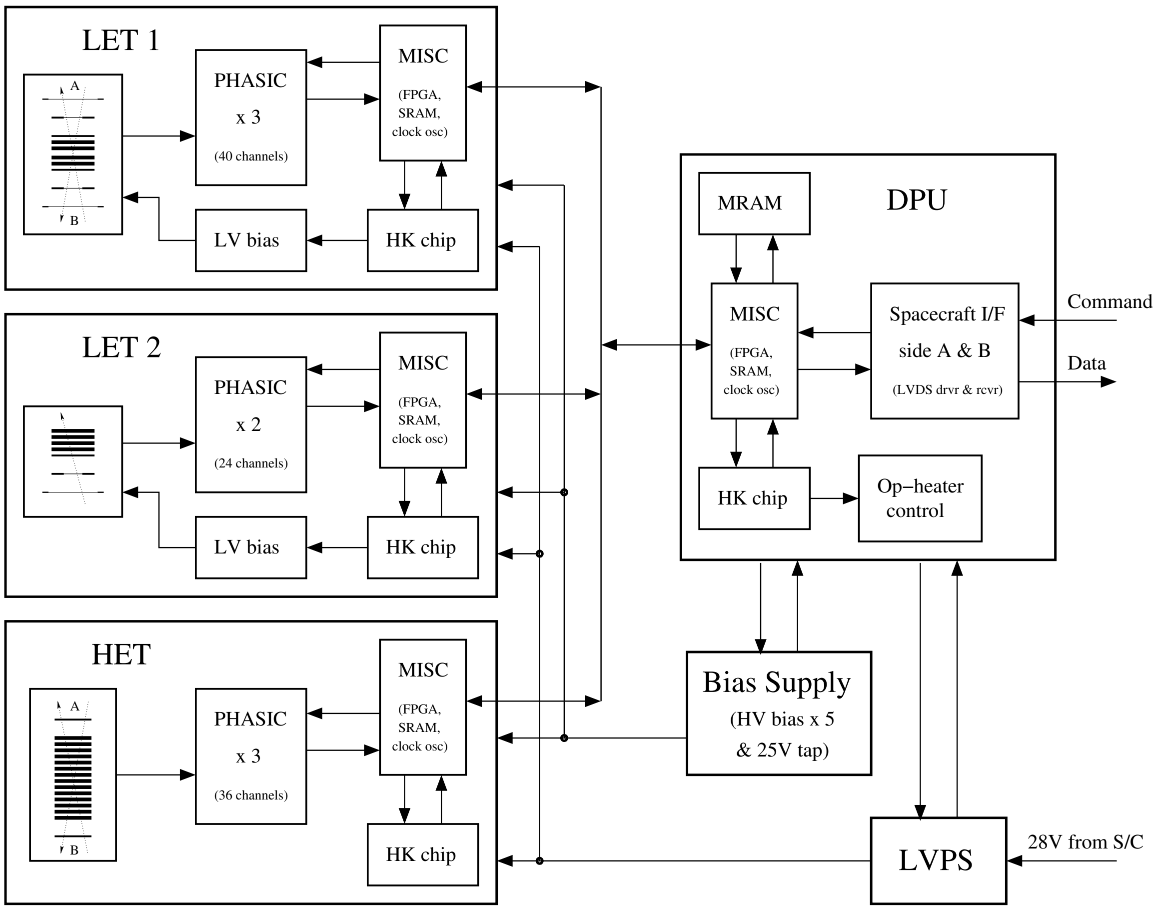


Figure 1-1 EPI-Hi Block Diagram

This document specifies design requirements for the Bias Supply that will provide low-noise, positive, adjustable high-voltage bias to EPI-Hi's thick silicon detectors. The three EPI-Hi telescopes are extremely sensitive to electronic noise, so every effort must be made to make this Bias Supply as quiet as possible, and employ as much of the same heritage design as was last used on the STEREO/SEP Bias Supply.

The EPI-Hi Bias Supply requirements specified herein are based on the information currently available (Phase B) and may evolve as the telescope designs mature. Space Instruments shall design electronic schematics and printed circuit board layout according to these requirements. Procurement of electronic parts, printed circuit boards and the board assembly shall be the responsibility of Caltech. Testing of one EM and one flight board shall first take place at Space Instruments, then continue at Caltech. Mechanical packaging design for the Bias Supply and manufacturing of its RF shield is the responsibility of GSFC.

EPI-Hi instrument is very constrained in terms of mass and power, and special attention must be paid to optimizing the use of these resources in the design and fabrication of the Bias Supply. Current estimates are 224g for the mass of assembled flight board, 130g for RF shields, 115mW power consumption at the beginning of detector life and 680mW at the end of life.

The schedule for Bias Supply design, fabrication and test is as follows:

Start design work on EM board	Mar. 6, 2013
Testing of the EM board	Nov. 29 – Dec. 27, 2013
Start work on the flight board	Jan. 1, 2015
Testing of the flight board	June 29 – July 6, 2015

Above dates are subject to change. Space Instruments and Caltech shall strive to beat the current schedule by about two months in order to keep the Earned Value parameters in good shape.

Other important Project milestones:

EPI-Hi Preliminary Design Review	Nov. 5, 2013
EPI-Hi Critical Design Review	Feb. 10, 2015

1.1 *Document Conventions*

In this document the acronym TBD (to be determined) means that no data currently exists. A value followed by TBR (to be resolved) means that it is preliminary. In either case, they may be followed by institution name indicating who is responsible for providing the data.

1.2 *Applicable Documents*

The following reference documents shall apply to the design, fabrication and testing of the EPI-Hi Bias Supply. It is assumed that they will be available on ISIS TWiki site at SwRI in due time.

1. NASA EEE-INST-002: Instructions for EEE Parts Selection, Screening, Qualification and Derating
2. 7434-9040 SPP Electromagnetic Environment Control Plan
3. 7434-9039 SPP Environmental Design and Test Requirements Document
4. SPP safety and mission assurance requirements

These documents and others, like mechanical drawings of the telescopes and tables with detector capacitances, will be provided to the Bias Supply designer separately.

2. EPI-Hi Harness Diagram

EPI-Hi harness diagram in Figure 2-1 describes how the Bias Supply Board is connected to the rest of the instrument. Internal harness routing has been optimized with respect to the connector voltage rating and physical size.

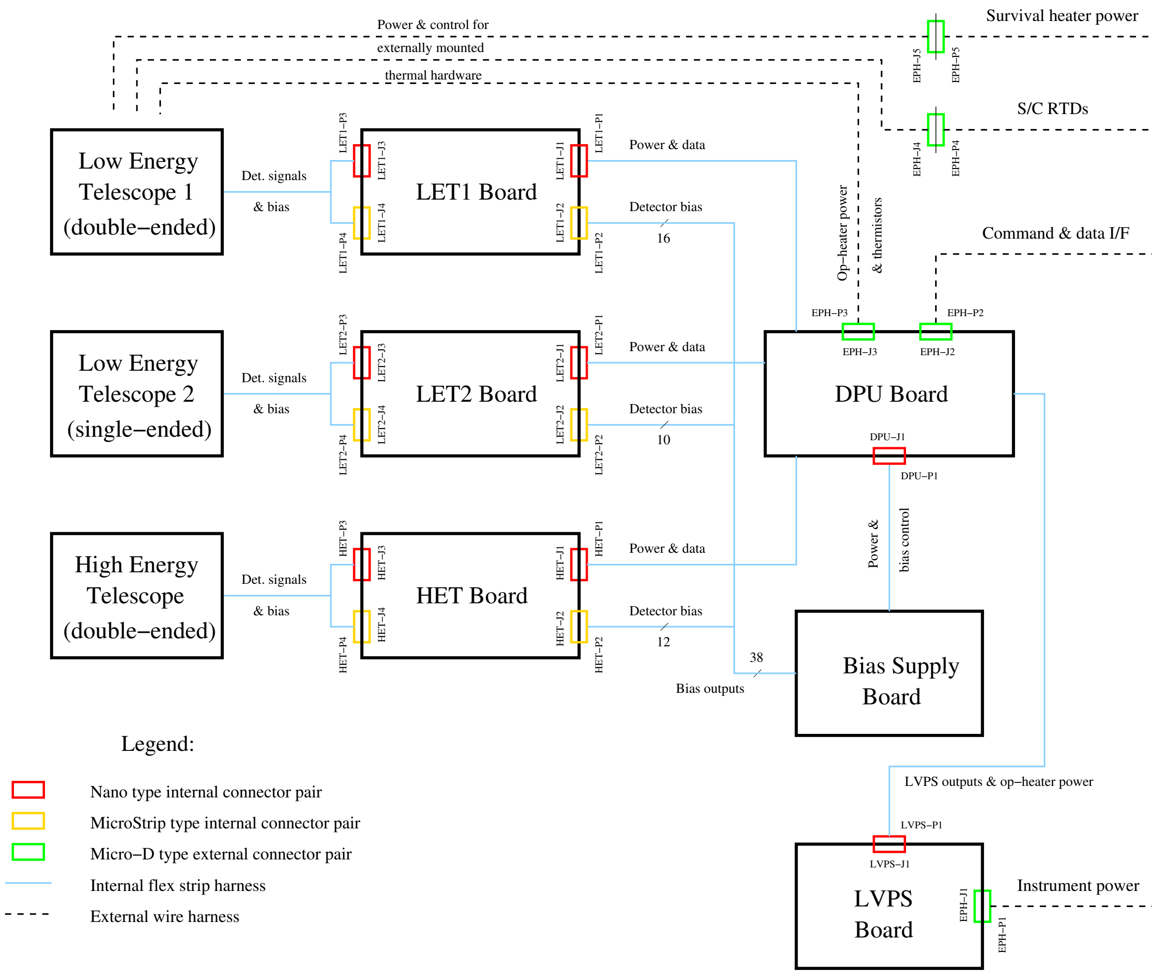


Figure 2-1 EPI-Hi Harness Diagram

3. Electrical Requirements

3.1 *Bias Configuration*

EPI-Hi bias configuration is presented in Figure 3-1 on the following page and explained below.

LET1, LET2 and HET comprise stacks of Si detectors as shown in Appendix Figures 7-1 through 7-4. The detectors have thicknesses of 10, 25, 500 and 1000um (microns). The order of detectors within a telescope stack is arranged by thickness so that the thinnest detectors are at the entry and the thickness gradually increases toward the deeper regions of the telescope. For double-ended telescopes the detector order is symmetrical with respect to the middle of the telescope where the thickest detectors reside. The same symmetry and order are preserved in the figures and tables of this document.

We refer to the EPI-Hi detectors as either ‘thin’ or ‘thick’ and they require different bias voltages that depend on their thickness. The task of providing the bias to these two groups of detectors is split in two:

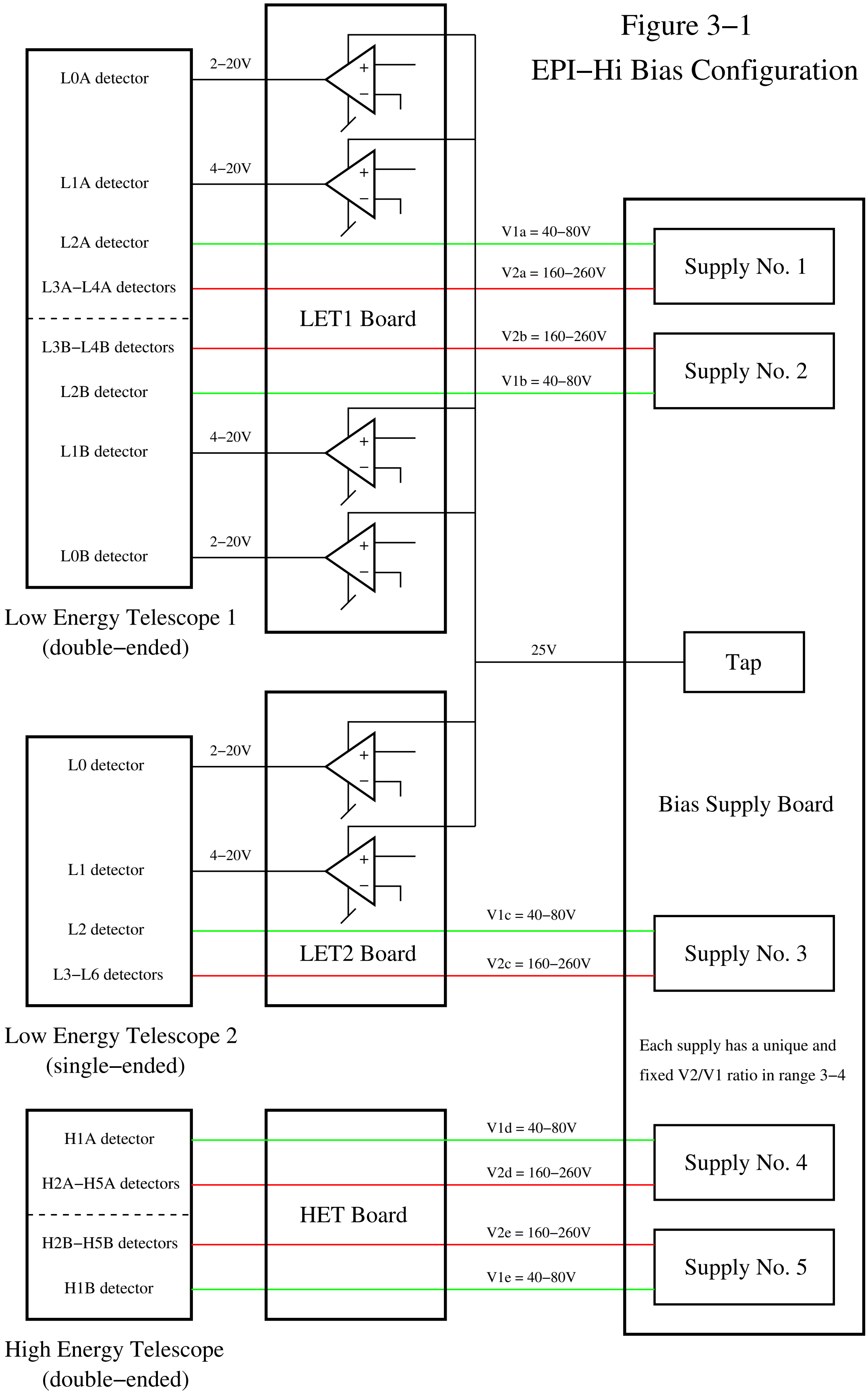
1. The thin detectors (10 and 25um) shall receive bias voltage that is generated by op-amps* on each telescope board. The Bias Supply shall have a single regulated 25V output feeding these op-amps.

2. The thick detectors (500 and 1000um) shall receive adjustable bias voltages directly from the Bias Supply as a proportionally divided pair coming from a dedicated supply. In Figure 3-1 these two bias lines are shown in green (V1) and red (V2). Each pair will have a unique and fixed ratio in the range between 3 and 4. The exact ratio will be determined early in detector testing phase because of the uncertainty inherent in the detector manufacturing process.

For redundancy, detectors located in each physical end of a given telescope shall have their own source of bias voltage. Since LET1 and HET are double-ended, while LET2 is single-ended, there are five telescope ends that need to be independently served with bias voltages. For the thick detectors this means that the Bias Supply Board will comprise five identical supplies. Each one will have its own control input and a pair of proportionally tied outputs, one for 500um (V1) and one for 1000um detectors (V2).

* The op-amps used on the telescope boards are Intersil P/N:
HS9-3530ARH-Q for flight parts, DSCC P/N 5962F9568701VXC and
HS9-3530ARH/Proto for EM parts. Each comes in a 10-pin flat-pack.

Figure 3−1
EPI−Hi Bias Configuration



3.2 *Input Power*

The Bias Supply shall receive regulated LVPS analog power +12V and -6V via DPU Board as specified in Section 6.1.1 (connector pinout for BIAS-J1). These voltages are allowed to vary +/- 5% over the full load and life of the mission.

3.3 *EMC Requirements*

The Bias Supply shall be designed in full compliance with the EMC requirements given in reference 2. They include a requirement that the Bias Supply be clock-synchronized to a frequency multiple of 50kHz.

3.4 *Control Signals*

The DPU Board shall provide five 0-5V analog signals to the Bias Supply for independent control of the five supplies within. Each control signal is sourced by the HKchip using a 10-bit DAC with its output buffered by on-chip rail-to-rail op-amp designed to drive a 20kohm load.

The DPU Board shall provide one 0-3.3V digital 50kHz clock to the Bias Supply per EMC requirement listed in the previous Section.

3.5 *Output Voltages*

The Bias Supply shall produce five pairs of adjustable proportionally scaled positive bias voltages for the thick detectors located in the five telescope ends as indicated by the color-coded table in Figure 3-2.
It shall also produce a single 25V regulated output, shown in the bottom row of the table. Voltage tolerance is looser for the divided voltages (V1a,b,c,d,e).

Bias Supply No.	Voltage Name	Telescope Name	Detector Name	Wafer Thickness [mm]	Min. Bias [V]	Max. Bias [V]	Voltage Tolerance [%]
1	V1a	LET1	L2A	0.5	40	80	+/- 20
1	V2a	LET1	L3A, L4A	1	160	260	+/- 5
2	V2b	LET1	L3B, L4B	1	160	260	+/- 5
2	V1b	LET1	L2B	0.5	40	80	+/- 20
3	V1c	LET2	L2	0.5	40	80	+/- 20
3	V2c	LET2	L3 – L6	1	160	260	+/- 5
4	V1d	HET	H1A	0.5	40	80	+/- 20
4	V2d	HET	H2A – H5A	1 & 2 x 1	160	260	+/- 5
5	V2e	HET	H2B – H5B	1 & 2 x 1	160	260	+/- 5
5	V1e	HET	H1B	0.5	40	80	+/- 20
Tap	25V	LET1 & 2	N/A	N/A	N/A	N/A	+/- 10

Figure 3-2 EPI-Hi Bias Voltage Range and Tolerance

3.6 *Leakage Current Loads*

Table in Figure 3-3 lists the nominal, end of life (EOL) and maximum in-spec operating loads for the ten outputs of the five bias supplies and the tap output. EOL leakage currents are anticipated at the end of detector life owing to radiation damage. EOL values given here (assuming 20 °C operating temperature) are conservative and could be relaxed if that leads to a simpler or more reliable Bias Supply design, or one that would better meet the resource allocations. The leakage is directly proportional to temperature, so EPI-Hi thermal design will strive to keep the detectors cool for as long as possible, but on SPP mission the spacecraft has to go through hot and cold cycles on orbit.

Each of the ten bias outputs shall be able to withstand a short circuit in any thick detector caused by either diode junction deterioration or dust particle impact that can physically break the detector. The maximum loads column gives a safety factor of two in order to satisfy this requirement (not applicable to 25V tap).

Bias Supply No.	Voltage Name	Telescope Name	Detector Name	Wafer Thickness [mm]	Detector Area [cm^2]	Nom. Current [uA]	EOL Current [uA]	Max. Current [uA]
1	V1a	LET1	L2A	0.5	4	1	30	60
1	V2a	LET1	L3A, L4A	1	4	2	80	160
2	V2b	LET1	L3B, L4B	1	4	2	80	160
2	V1b	LET1	L2B	0.5	4	1	30	60
3	V1c	LET2	L2	0.5	4	1	30	60
3	V2c	LET2	L3 – L6	1	4	4	160	320
4	V1d	HET	H1A	0.5	2.3	1	20	40
4	V2d	HET	H2A – H5A	1 & 2 x 1	2.3	7	180	360
5	V2e	HET	H2B – H5B	1 & 2 x 1	2.3	7	180	360
5	V1e	HET	H1B	0.5	2.3	1	20	40
Tap	25V	LET1 & 2	N/A	N/A	N/A	1000	1045	1200

Figure 3-3 EPI-Hi Leakage Current Loads

3.7 *Grounding*

Analog power returns coming from the Bias Supply are as follows:

+12V shall have a separate return, referred to as “dirty”, from +5V and -6V returns, referred to as “clean”.

All returns will be tied together on the LVPS Board.

A detailed grounding diagram shall be developed by Caltech and Space Instruments, featuring ground connections of all elements from detectors and their filter capacitors to the Bias Supply.

3.8 *Monitoring Signals*

The Bias Supply shall provide only one analog monitoring signal (the board temperature, measured by a thermistor) to the DPU Board as defined in the connector pinout for DPU-P1. This signal does not require any conditioning. It will be read out with 14-bit resolution in the HKchip located on the DPU Board.

The thermistor in the flight Bias Supply shall be Measurement Specialties P/N S311P18-09S7R6. It has a value of 30kΩ at 25°C. The EM thermistor P/N is 44008RC. The thermistors, their data sheet and the calibration table shall be provided by Caltech.

4. Mechanical Requirements

4.1 *Form Factor and Dimensions*

Given that EPI-Hi instrument is highly constrained in terms of mass resources, the Bias Supply Board shall be designed as a rigid-flex board to fit in the smallest volume possible. The proposed board area is 13.5 cm x 14 cm with a 4 cm x 9 cm extension. Nominal thickness of the board shall be 1.5 mm. The preliminary board outline drawing is in the Appendix, page 19.

Figure 4-1 shows the EPI-Hi telescopes mounted on the electronics box and the board stack. Bias Supply is the fourth board from the left, but this early version doesn't show the flex circuits coming off it.

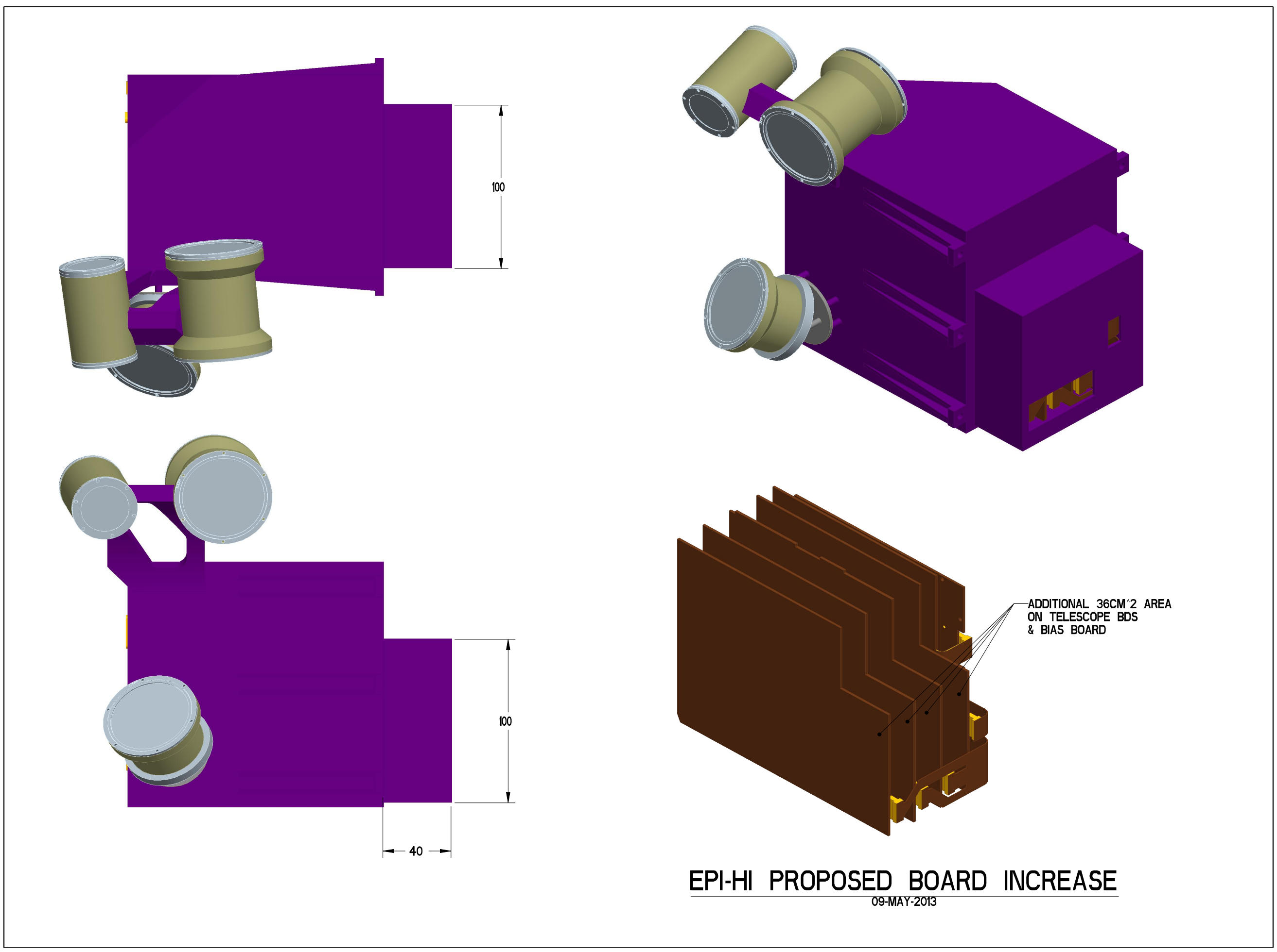


Figure 4-1 EPI-Hi Electronics Boards and Telescopes

5. Connector Types

Bias Supply connectors are described in Figure 5-1. The following notation is used:
- Nano is Glenair Series 89 Nanominiature connector per MIL-DTL-32139.
- MicroStrip is Glenair Series 171 single-row connector with Micro-D contacts per MIL-DTL-83513.
- TH is through-hole mount connector on rigid PCB or PCB tab at the end of a flex strip.

PCB or PCB tab thickness is 0.062” (1.5 mm).
- SM is surface mount connector on PCB.

Connector type is defined by terms “pin” (P) and “socket” (S). Example: Nano 25S is a 25-socket (female).

By convention, harness connector on the free end has P reference designator as part of its name, while its mate which is typically mounted either on a box or a bracket carries J in its name.

Bias Supply Connector Name	Connector Purpose	Bias Supply Connect. Type	Bias Supply Connector - Part Number - Mount Type, Panel Thickness	Mating Connector - Part Number - Mount Type, Entry - Backshell P/N
DPU-P1	Bias Supply power & control signals	Nano 31S	891-007-31SA2-BST1J-429 TH on flex strip, Straight	891-008-31PA2-BRT1T-429 TH, Right angle
LET1-P2	Bias Supply outputs for LET1	MicroStrip 12P	171-007-14P-.110-PB-429 TH on flex strip, Straight	171-008-20S-PBMH-429* SM, Right angle
LET2-P2	Bias Supply outputs for LET2	MicroStrip 12P	171-007-14P-.110-PB-429 TH on flex strip, Straight	171-008-20S-PBMH-429* SM, Right angle
HET-P2	Bias Supply outputs for HET	MicroStrip 12P	171-007-14P-.110-PB-429 TH on flex strip, Straight	171-008-20S-PBMH-429* SM, Right angle

Notes:
* Custom P/N will be assigned for this modified connector so guide pins can be tied to GND

Figure 5-1 Bias Supply Connector Types

6. Connector Pinouts

6.1 DPU-P1 Bias Supply Power & Control Signals

Pin	Signal Name
1	+12A
2	+12A
3	+5A
4	+5A
5	-6A
6	-6A
7	ANA PWR RTN
8	ANA PWR RTN
9	LET1 A CTRL
10	LET1 A CTRL
11	LET1 B CTRL
12	LET1 B CTRL
13	BIAS TEMP +
14	BIAS TEMP +
15	BIAS TEMP -
16	BIAS TEMP -
17	+12A PWR RTN
18	+12A PWR RTN
19	LET2 CTRL
20	LET2 CTRL
21	HET A CTRL
22	HET A CTRL
23	HET B CTRL
24	HET B CTRL
25	Spare*
26	Spare*
27	Spare*
28	DIG PWR RTN
29	DIG PWR RTN
30	50 KHZ CLK
31	50 KHZ CLK

6.2 LET1-P2 Bias Supply Outputs for LET1

Pin	Signal Name
1	LET1 BIAS RTN
2	LET1 25V
3	LET1 L2A HV
4	LET1 L34A HV
5	LET1 L34A HV

6	LET1 L2A HV
7	LET1 L2B HV
8	LET1 L34B HV
9	LET1 L34B HV
10	LET1 L2B HV
11	LET1 25V
12	LET1 BIAS RTN

6.3 LET2-P2 Bias Supply Outputs for LET2

Pin	Signal Name
1	LET2 BIAS RTN
2	LET2 25V
3	LET2 L2 HV
4	LET2 L3-6 HV
5	Spare*
6	Spare*
7	LET2 L2 HV
8	LET2 L3-6 HV
9	Spare*
10	Spare*
11	LET2 25V
12	LET2 BIAS RTN

6.4 HET-P2 Bias Supply Outputs for HET

Pin	Signal Name
1	HET BIAS RTN
2	Spare*
3	HET H1A HV
4	HET H2-4A HV
5	HET H2-4A HV
6	HET H1A HV
7	HET H1B HV
8	HET H2-4B HV
9	HET H2-4B HV
10	HET H1B HV
11	Spare*
12	HET BIAS RTN

Notes:
* The mating contact will be tied to the neighboring signal so the spares won't be left floating

7. Appendix

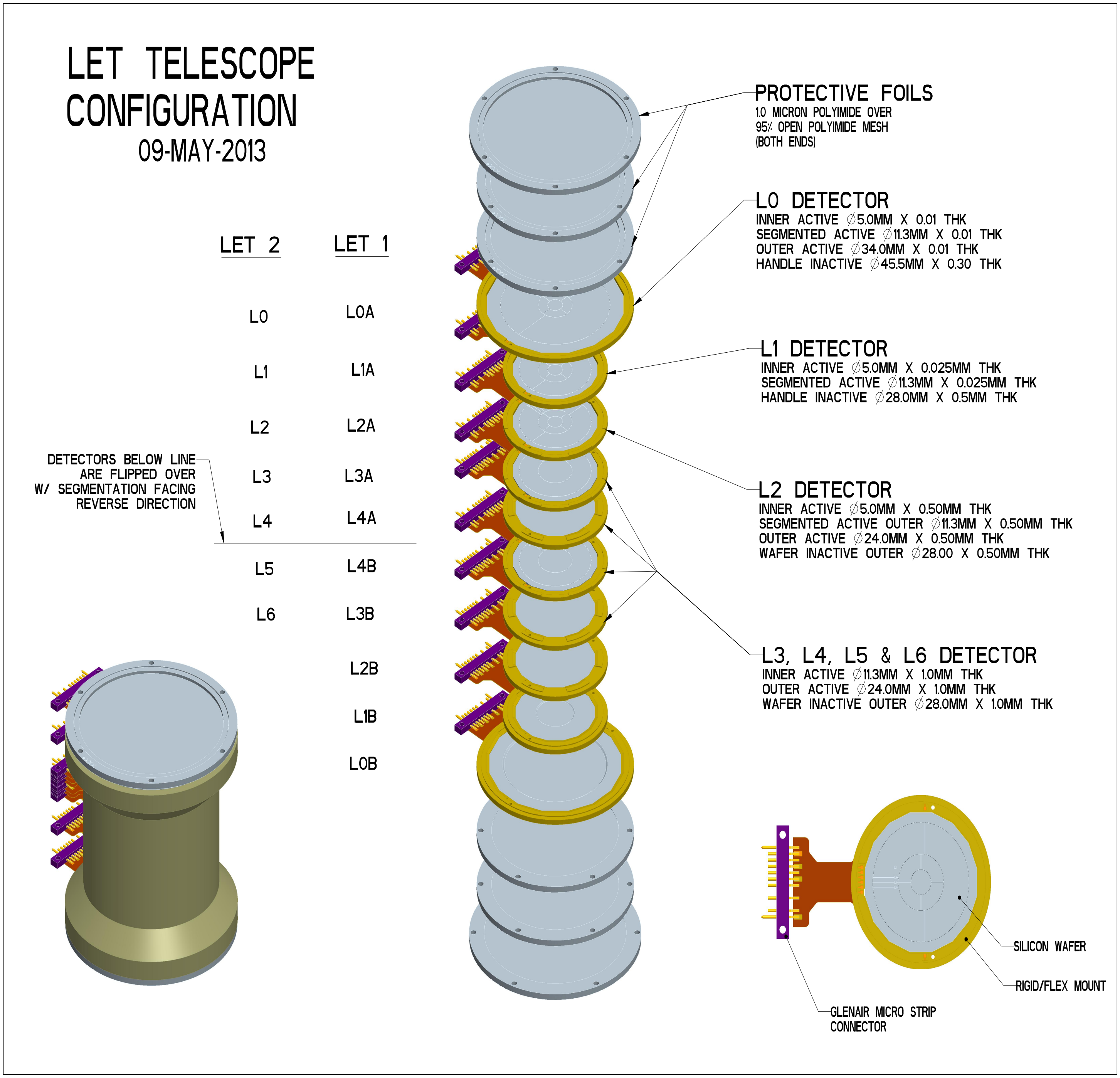


Figure 7-1 Detector stacks of the Low Energy Telescopes 1 and 2 (LET1 is double-ended, LET2 is single-ended)

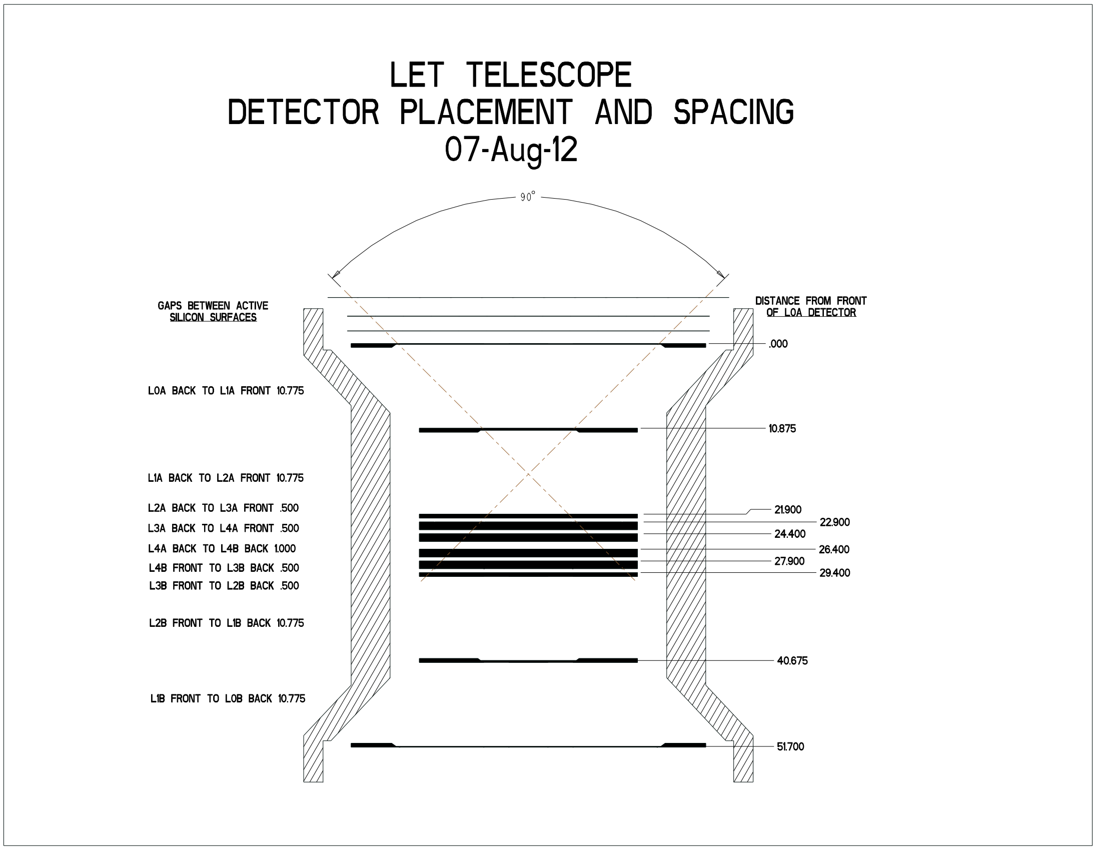


Figure 7-2 Detector placement & spacing in the Low Energy Telescopes 1 and 2 (LET1 is double-ended, LET2 is single-ended)

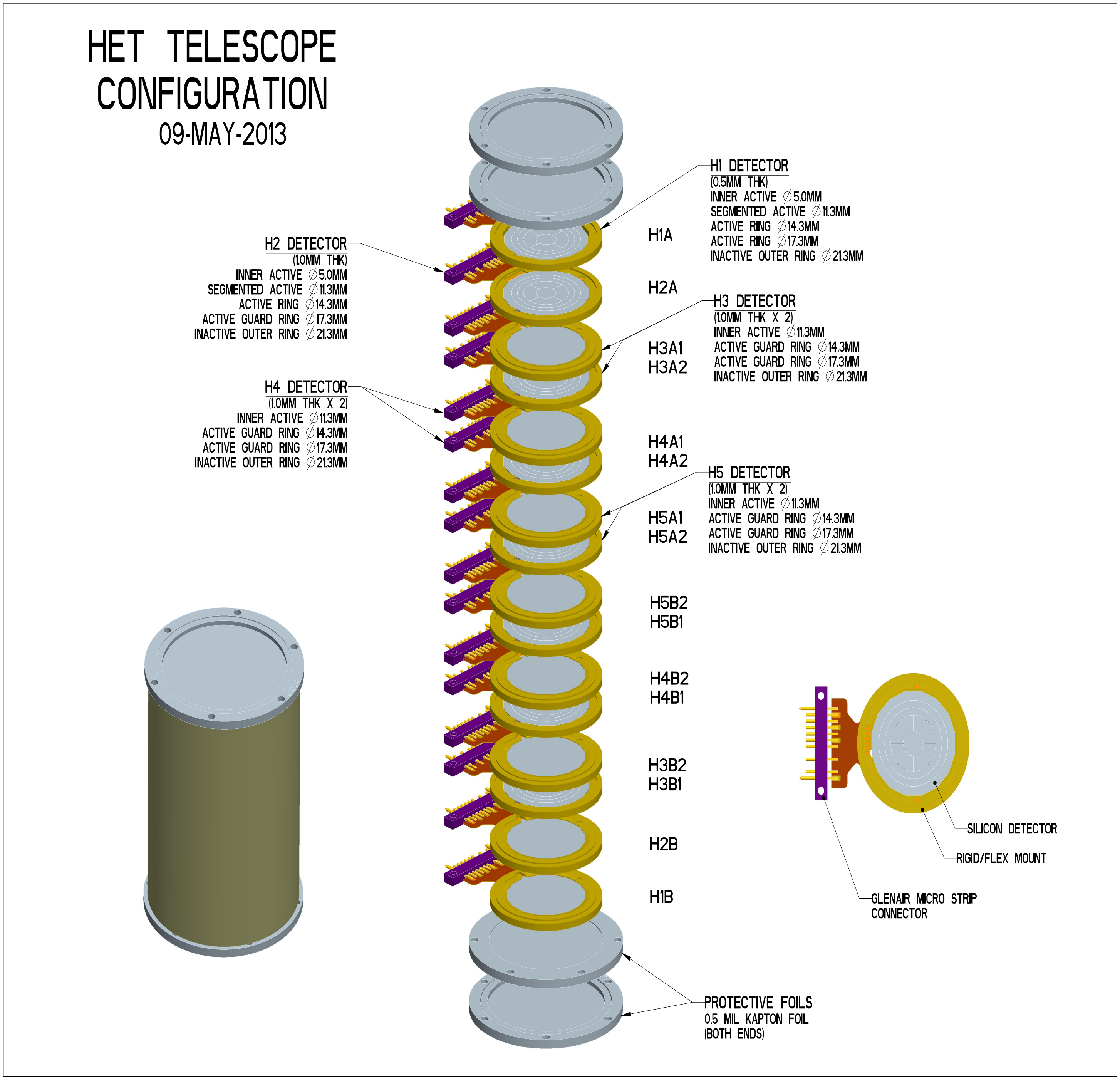


Figure 7-3 Detector stack of the High Energy Telescope

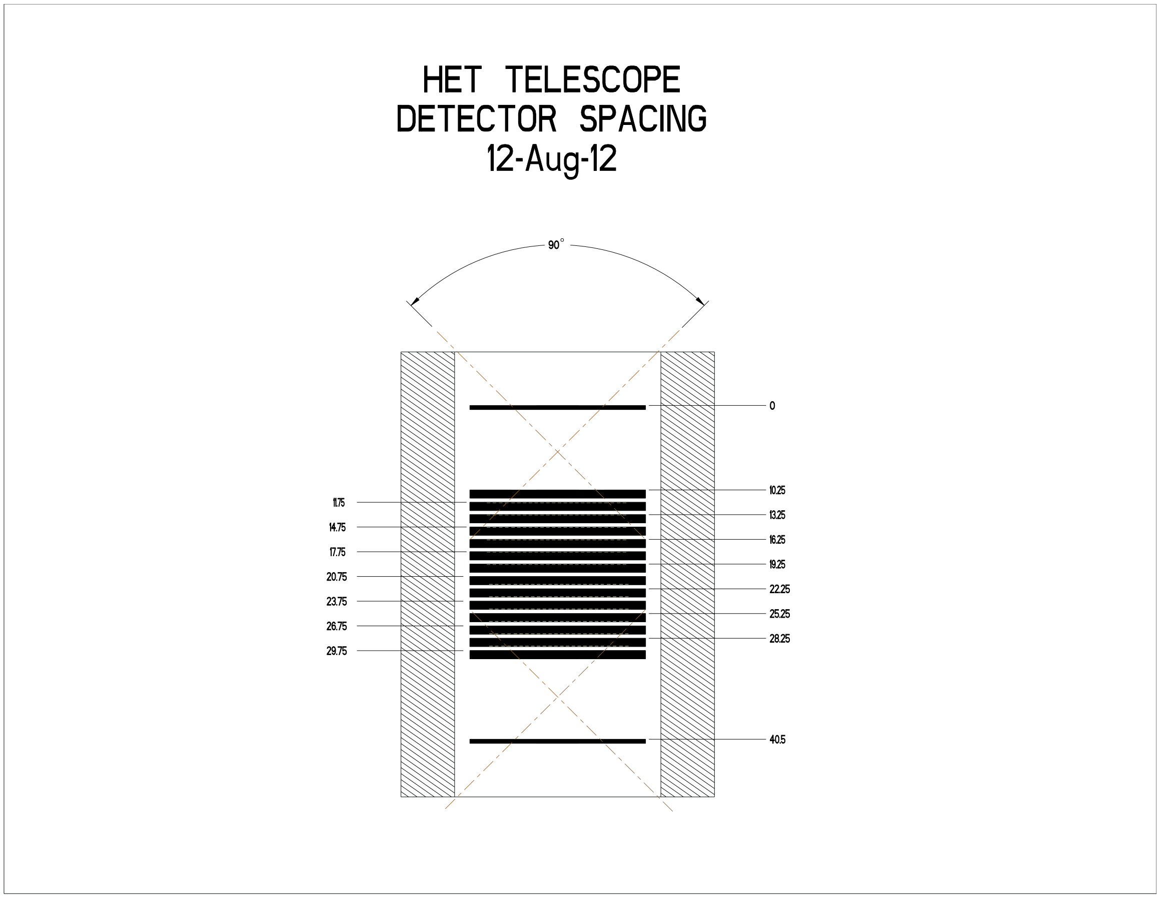
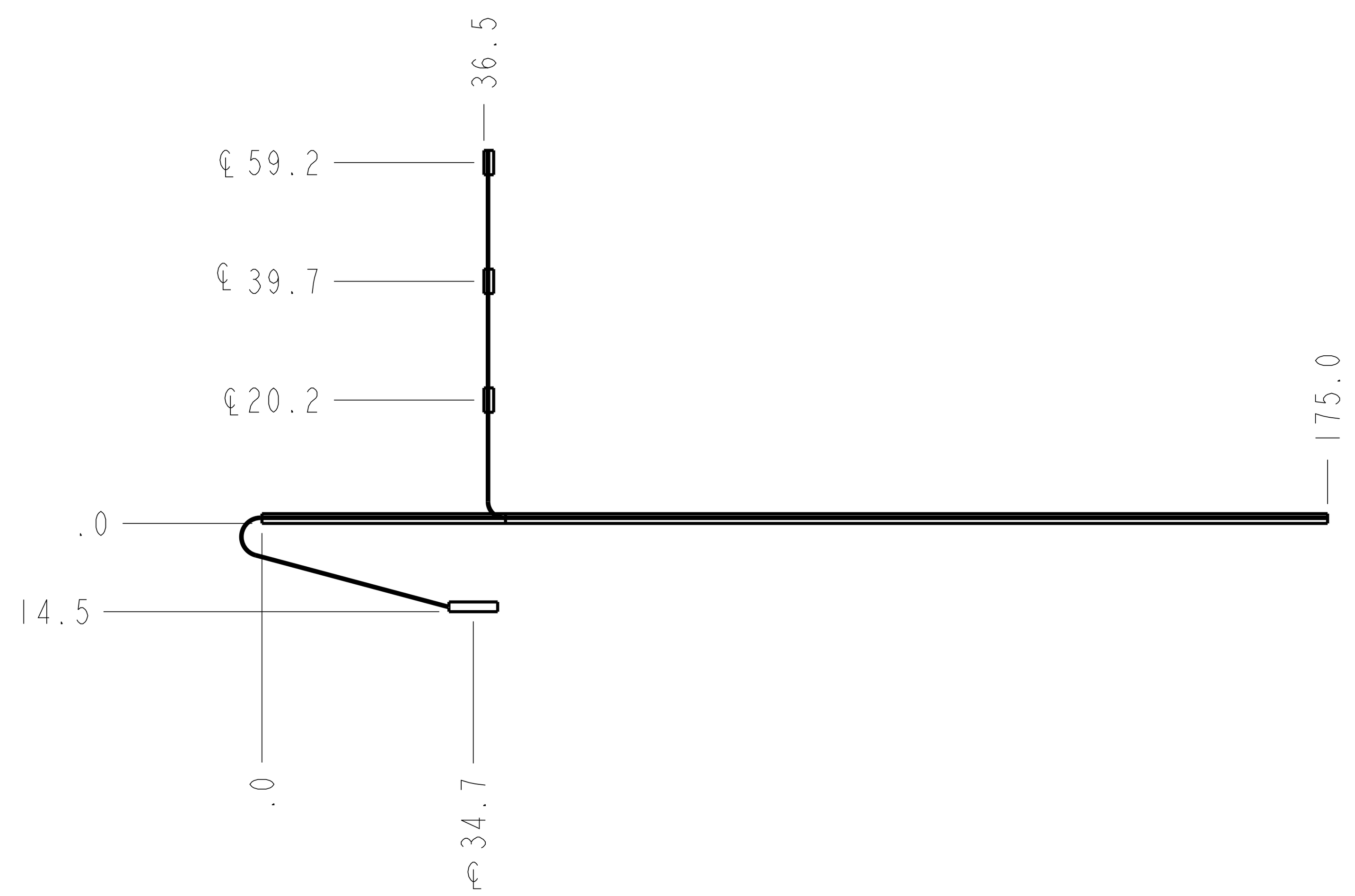
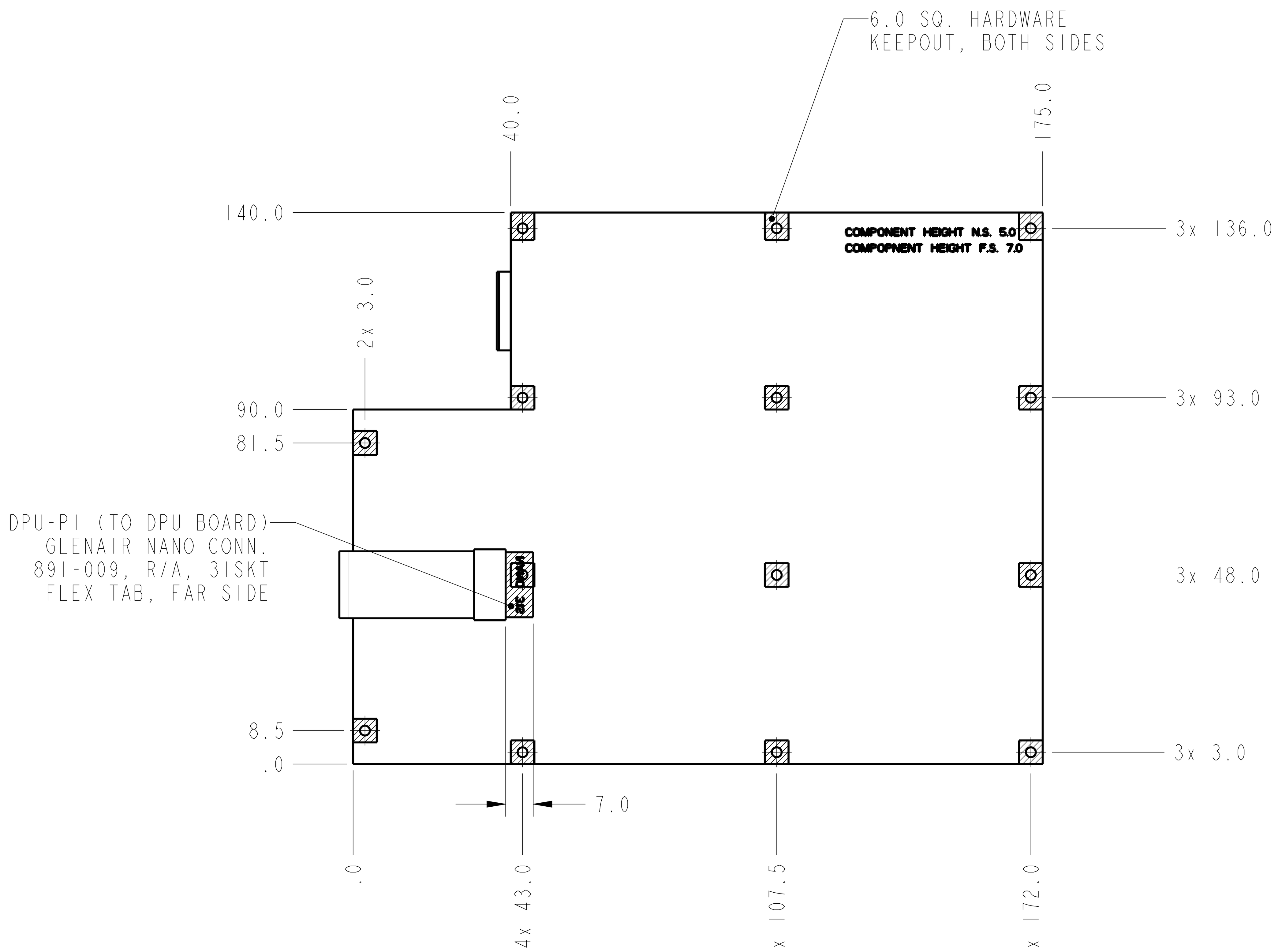
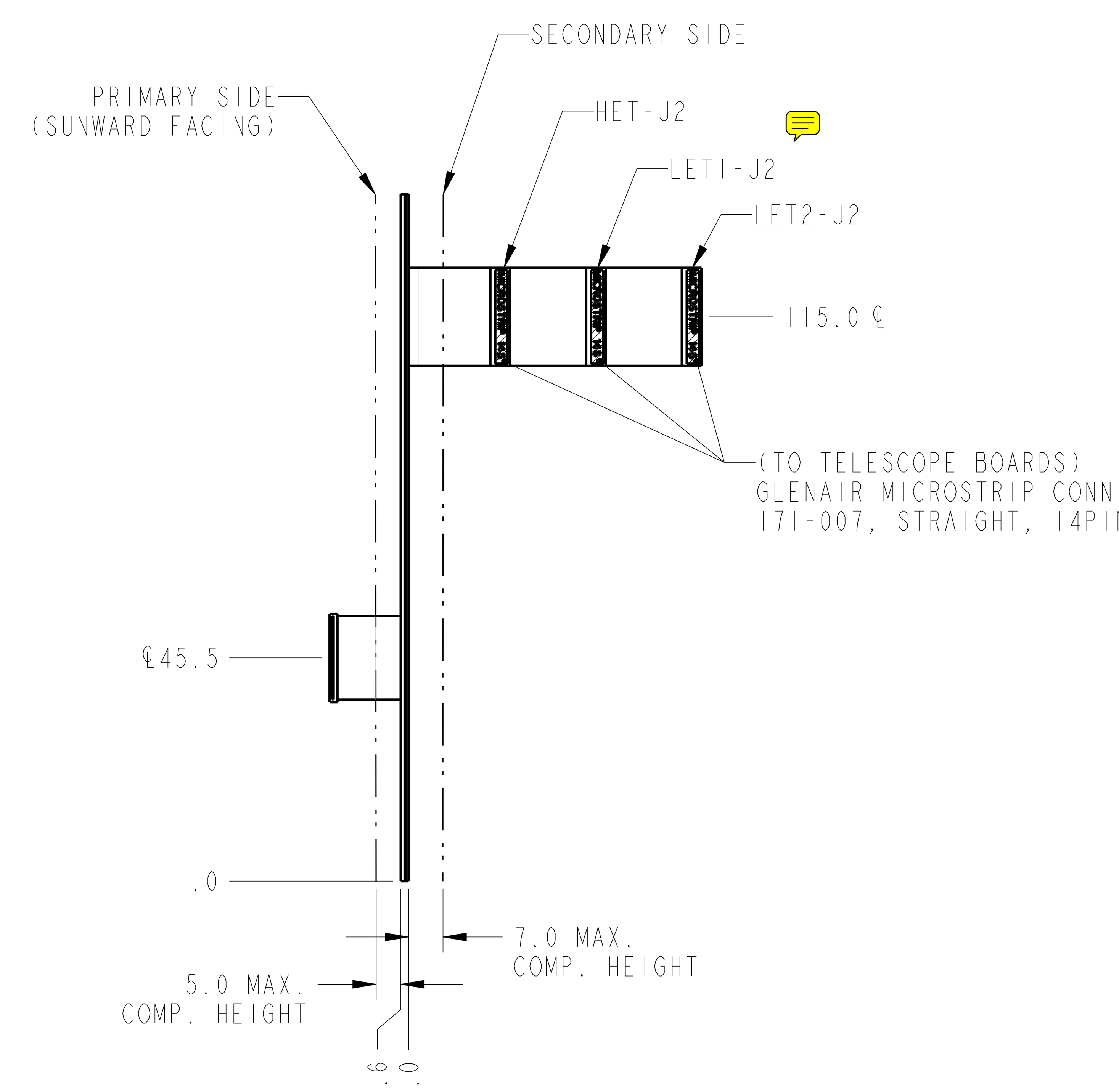


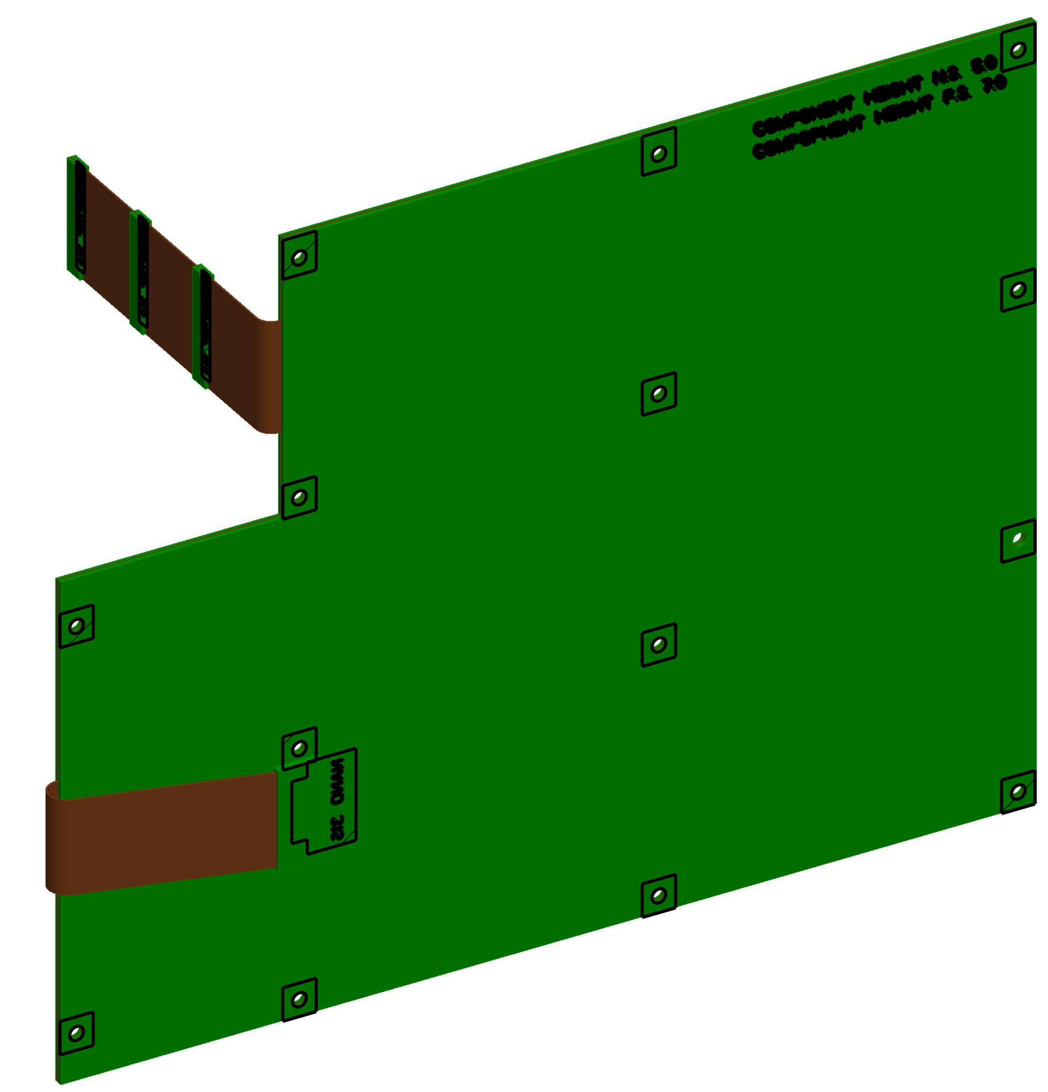
Figure 7-4 Detector placement & spacing in the High Energy Telescope

REV	ZONE	DESCRIPTION	DATE	APPROVAL
-	-	-	-	-









PRELIMINARY

PLOT DATE: 08-Jul-13

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ITEM NO.	REQD	REQD	PART NO.	DESCRIPTION	MATERIAL	MAT'L SPEC OR CAGE CODE
-		X	-	PWB, POLYIMIDE FLEX, MULTI-LAYER	POLYIMIDE	-

LIST OF MATERIAL

THIRD ANGLE PROJECTION

HARDWARE CLASSIFICATION A

INCH — UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN.
HYBRID — UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MM [IN]
METRIC — UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE MM

UNLESS OTHERWISE SPECIFIED: REMOVE ALL SHARP EDGES R.010 TOLERANCES FOR INCHES: &surf_finish
.XX ±.01 .XXX ±.005 X/X ±1/16 ∠ ±.5° FINISH IN µIN

UNLESS OTHERWISE SPECIFIED: REMOVE ALL SHARP EDGES R0.25 TOLERANCES FOR METRIC:
X.XX ±0.07 X.X ±0.15 X ±0.2 ∠ ±0.5°
XX ±0.3 XXX ±0.8 XXXX ±1.5 FINISH IN µM

SOFTWARE: Pro/ENGINEER WF5.0
FILE LOCATION: \SSHUMAN\SOLAR-PROBE
DRAWING FILE: 2190793 REV -.IL9.0
MODEL FILE:ELECTRONICS-BOARD-BIAS REV -.IL9.0

NEXT ASSY	USED ON
2190794	BIAS BOARD

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION — Goddard Space Flight Center — GREENBELT, MD [X] / WALLOPS ISLAND, VA [ ]

	NAME	INIT.	DATE
DESIGNED	S. SHUMAN		
DRAWN	S. SHUMAN		
CHECKED	B. KECMAN		
APPROVED -	-		
APPROVED - ELEC ENGINEER	R. COOK		
APPROVED - SYS-ENGINEER	B. KECMAN		
APPROVED - PDL	T. vonROSENVINGE		

DRAWING INTERPRETED PER 500-PG-8700.2.5

TITLE: **OUTLINE DRAWING, BIAS ELECTRONICS, BOARD**

SIZE D | CAGE CODE 36FC1 | DWG NO. 2190793 | REV -

SCALE: 1.000 | SHEET: 1 OF 1

GSFC 660.3/M (01/10)