

# Solar Probe Plus

*A NASA Mission to Touch the Sun*



## Integrated Science Investigation of the Sun Energetic Particles

### Preliminary Design Review

05 – 06 NOV 2013



## ISIS Power

*David Do*



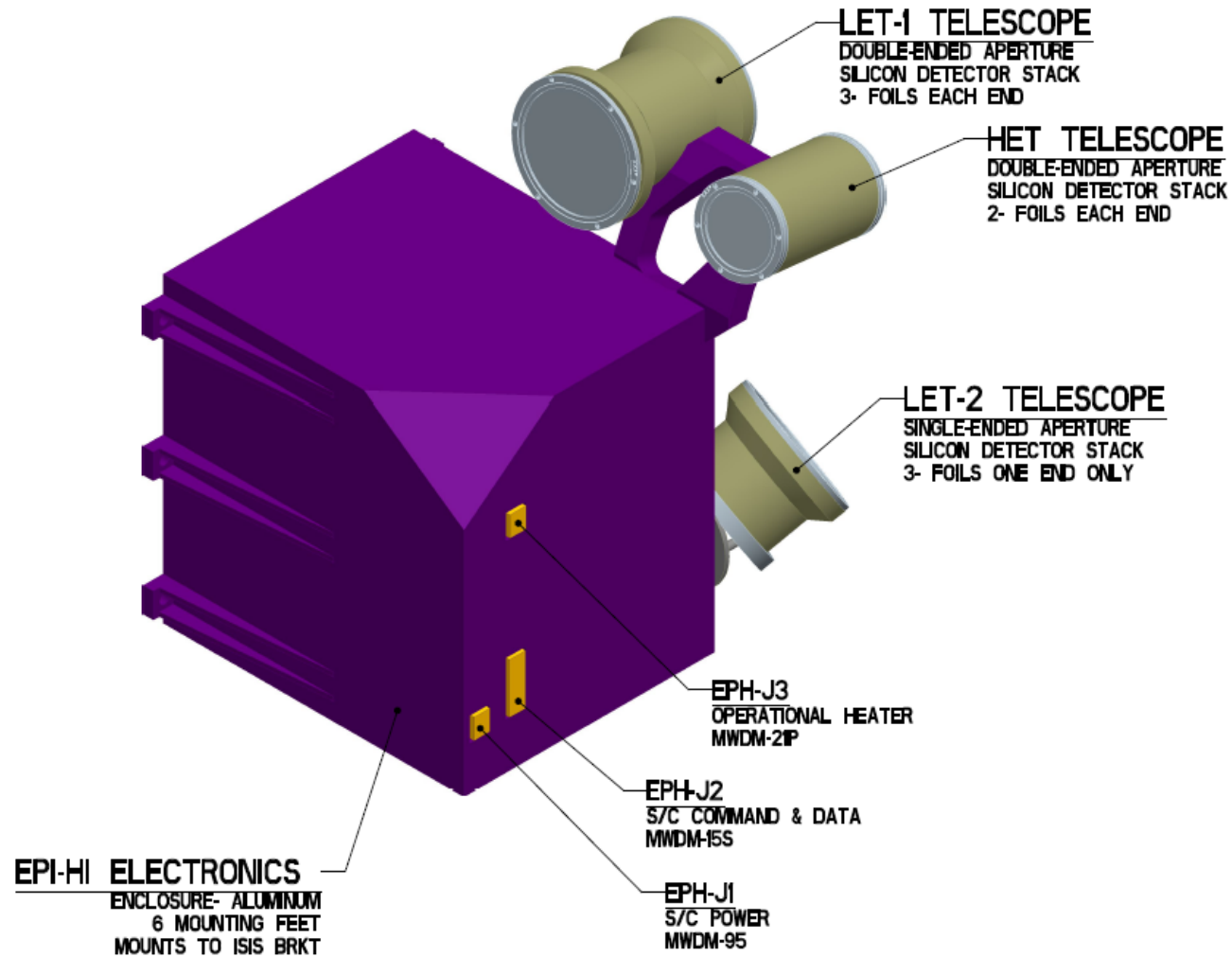
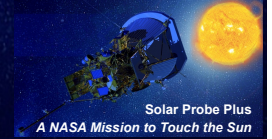
# Outline



- EPI-Lo and EPI-Hi LVPS
  - Power requirements
  - Block diagrams
  - Circuit topologies and descriptions
  - Circuit margins
  - Packaging
  - Thermal management
- Plans for testing including bench checkout equipment
- Maturity of the design (BB testing, design, analysis completed)
- Preliminary parts lists and any special testing required
- Summary and follow-up from peer review held prior to the instrument PDR



# EPI-Hi Electronics Overview





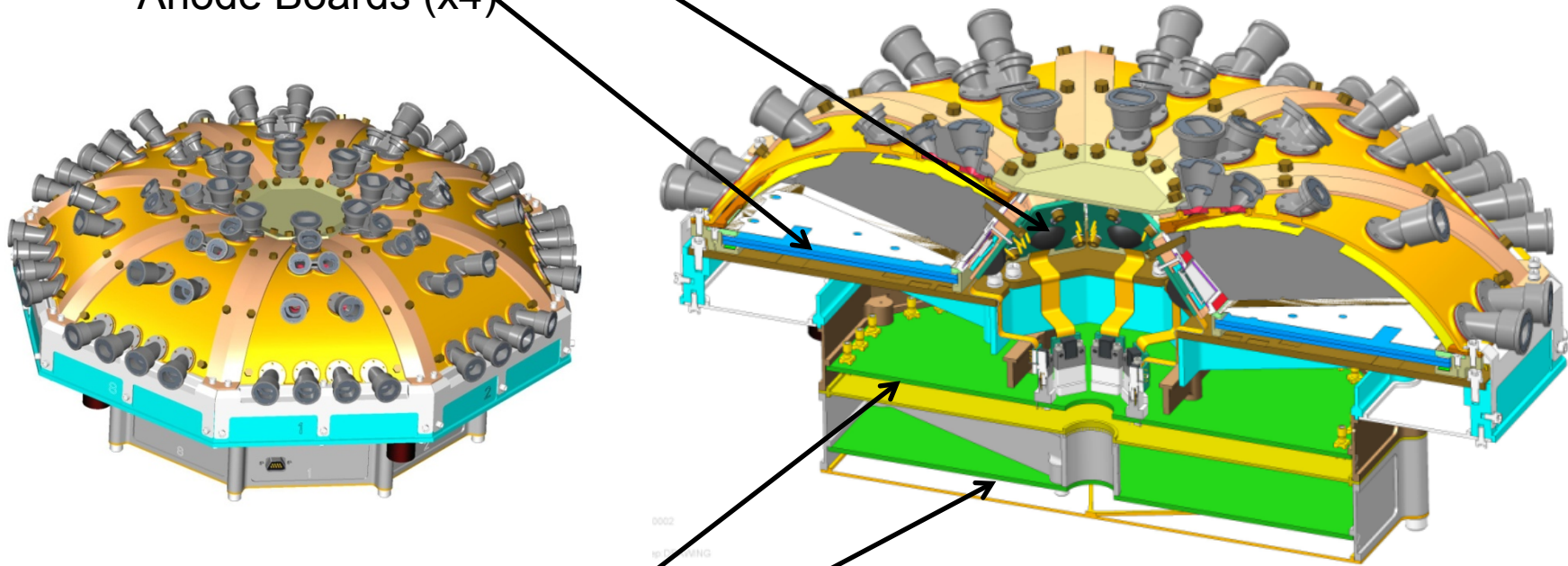


# EPI-Lo – Electronics Overview



Energy Boards (x8)

Anode Boards (x4)

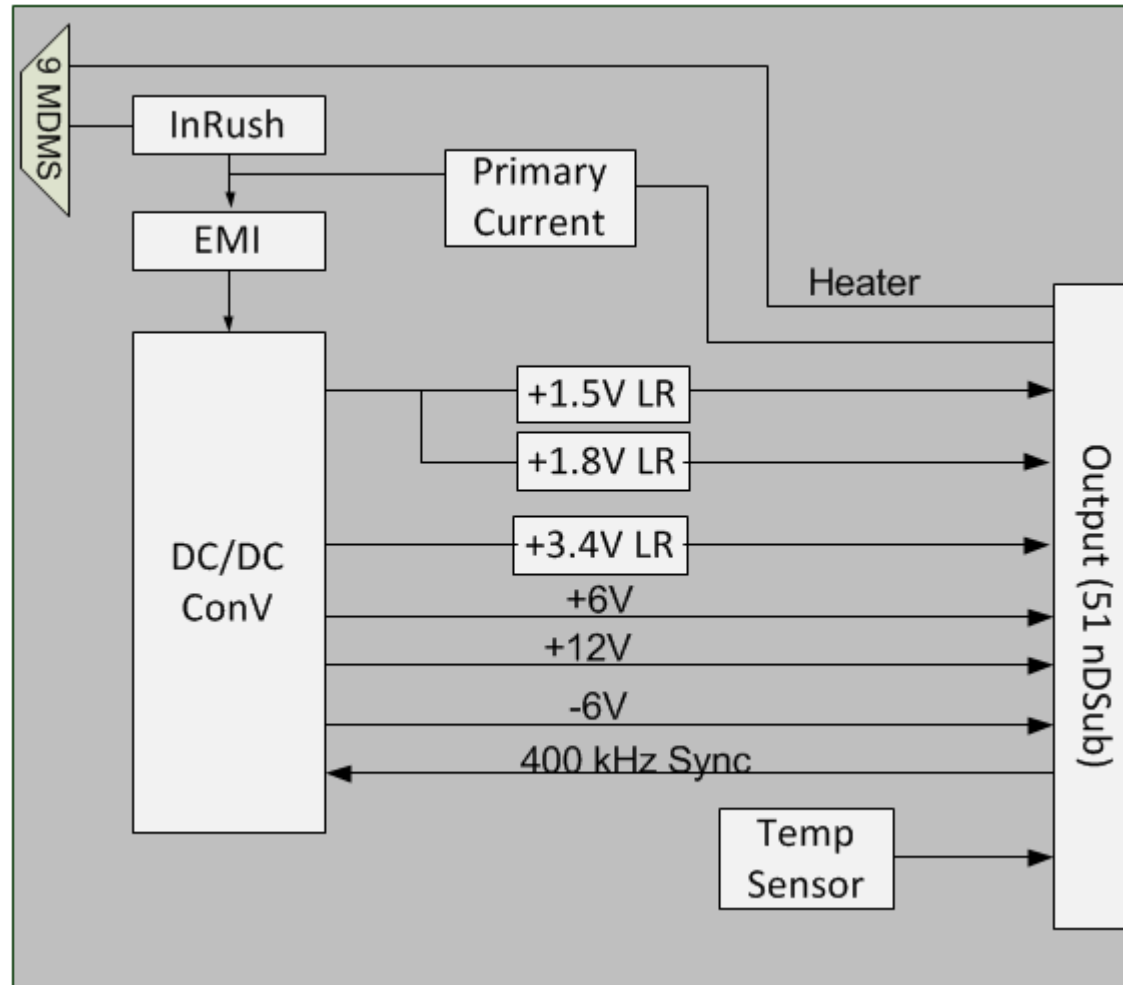


Event Board

Power Board

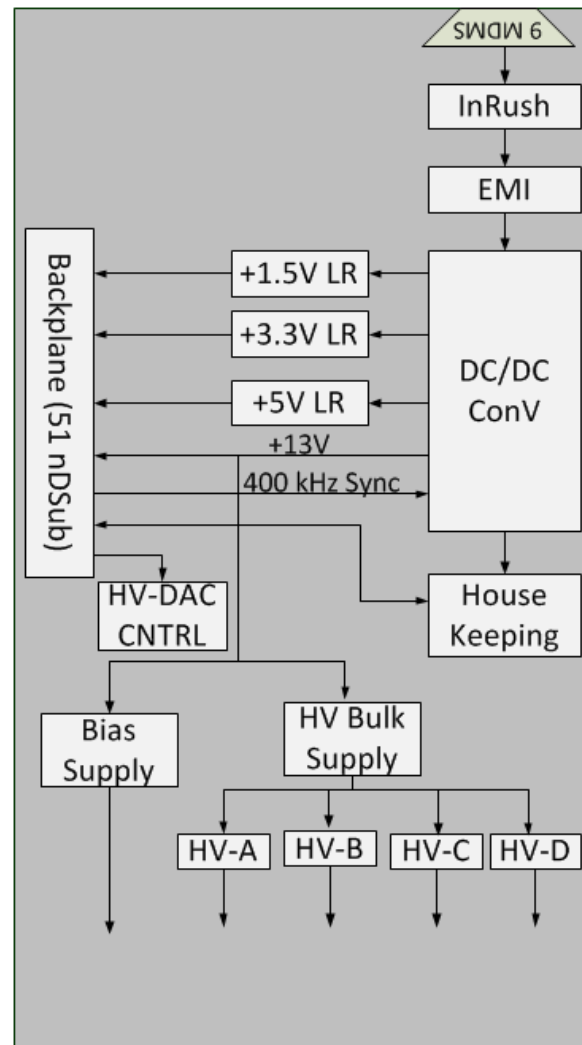


# EPI-Hi Block Diagram





# EPI-Lo Block Diagram





# Environment Requirements

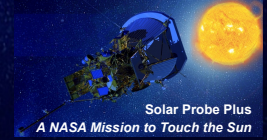


- Thermal
  - Survival is -55C to +75C
  - Operational is -20C to +55C
  - Turn-on at -30C
  - Qualification Test -30C to +65C
- Radiation
  - 75 kRad (includes F<sub>DM=Z</sub>)
  - LET > 70 MeV\*cm<sup>2</sup>/ mg
    - For LET < 70 MeV\*cm<sup>2</sup>/ mg appropriate SEE mitigation shall be applied

update



# LVPS Major Input Requirements

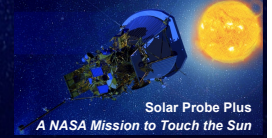


- Requirements from Solar Probe Bus
- Input Specification
  - Operate over bus voltage of 24 to 35V
  - Survive any standing or fluctuating voltage from 0 to 40V
  - Meet EMI/EMC
  - Inrush current limit
  - Primary Secondary isolation  $>1\text{M}\Omega$
  - Overall efficiency  $> 70\%$

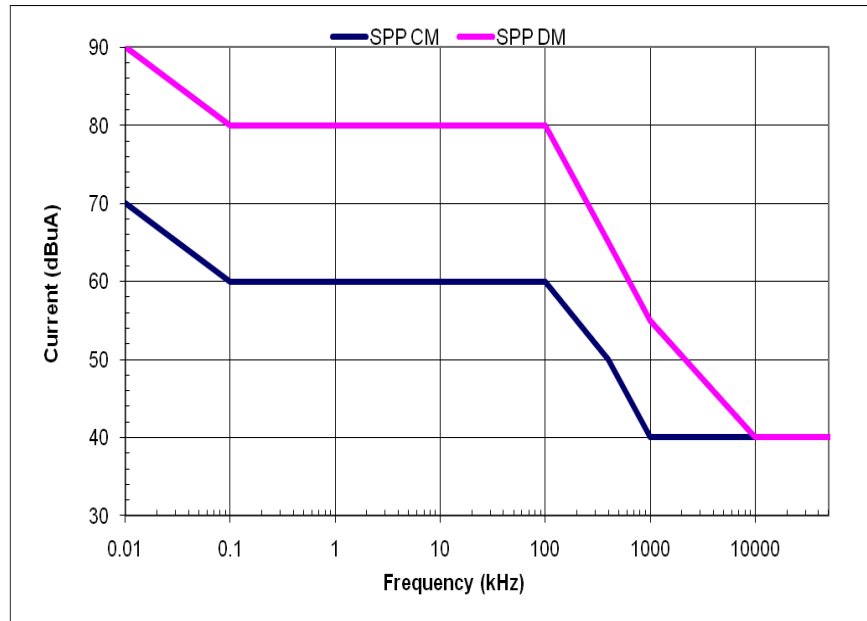




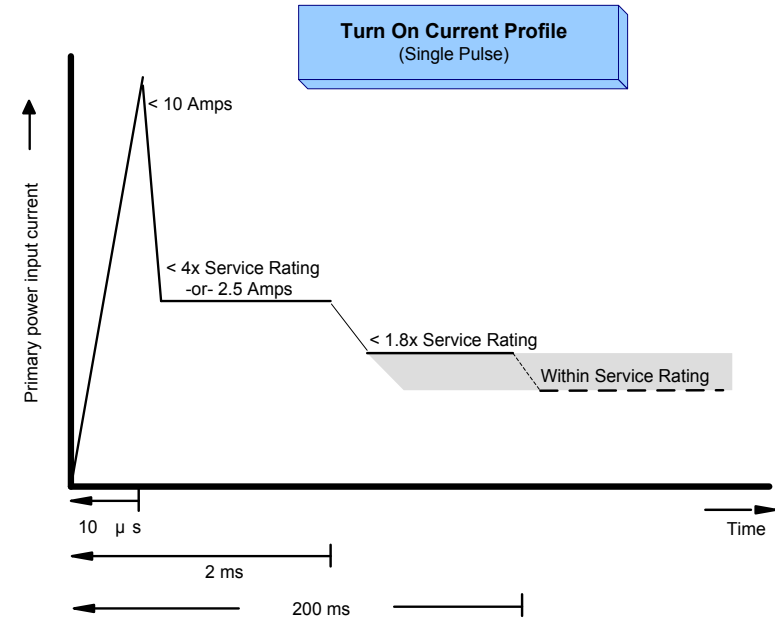
# Input Power Requirement



- EMI/EMC
- Inrush Current



CE01& CE03 Limit



In-Rush Current Limit



# Output Requirements:



- EPI-Hi:
  - Generate low voltages: +12V, +6V, +3.3V, +1.8V, +1.5V & -6V
  - Primary input current telemetry
  - Temp sensor
  - Provide path for heater voltage
  
- EPI-Lo:
  - Generate low voltages: +13V, +5V, +3.3V and +1.5V
  - House keeping through ADC for primary input current, temperature, output currents and output voltages
  - Generate high voltages and bias voltages to sensors



# Interface



- EPI-Hi
  - Input connector: MWDM2L-9SCBRR2-0.110-429
  - Output connector: 891-008-51PSBRT1T-429TH
  
- EPI-Lo
  - Input connector: MWDM\_L-9SSMR
  - Inter board connector: 891-008-51PSBRT1T-429
  - Safing connector: 803-005-07M5-3EN
  - Bias voltage connector: 09-9001-1
  - High voltage: Pig tails



# Power Topology



- Common for EPI-Hi and EPI-Lo:
  - Main converter is forward with resonant reset operating at 200kHz. Efficiency is >80%.
  - Digital voltages are linear regulated
- EPI-Lo HVPS:
  - Bulk high voltage is set at 3.5kV
  - High voltages of up to 3.4kV are controlled through Optocouplers
  - Bias voltage is up to 200V





# EPI-Hi Output Requirements



	Output Regulation	Min Load (mA)	Nom Load (mA)	Max Load (mA)
+1.53V	±2.5%	50	100	150
+1.82V	±2.5%	20	40	60
+3.41V	±2.5%	145	287	430
+6V	±5%	79	338	500
+12V	±7%	8	16	64
-6V	±7%	6	12.6	19



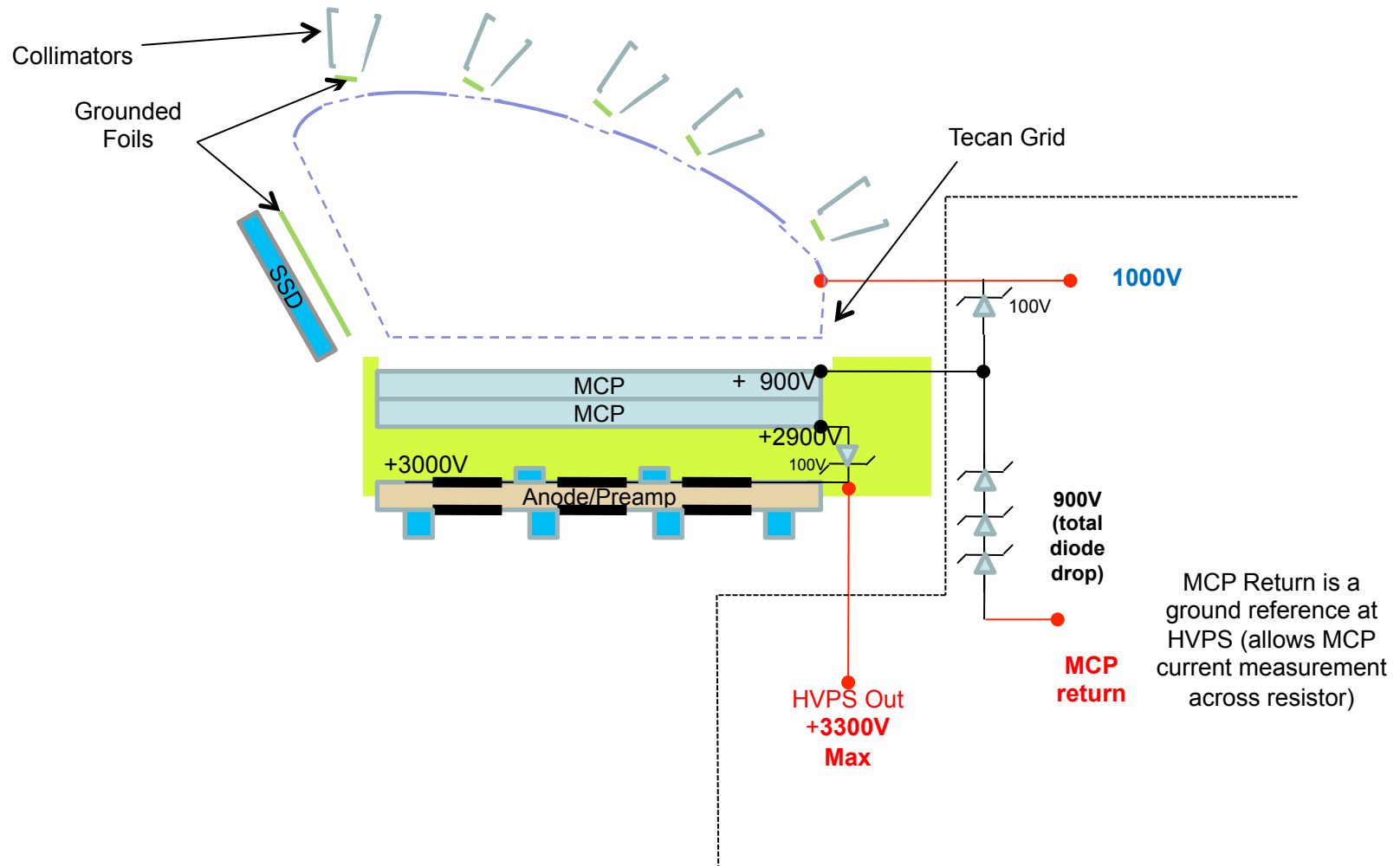
# EPI-Lo Output Requirement



	Outputs Regulation	Min Load (mA)	Nom Load (mA)	Max Load (mA)
+1.5V	±3%	45	80	200
+3.3V	±3%	150	200	460
+5V	±5%	115	135	160
+13V	±5%	10	63	90



# Sensor Voltages





# EPI-Lo HVPS Requirements



	Max Output Voltage (V)	Min Load (uA)	Max Load (uA)
Bias	200	0	20
Bulk	3400	0	250
HVPS	3300	0	40
Grid	1000	0	1
MCP	900	0	40





# HVPS Current Limit



- Control range: 0uA to 125uA
- Control granularity: <1uA
- Response time: <1ms



# LVDS Fault Mitigation



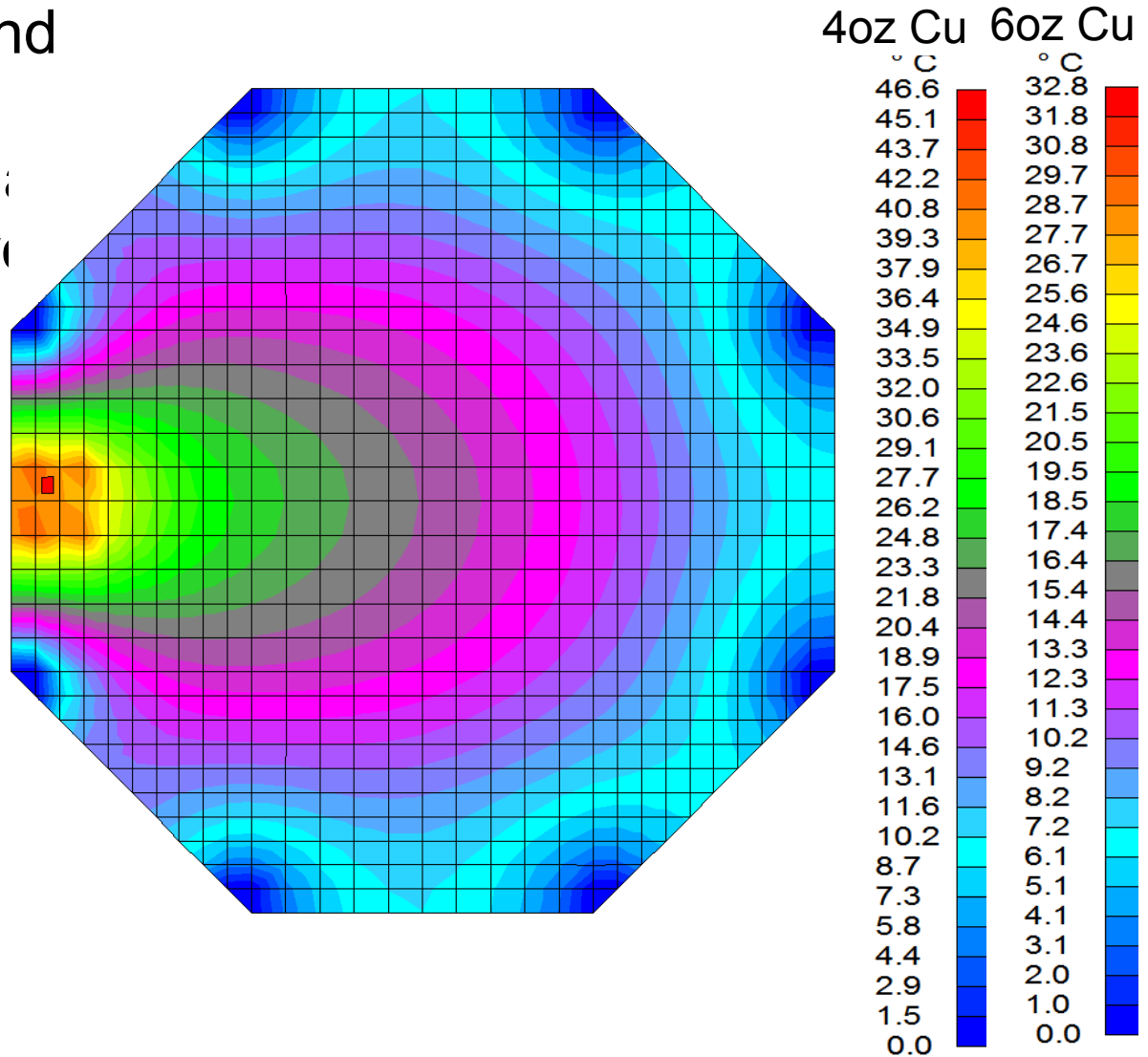
- Transformer: primary and 3.3V winding is well isolated
- +3.3V is linear regulated from +3.6V
- Linear pass transistor is rated for 100V
- Preliminary thermal analysis shows 33°C rise



# Thermal Analysis

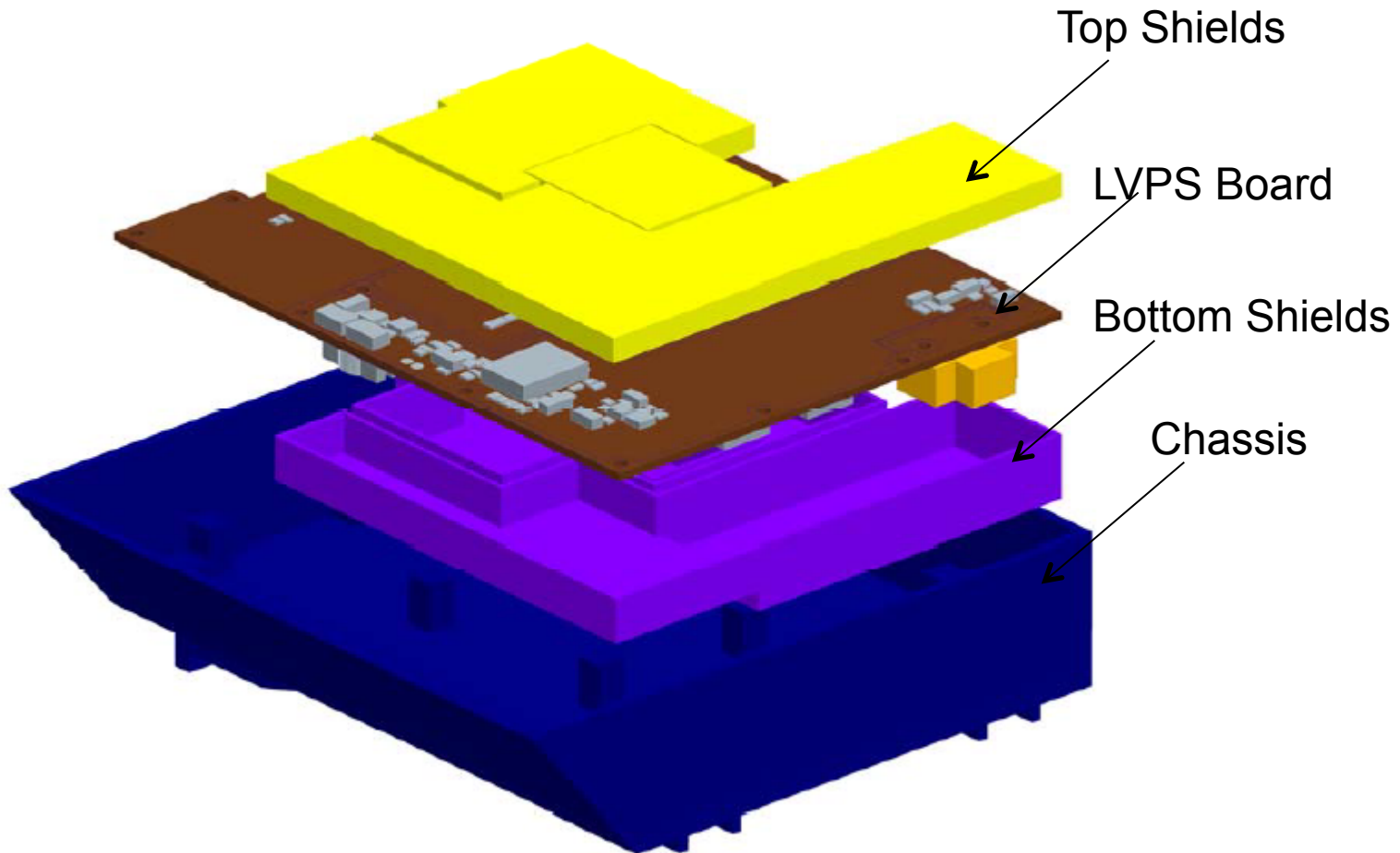


- Ran two cases: 4 oz and 6 oz Cu in PWB
- Thermal contours similar; one plot shown with two contour levels for each PWB case
- TO-254 temps for 4oz
  - Junction = 46.6°C
  - Case = 27.0°C
- TO-254 temps for 6oz
  - Junction = 32.8°C
  - Case = 13.2°C





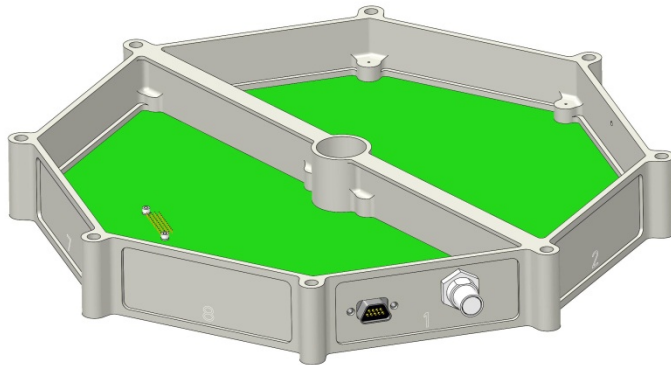
# EPI-Hi Package







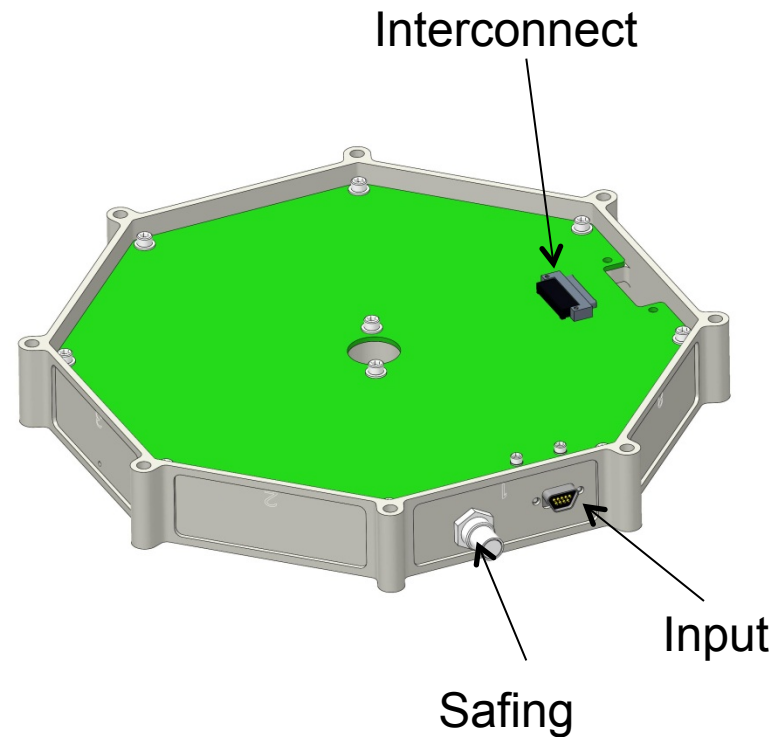
# EPI-Lo Packaging



Packaged in octagon frame

Stiffener goes across the board

Power dissipation is estimated  $<1.5W$

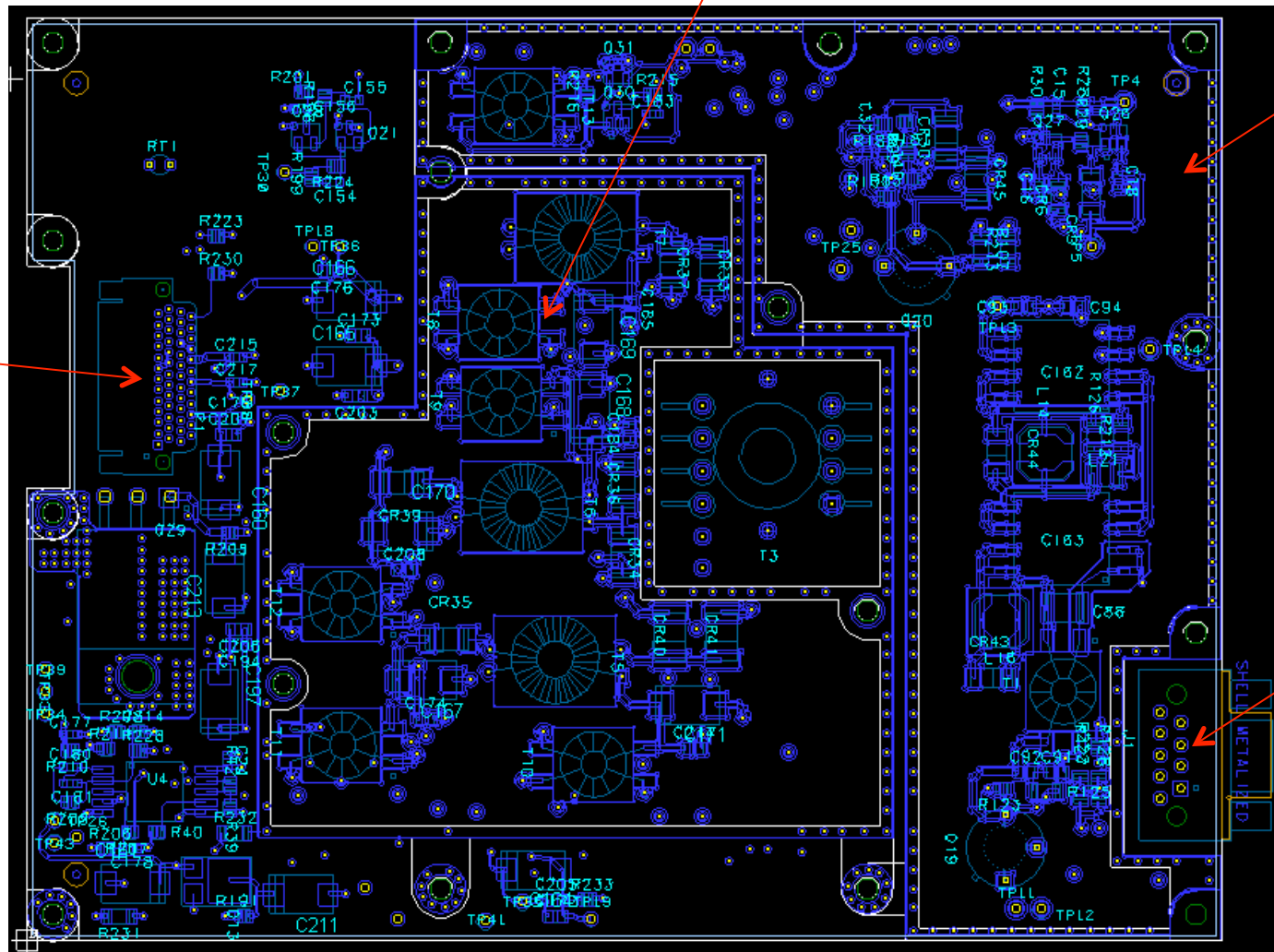




## Primary Shield

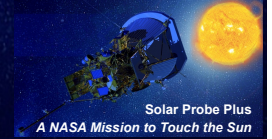
## Output

## Input



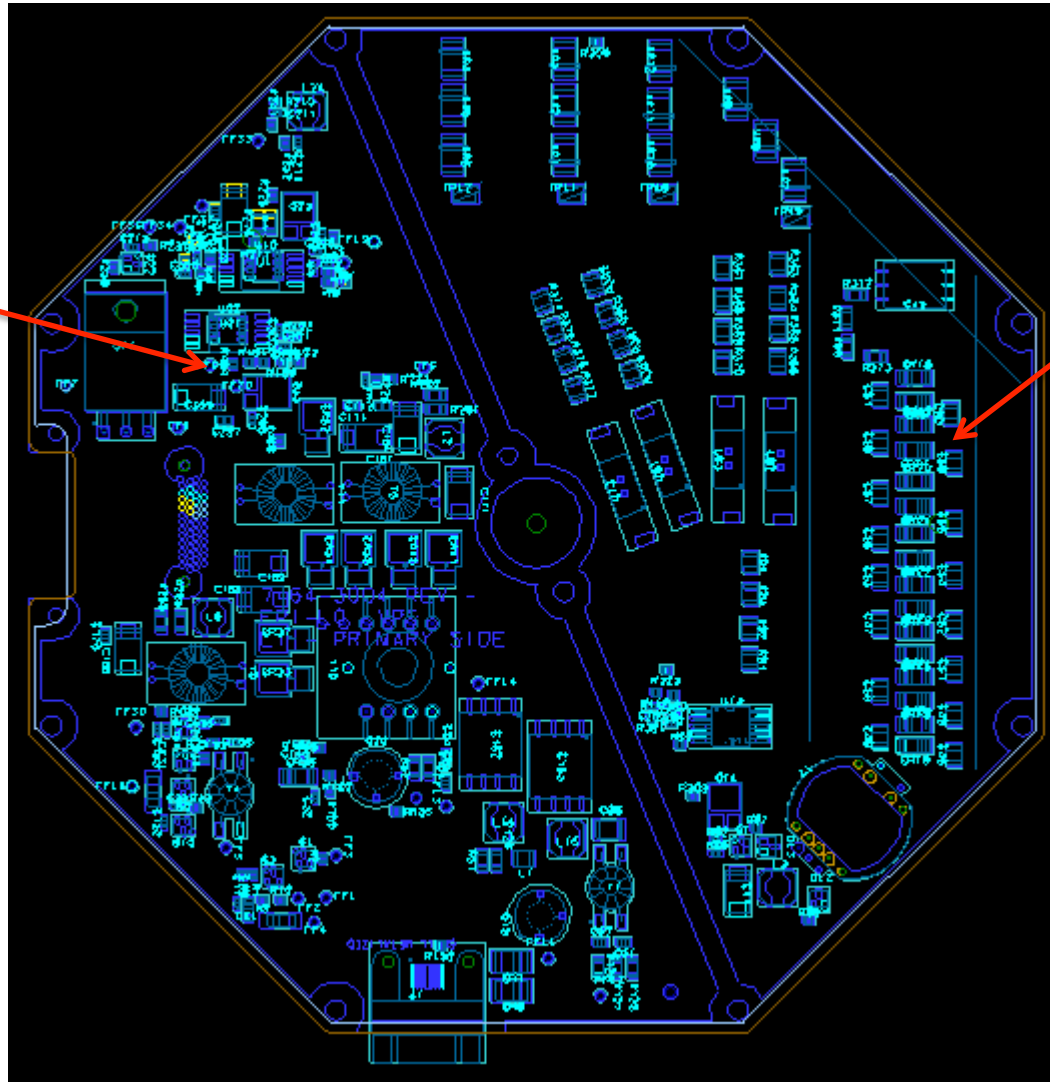


# EPI-Lo Board Placement



LVPS

HVPS





# Plans for testing

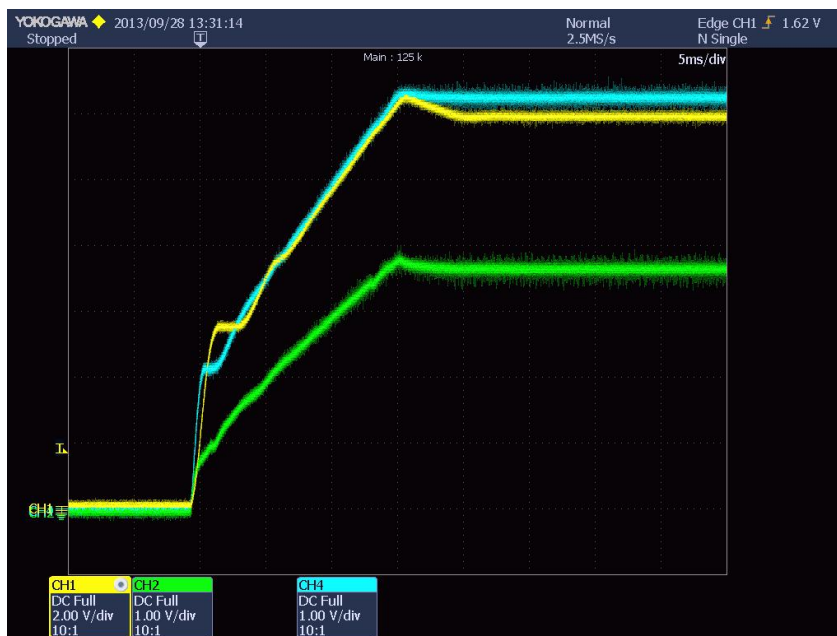


- Follows APL Manufacturing Flow, these are significant highlights
  - Populate Passive Components with Automatic Measurement.
  - Populate Actives and Install Known Tailors or Tailor Flags
  - Install into Flight Frame
  - Execute Test Procedure to Test and Tailor Entire Board
  - ESS Testing
  - Execute Functional Test Procedure
  - Photograph and Conformal Coat
  - Execute Test Procedure to Calibrate and Characterize Board (over temperature)
  - Release to Next Assembly





# Breadboard Testings



Start Up



Transformer Reset



# Output Regulation and Efficiency



	Load(A)	Regulation(V)	Power(W)
+1.53V	0.14	1.505	0.2107
+3.41V	0.287	3.69*	0.9758
+6V	0.338	5.97	2.01786
+12V	0.016	11.98	0.19168
-6V	0.012	5.95	0.0714
input	0.159	28	4.452
			78%

- \*+3.41V shown preregulated. Efficiency is calculated using +3.4V.
- +3.41V and +1.82V linear regulator have same design as +1.53V.



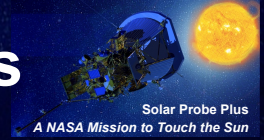
# Analysis



- Preliminary EMI completed
- Worst Case analysis for digital voltages completed:  $\pm 2.3\%$



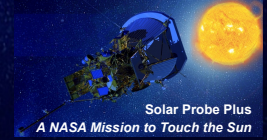
# Voltage Regulation WCA Method and Assumptions



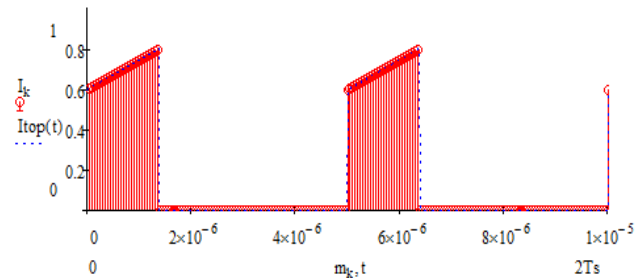
- WCA Method
  - Extreme Value Analysis in Mathcad
- Temperature Range
  - -20C to +65C operational
- Resistors Variation
  - K resistors are 100 ppm (0.8%) + 1% initial tolerance + 2% Aging  $\approx$  4%
  - E resistors are 25 ppm (0.2%) + 0.1% initial tolerance + 1% Aging  $\approx$  1.3%
  - Z resistor are 5ppm(0.04%)+ 0.01% initial tolerance 0.16% Aging  $\approx$  0.2%
- RH1078
  - 100Krad data from datasheet
- PWM5302S
  - 100Krad data from datasheet



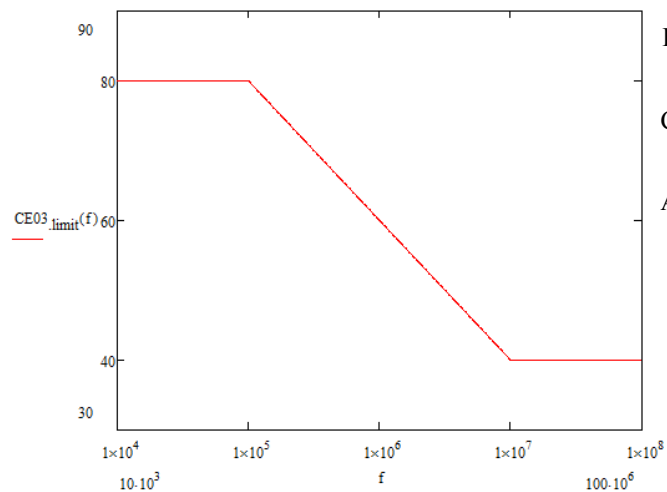
# EPI-Lo EMI Analysis



Waveform in time



Primary Current in Discrete Time

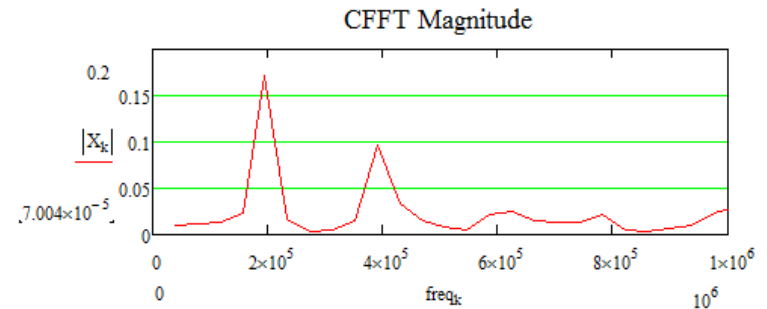


CE03 Limit

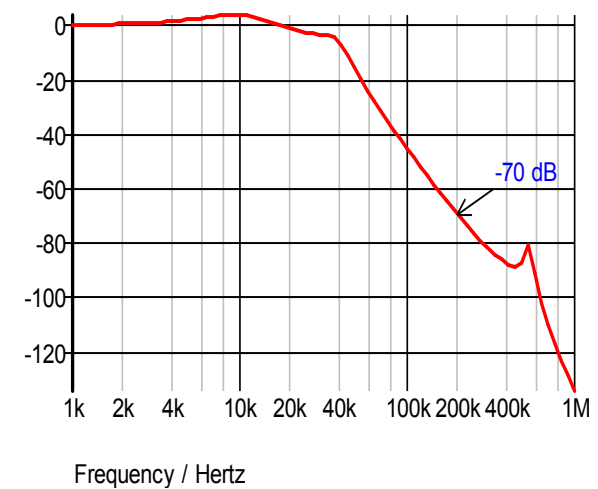
$$I_{in_{dB}} := 20 \log \left( \frac{\text{peak}}{\mu A} \right) = 104.725$$

$$CE03_{limit}(200kHz) = 73.979$$

$$Aten := I_{in_{dB}} - CE03_{limit} \left( \frac{1}{T_s} \right) = 30.746$$



Primary Current in CFFT



EMI Filter Attenuation





# Parts



- All parts are rad-hard to 100krad
- No parts concerns

Add table of parts



# Status Summary



- EPI-Hi
  - EM PCB Fabricated
- EPI-Lo
  - EM Placement completed
  - EM Board is in layout phase



# Plan Forward



- EPI-Hi
  - Complete testing EM
  - Fabricate flight
- EPI-Lo
  - Fabricate and completing testing EM
  - Fabricate flight
- Finalize all documentation and procedures for flight build
- Build, tailor, calibrate, and qualify flight units



# Peer Reviews



- EPI-Hi LVPS: May 2013
- EPI-Lo Power: Aug 2013
- Major Action Items:
  - EPI-Hi:
    - Shielding over switching circuits
    - Output loads
    - Output regulations
  - EPI-Lo:
    - MCP voltage accuracy
    - LVDS fault mitigation
    - Bias Voltage Zener diode protection