Solar Probe Plus

A NASA Mission to Touch the Sun

Integrated Science Investigation of the Sun Energetic Particles

Preliminary Design Review

05 – 06 NOV 2013

EPI-Hi Electronics

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Electronics System Overview

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Key Driving Requirements

Solar Probe Plus
A NASA Mission to Touch the Sun

- Support three independent charged particle telescopes: LET1, LET2 and HET.
- For each telescope provide for detection of coincident signals from various Si detector elements to define “events” caused by the incidence of individual nuclei, electrons and neutral particles/photons.
- For each event, provide pulse height analysis of the signal amplitudes in the various stimulated detector elements. Large dynamic range is needed for measurement of electrons through Zn nuclei.
- Sort and count the events according to particle type and energy.
- Integrate the counts for the various particle/energy categories over time periods ranging from seconds to hours.
- Format the count rate data into packets and transmit them to the s/c.
- Include in data packets the raw pulse height data for a sample of events to aid in-flight calibration.
- Monitor instrument health by measurement of detector leakage currents, instrument temperatures, power supply voltages and total instrument current draw, and include this “housekeeping” data in telemetry packets.
- Respond to commands for altering threshold voltages, bias voltages, etc. and performing instrument self-tests and auxilliary functions.
- Control instrument operational heaters.

Constraints and their Implications

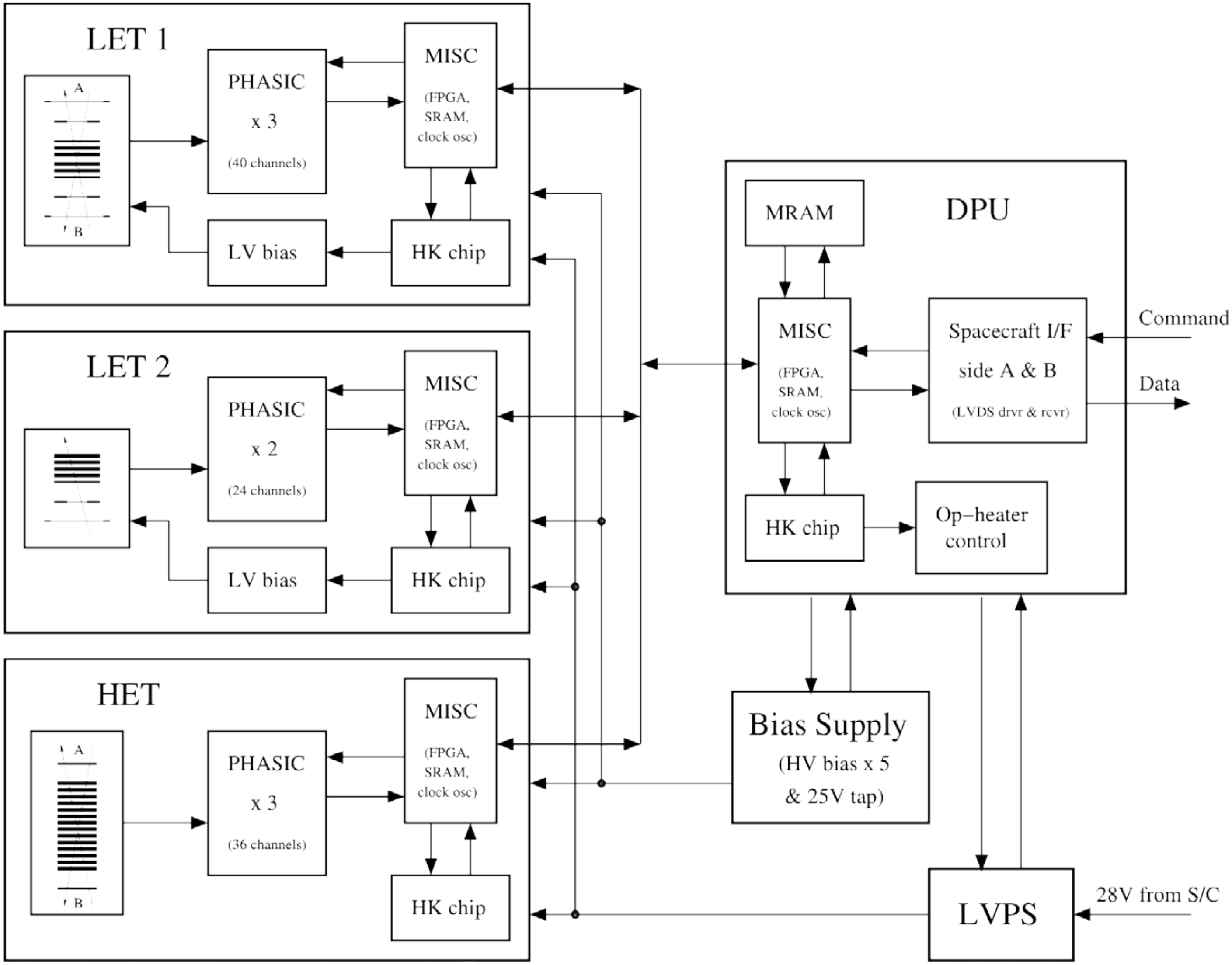
Constraints

- Both power and mass are very tightly constrained
- Design should be single string, yet reliable
- Primary data collection occurs when s/c cannot communicate with Earth
- Radiation environment is more severe than in typical mission

Implications

- Reliability through minimization of parts count and use of “natural” redundancy
- Use of custom radhard VLSI: PHASIC and HKCHIP
- Design should be “bullet proof” with regard to radiation affects: no latch-up, no processor crash due to SEU, total dose tolerant > 100 kRad
- Design should be capable of autonomous operation during primary data collection period (<0.25 AU from sun)

EPI-Hi Block Diagram



Key Features

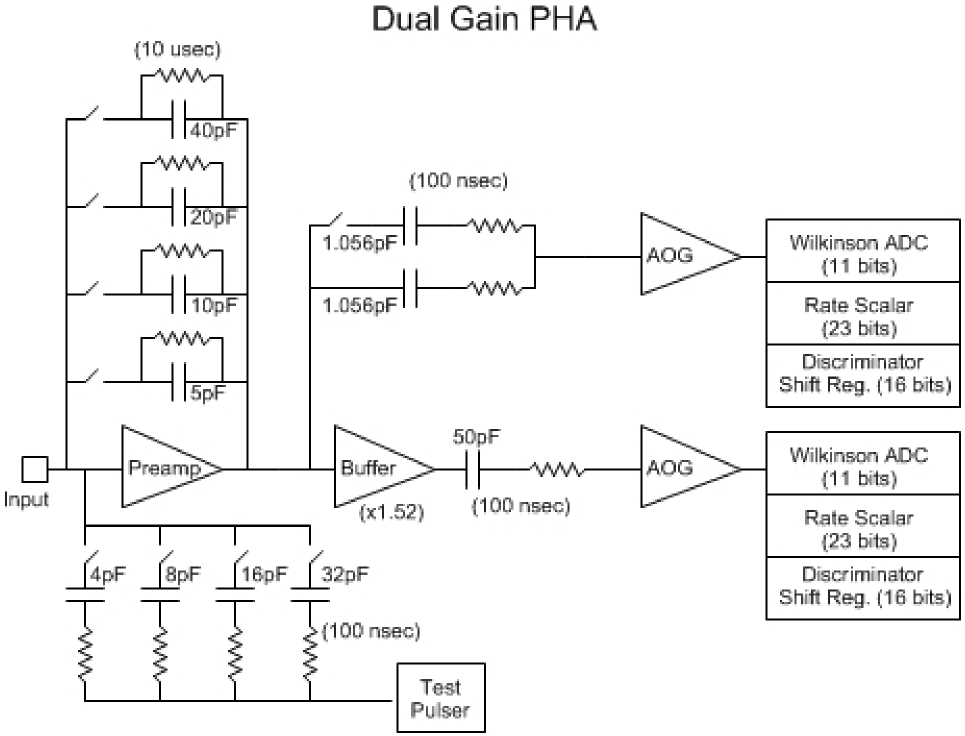
- Each telescope supported by independent electronics board including PHASICs, processor (MISC) and HKCHIP.
- A separate DPU board provides a processor dedicated to formatting data and providing a single point interface with s/c.
- Low Voltage Power Supply (LVPS) and Bias Supply board are shared.
- Bias Supply board contains separate supplies for separate telescope “ends”. (limited redundancy)
- Logic and processors are implemented within RTAX 250 FPGAs. A single FPGA is used on each telescope board and on the DPU board.
- Large system heritage from earlier projects: STEREO and NuSTAR.

Instrument to S/C Electrical Interfaces

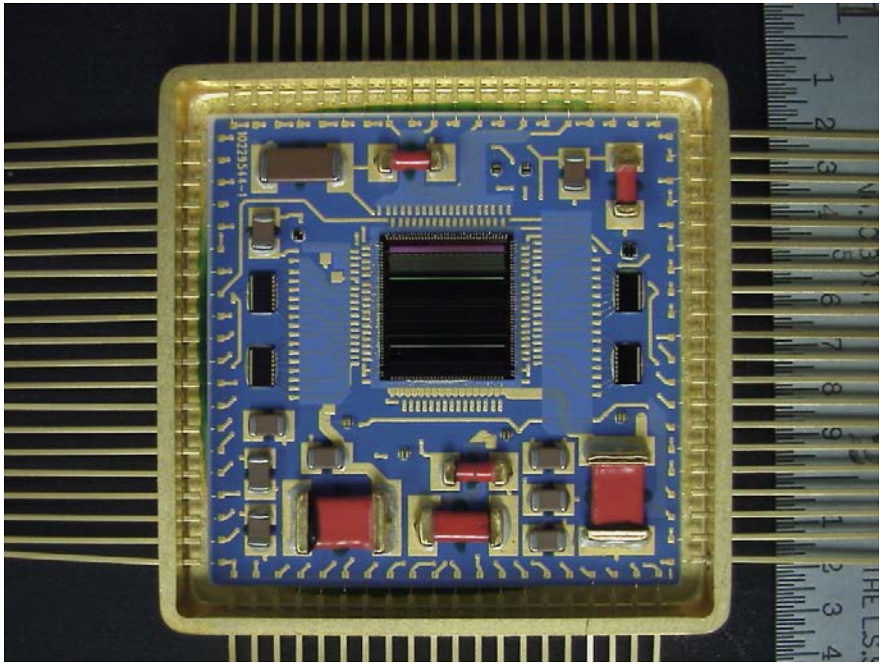
- Interfaces with S/C specified by ICD under APL control
- Command and data interfaces with S/C go through DPU board, have redundant A and B sides
- Both command and data interfaces are 115.2 kbaud LVDS using radhard drivers/receivers specified by APL.
- Reset and Timing signals removed from interface by APL for simplicity. Functions included in command signal protocol.
- MISC boot method has been modified to accommodate lack of Reset signal.
- S/C supplies separate 30V power services for survival and operational heaters.
- S/C monitors instrument temp via S/C supplied thermistors.

PHASIC Overview

- PHASIC stand for “pulse height analysis system integrated circuit”
- Originally developed and used in NASA’s STEREO mission.
- Each PHASIC contains 16 complete dual gain pulse height analysis (PHA) chains.
- STEREO PHASICs still operational in space.
- Mods for SPP include widening dynamic range, and improving total dose tolerance to >100 krad

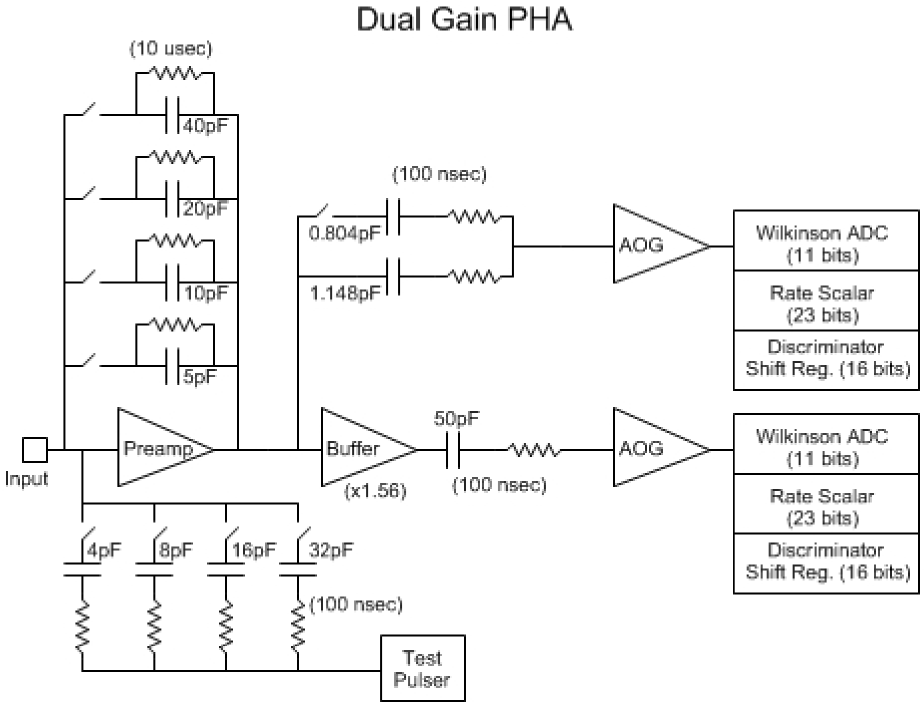


PHASIC packaging



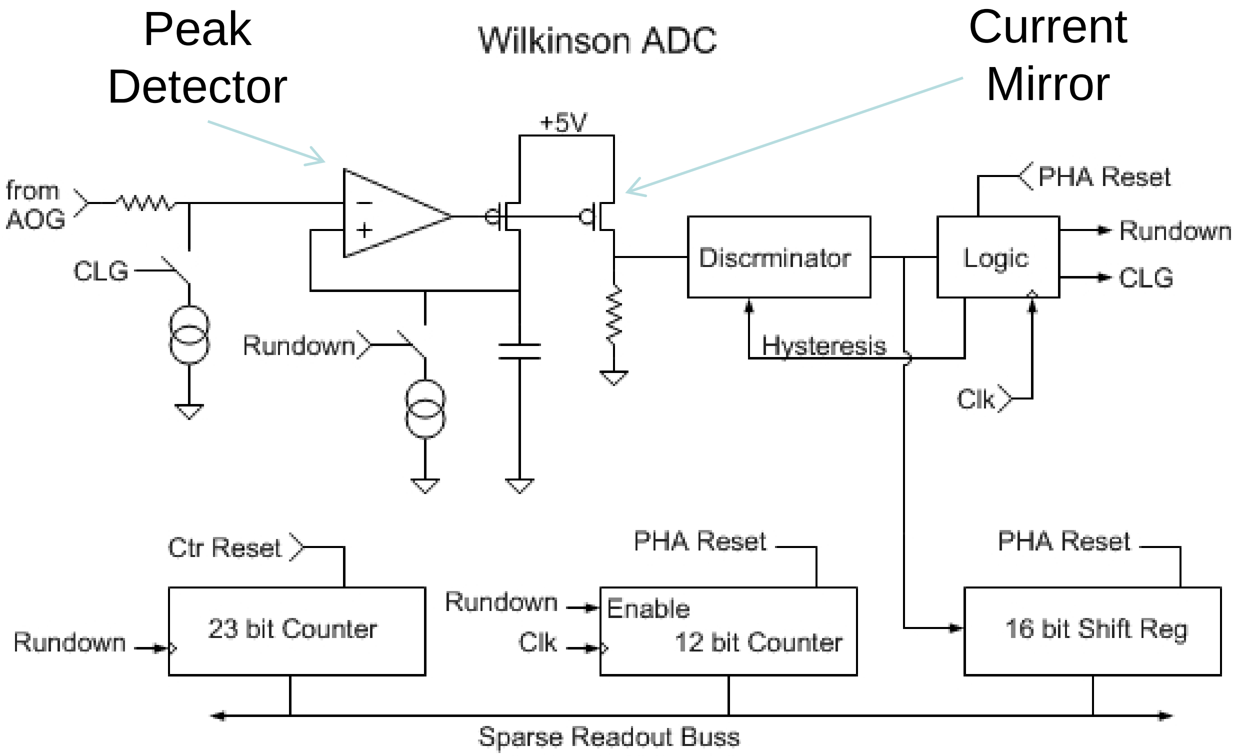
- PHASIC die is installed in an 80-pin hermetic Covar package along with a few passive components to form a “hybrid” circuit.
- Hybrid substrate design and passives same as for STEREO.
- PHASIC hybrid to be qualified and screened to class H (as on STEREO).
- Passive components include a precision resistor for each PHA chain that sets the rundown current . Allows PHA channel gain to have low <50 ppm/degC temperature coeficient.

PHASIC Mods near Preamp



- Preamp output stage changed from “follower” to “open drain” to increase output swing.
- Preamp compensation method changed for lower noise.
- Buffer added in high gain signal chain
- High/Low gain ratio increased from 20 to 68, with programmable option of 40
- High/low gain boundary falls between alphas and carbon for most detectors

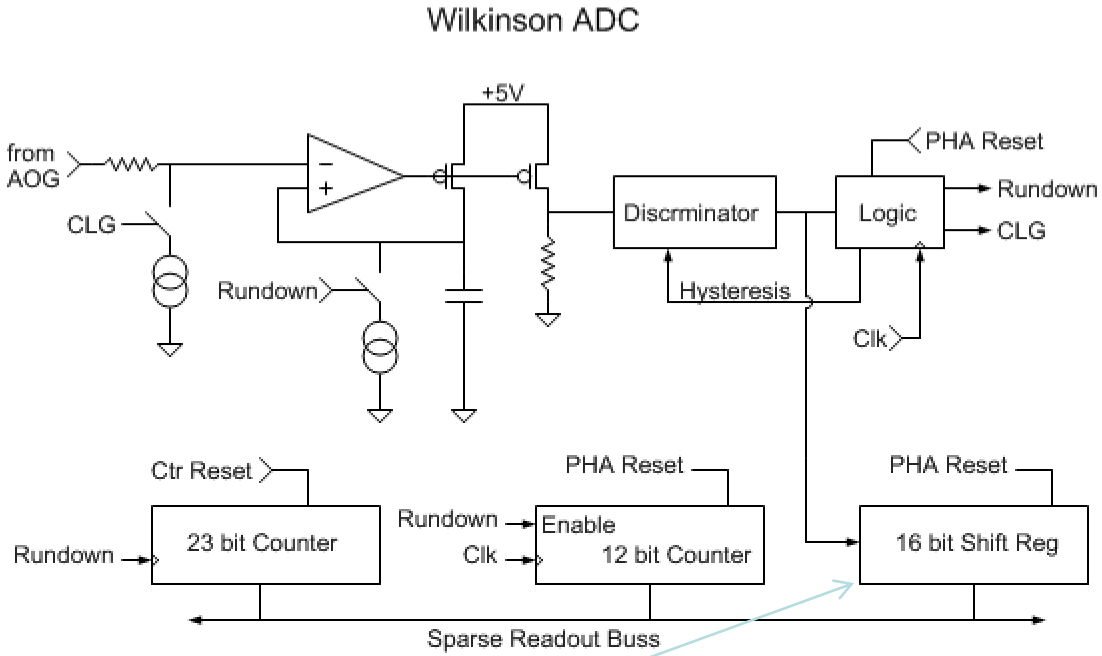
PHASIC Mods near Peak Detector


Peak Detector

Current Mirror

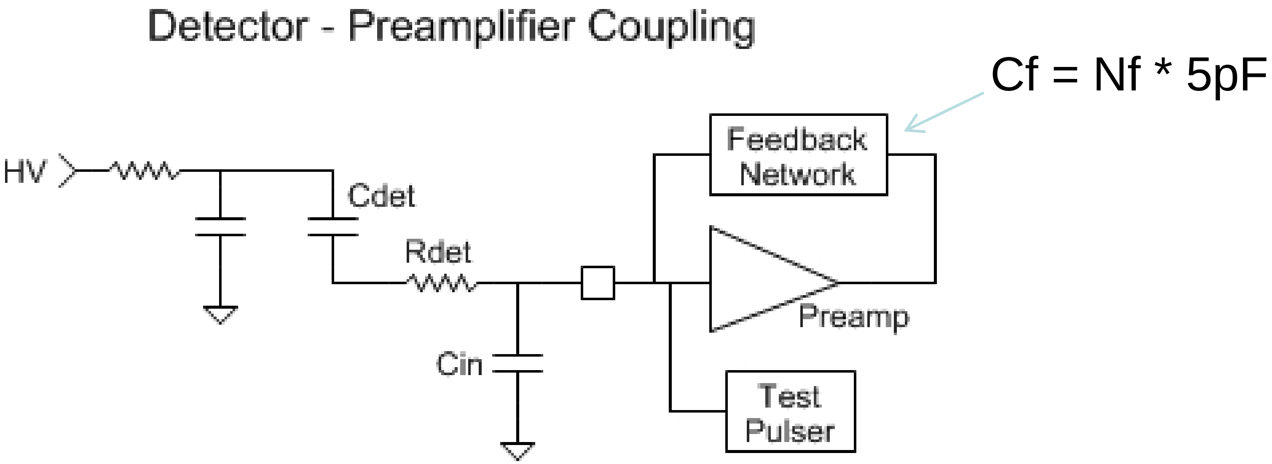
- STEREO Peak detector contained two differential amplifier stages at input. For Solar Probe reduced to one stage but with higher current resulting in lower noise.
- Size of FETs in current mirror at output increased to improve matching and threshold uniformity.

PHASIC Mods near Peak Detector cont.



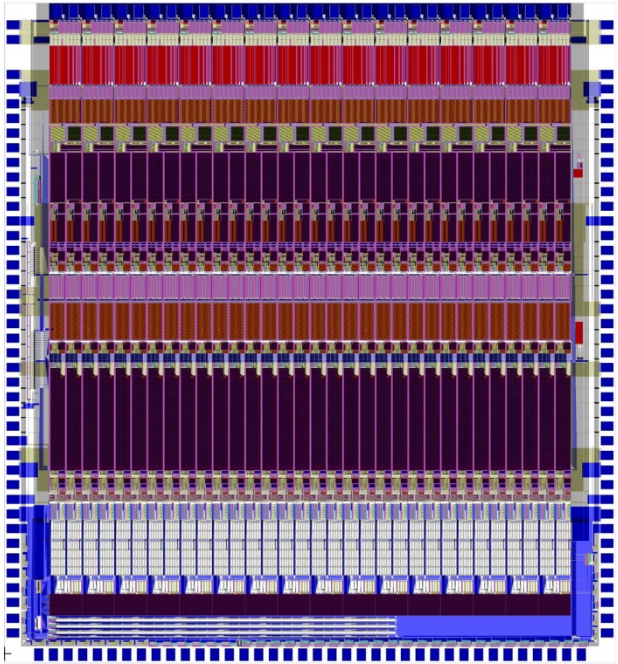
- 16 bit shift register added to capture time history of discriminator output to aid in cross-talk identification.

Predicted PHASIC noise/threshold



Det	Cdet (pF)	Rdet (ohm)	Cin (pF)	Nf	Threshold (MeV)	Full Scale (MeV)	Zn @ 45 (deg)	Freq(G.C.) (MHz)	Phase Margin (deg)
L0	208	0	30	1	0.09	268	83	12.3	98
L1	93	30	40	1	0.05	268	251	13.3	65
L2(H1)	20	10000	60	6	0.12	2802	2660	13.4	60
L3(H2)	40	7500	80	9	0.19	4337	4092	10.8	61
H3	30	15000	80	13	0.28	6155	6203	10.5	56

PHASIC Radiation Tolerance



- Total dose tolerance improved by adding proven Aeroflex processing steps to commercial ON Semi C5N CMOS process.
- Layout modified to comply with slight Aeroflex design rule differences.
- 12 krad improves to >100 krad
- Latchup threshold should still be >80 MeV/(mg-cm2) due to use of guard rings

PHASIC Status

- Engineering run though C5N commercial process was completed, yielding “EM” wafers and dice.
- EM dice installed in STEREO hybrids and tested.
- Due to need to operate some SPP channels at higher gain, systematic noise was issue; due to PHASIC in socket on test fixture.
- Completed new test fixture without socket. Residual noise was eliminated, allowing full performance testing to proceed.
- Initial test results indicate noise and dynamic range goals achieved and new 16 bit SR’s are functional.
- Linearity and threshold testing in progress (should be done by PDR).
- PHASIC Manual has been updated to account for SPP mods.

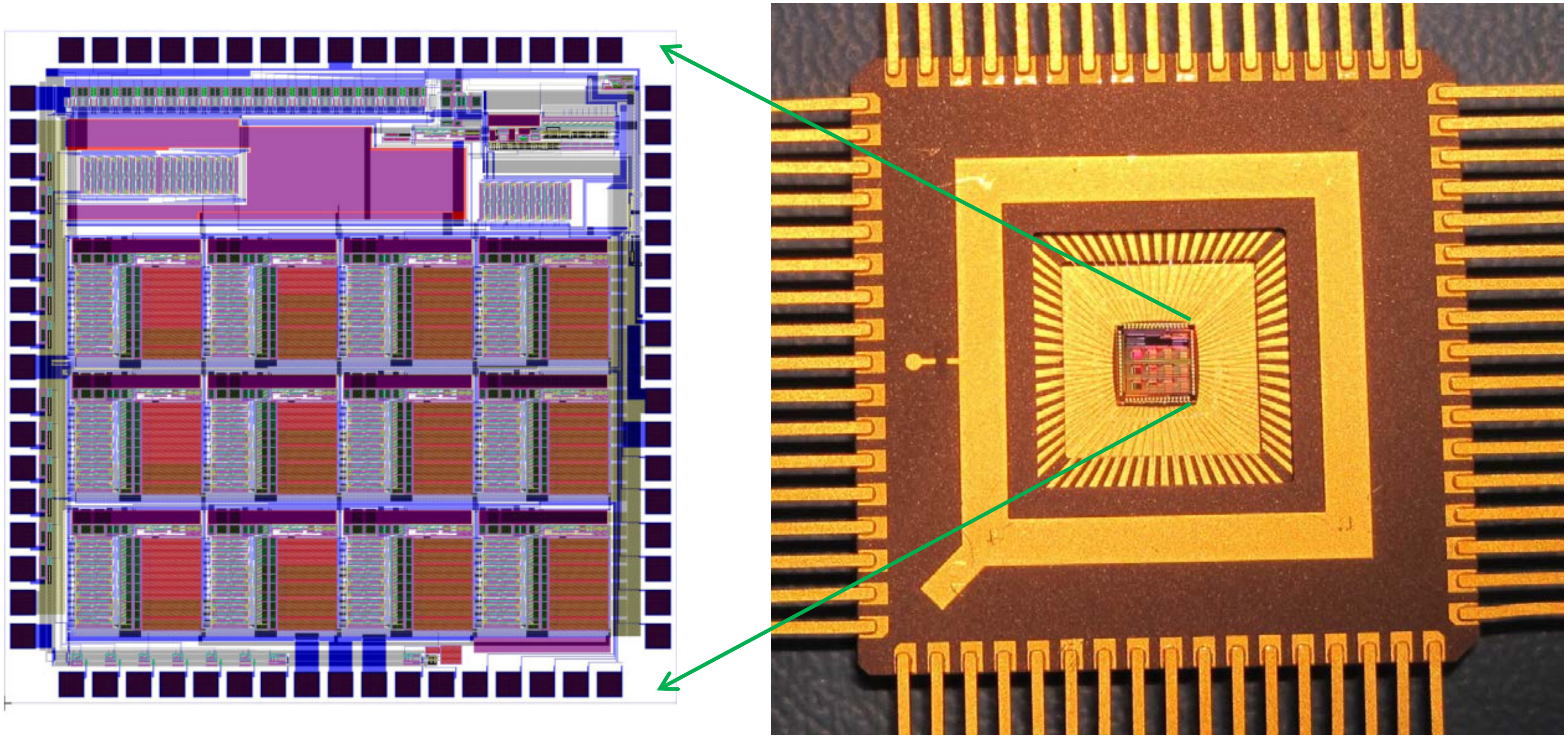
What is a MISC?

- MISC stands for “Minimal Instruction Set Processor”
- Public domain design concept by Charles Moore, inventor of FORTH
- Our implementation defined in 2002 for STEREO, with Dr. C.H. Ting
- 24 bit word width; Four 6-bit instructions per word
- All instructions execute in single clock cycle
- Dedicated I/O bus and instructions
- 11 prioritized interrupts
- Both MISC design and FORTH operating system stable since 2002.
- Compact design fits nicely in RTAX250.
- Data and Return stacks implemented using “block ram” in RTAX250, with EDAC becomes SEU tolerant.
- RTAX250 implementation (flown on NuSTAR) runs @ 15 MHz
- MISC uses 36% of RTAX250 “R cells” (flip-flops) and 63% of “C cells” (logic gates), leaving 1050 R cells and 900 C cells for application specific logic.
- Estimated app specific logic for telescope board: 500 Rcell, 300 Ccell based on similar STEREO design, i.e. < 50% of available resources

HK Chip

- Housekeeping Chip is a new ASIC design for use in EPI-HI.
- Includes most auxiliary functions needed for a small instrument in a 68 pin hermetic ceramic package:
- Delta sigma modulator, for making DC voltage (0-5V) measurements to monitor power supply voltages, currents, and instrument temperatures.
- 35 input analog multiplexor
- 12 10-bit DACs with option of rail to rail buffered output
- 12 digital outputs designed to drive opto-isolated power switches for heater control
- DACs may be ganged for greater voltage setting resolution
- DAC outputs may be internally routed to modulator for precision measurement => low precision DACs can be used to generate high precision voltages and improved in-flight PHASIC calibration.

HK Chip Packaging



- HK Chip packaged in hermetic 68 pin ceramic package
- HK Chip to be qualified and screened to level Q, with PIND test included.

HK Chip Status

- HK Chip was laid out using Aeroflex design rules.
- Fabrication of EM parts was done with ON Semi C5N process through MOSIS.
- Test results: DAC linearity limited to 8 bits; Delta sigma modulator can provide up to 18 bit performance. Buffer amps, digital outputs and power on reset circuit all perform properly.
- Design judged adequate for flight re-spin with Aeroflex radiation hardening.
- Flight re-spin will occur simultaneously with PHASIC flight fab on same wafers.