

Solar Probe Plus

A NASA Mission to Touch the Sun



Integrated Science Investigation of the Sun Energetic Particles

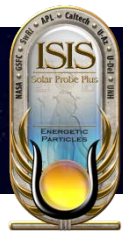
Preliminary Design Review

05 – 06 NOV 2013

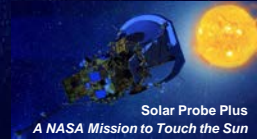
EPI-Lo Electronics

Reid Gurnee

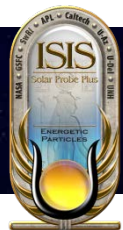




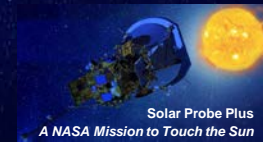
Outline



- Electronics Overview
- Block Diagrams
- Driving Requirements
- Event Board
 - Functionality, Interfaces, prototyping, FPGA, layout
- Anode Board
 - Functionality, Interfaces, prototyping, layout
- Energy Board
 - Functionality, Interfaces, prototyping, layout
- Packaging and thermal considerations
- Radiation analysis
- Plans for testing
- Preliminary parts list and special screening considerations
- Status Summary
- Plan Forward
- Summary and follow-up from peer reviews

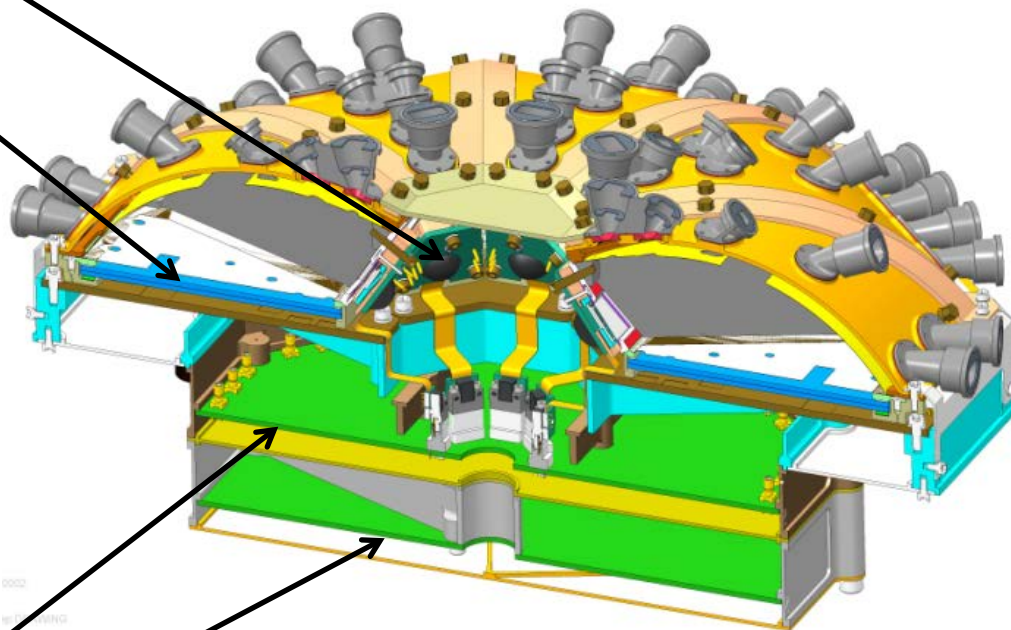
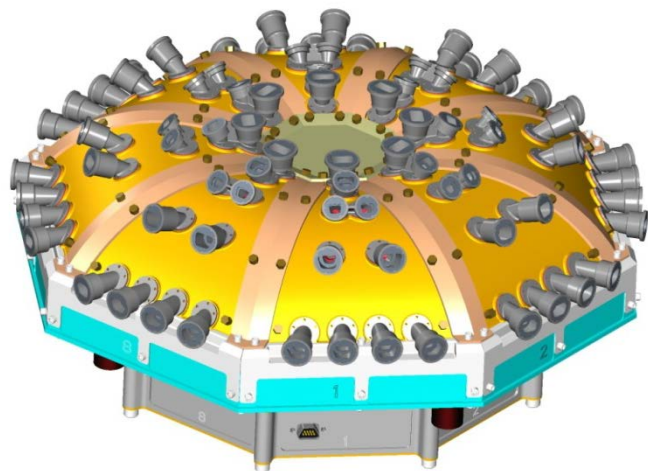


EPI-Lo – Electronics Overview



Energy Boards (x8)

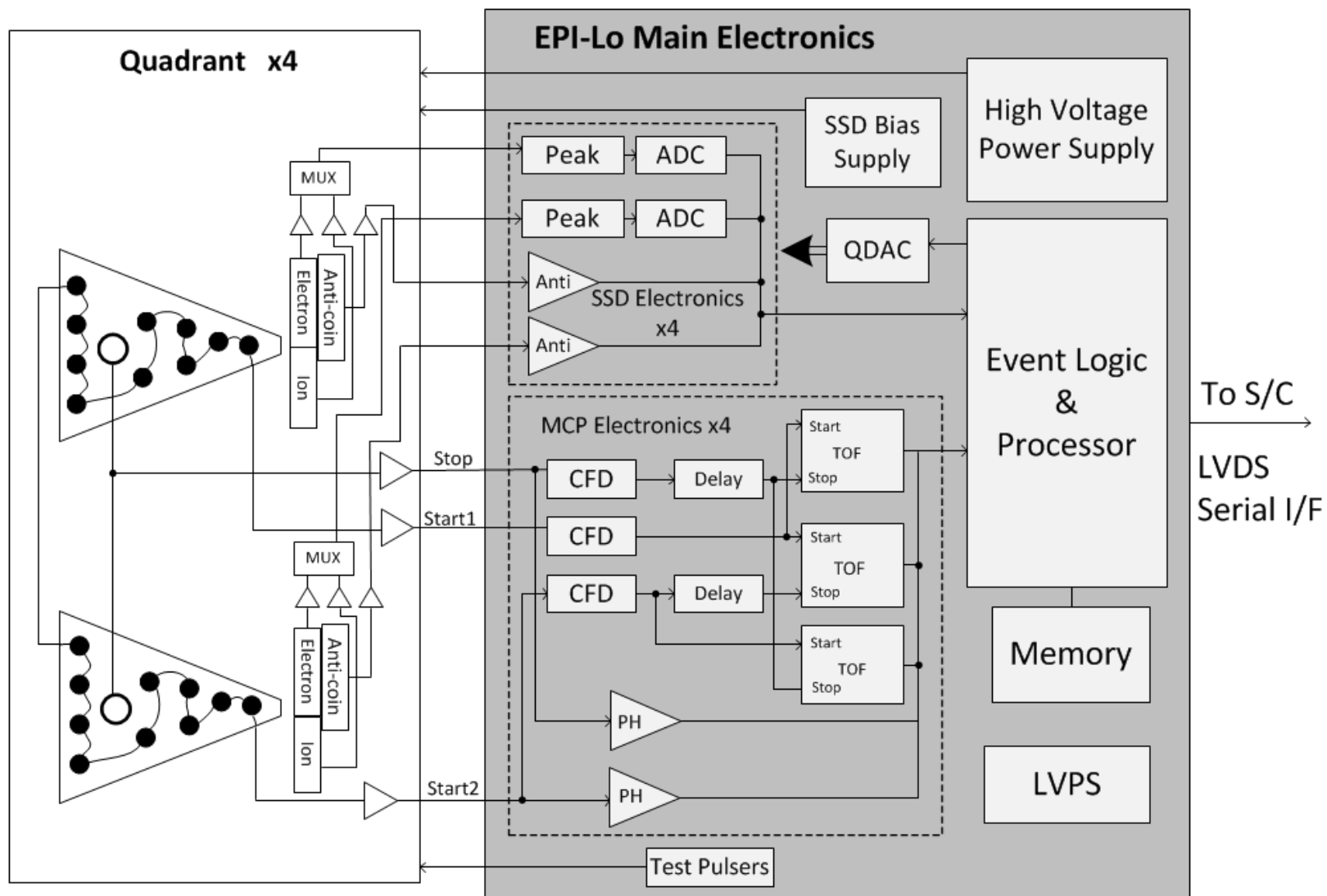
Anode Boards (x4)



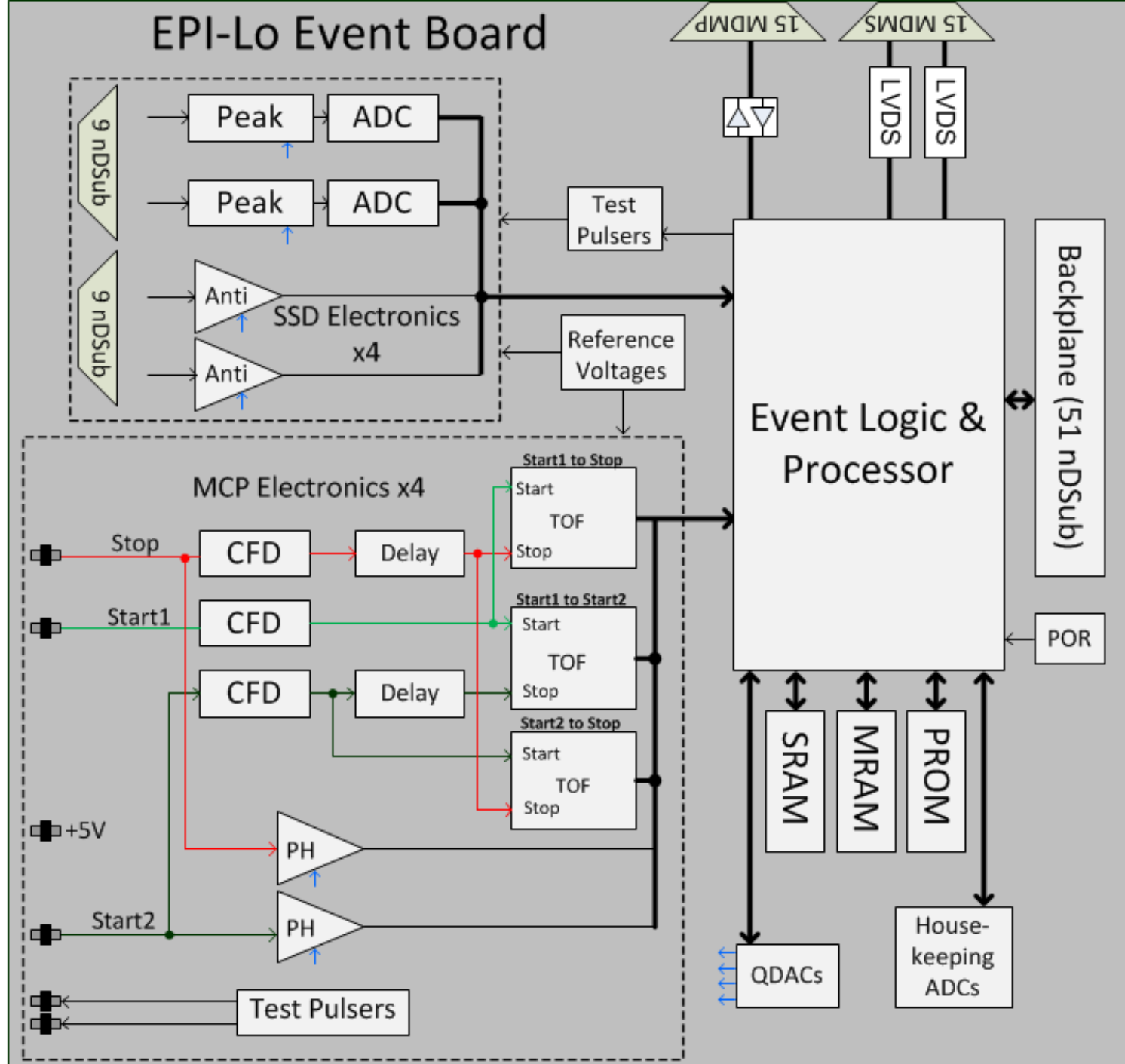
Event Board

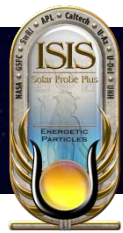
Power Board

EPI-Lo Block Diagram

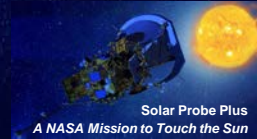


EPI-Lo Event Board

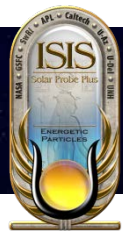




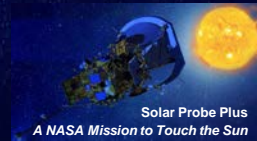
Electronics Driving Requirements



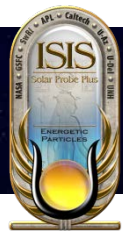
- Analog Performance
 - Timing resolution $< 400\text{pS}$ FWHM
 - Energy resolution $< 15\text{KeV}$ (typically sensor / pre-amp dominated)
- MCP timing system dynamic range of 500k to 25M electrons
- Energy system dynamic range of 30keV to 15MeV
 - Higher energies ($>1\text{MeV}$) use pulse width mode



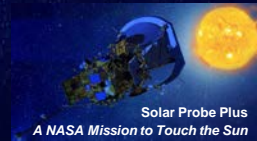
Event Board Functionality



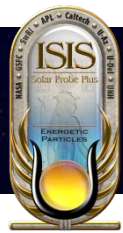
- Instrument processor
 - Embedded processor in RTAX2000
 - Execute Flight Code, Accumulating and Formatting Telemetry, Commanding, and Alarm Detection and Action
 - Spacecraft communication
 - Core code in PROM, classification tables and application code in MRAM
 - Accumulate data into classification tables
- Event Processing
 - Communicate and handle timing with ADCs, TOFs
 - Pre-process and accumulate event data
 - Accumulate Rates
- HVPS control
 - Control four opto-coupler generated HVPS outputs
 - Provide high speed safing of HVPS in response to over current



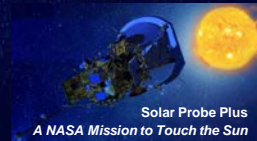
Event Board Functionality



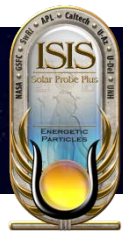
- Time-of-flight based on APL TOD-D and CFD-D ASICs
 - New ASICs developed for future programs
 - Improved size and performance from previous ASICs
 - 12 CFDs and 4 TDCs for timing system
- Solid State Detector Energy Measurements
 - 8 Peak detect and A/D converters for energy system
 - Peak detect chips are APL ASICs flown on previous missions (PEPSSI, Jedi, RBSPICE)
- MCP pulse height comparators
 - Two comparators for each MCP monitor MCP gain
- Pulsers
 - Independent pulsers for start and stop signals on each anode board
 - Two pulsers for Energy system
 - All pulsers have programmable amplitude



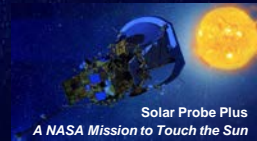
Event Board Interfaces



- Solid State Detector Interface
 - 8, 9-pin ndsub connectors to energy boards
 - ~10 mV to over 1 V unipolar-shaped pulses
 - Control, pulser, and power lines
- Anode Board Interface
 - 12 Time-of-Flight Coax connectors to anode
 - ~10 mV to over 1 V fast-shaped pulses
 - 12 power and pulser Coax connectors
- Test Port Connector
 - 1 Test Input (to aid in end-to-end timing tests)
 - 5 Test-point outputs
- Spacecraft data connector
 - Redundant LVDS interface



Energy System Updates

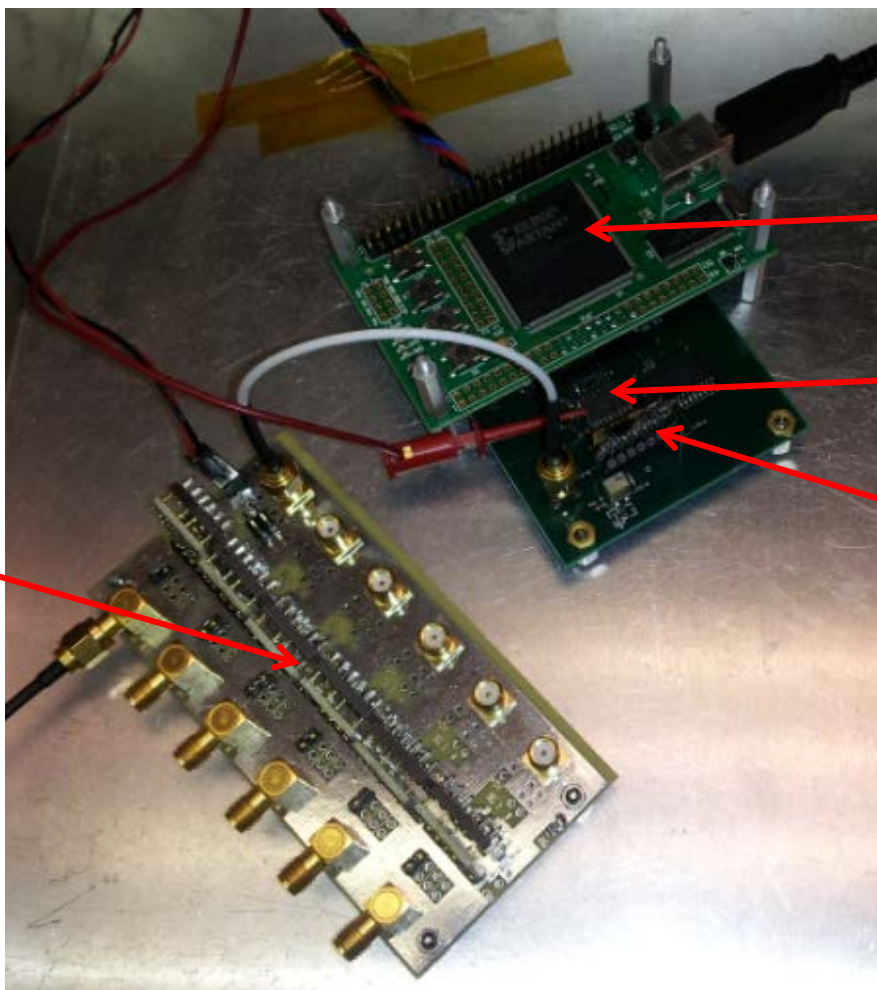


- Energy system re-designed from previous instruments
 - 8 ADC121s read out the 8 peak detect chips
 - Prior designs used MUX and one fast ADC
 - New design allows de-coupling of quadrants – each quadrant had completely independent readout electronics and can be operated as an individual instrument
 - Event logic will be identical for each quadrant and then the data will be combined
 - New approach significantly simplifies event logic design and increases data processing rates

Energy System Prototype

- Test interface of peak – detect chip to ADC

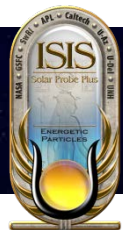
SSD pre-amplifiers



Digital
readout

ADC121 (EM)

Peak Detect
SIP

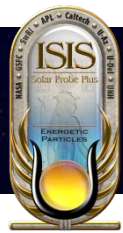


Energy System Prototype Performance

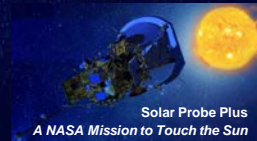


- Energy resolution of test setup far exceeds requirement
- No glitches observed on signal when ADC transitions into track mode after the peak detect SIP captures an event

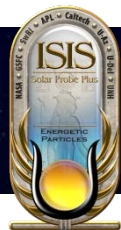
DB atten	KeV		Codes	Std Dev	FWHM	FWHM (KeV)
0	1820.00		3945	5.15	12.1025	9.92405
-6	912.161		3000	4.56	10.716	8.78712
-7	812.964		2910	3.25	7.6375	6.26275
-8	724.555		2830	3.16	7.426	6.08932
-9	645.760		2761	3.02	7.097	5.81954
-10	575.535		2696	2.9	6.815	5.5883
-15	323.647		2478	2.55	5.9925	4.91385
-20	182.000		2339	2.41	5.6635	4.64407
-25	102.346		2255	2.34	5.499	4.50918
-30	57.553		2203	2.23	5.2405	4.29721
-35	32.365		2174	2.15	5.0525	4.14305
-40	18.200		2157	2.36	5.546	4.54772



FPGA



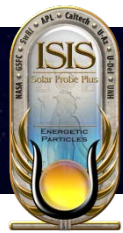
- FPGA contains all event logic and event processing
 - SCIP: 16-bit 10 MIPS processor (reused custom embedded processor based on Harris RTX2010 and APL's FRISC)
 - Processor memory interface to PROM, MRAM, SRAM
 - Support I/O
 - Provide voltage supply clocks, read safing status, set thresholds, monitor housekeeping, etc.
 - LVDS spacecraft communication interface
 - Processor test port interface
 - Event Logic
 - Count sensor basic rates and diagnostic rates
 - Provide pulser stimulus
 - Collect and process TOF values to generate start direction and particle time-of-flight
 - Select appropriate SSD channel and record energy deposited
 - Detect anti-coincidence (electron only) and pulse-height over-threshold (start and stop)
 - Send selected valid events based on commanded event criteria to processor event buffer
 - Event logic test port for ground testing



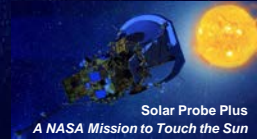
FPGA



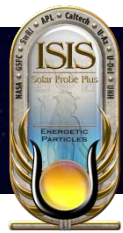
- Actel RTAX2000SL -1 speed CCGA-624 (common buy part)
 - Estimate ~40% resource utilization based on RBSPICE design
 - Internal RAM for event FIFO only
 - No minimize size required and soft memory is fine
 - # user I/O of 418 user I/O total
 - # spares to power board + 6 spares through Schmitt triggers to test connector + # true spares = # spares
 - Note: At the FPGA requirement review, moderate reuse designs are green for at least 17 uncommitted I/O pins
- 1.5V Core Voltage, 3.3V I/O Supply Voltage
 - +/-5% voltage tolerance
 - Supplies can be powered up or powered down in any sequence as long as some app note details are considered
 - I/O are tri-stated during power-up
- Lower standby current part but still significant power contribution at hot temperatures



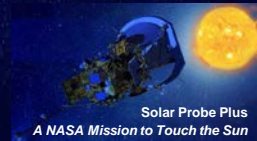
FPGA



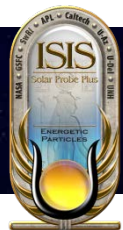
- Part prototyping
 - Reprogrammable Aldec/Actel system for EM
 - Board layout also accommodates commercial socket if needed
 - RTAX2000SL -1 speed CCGA-624 for flight (participating in common buy)
- Design prototyping/reuse
 - SCIP is identical to RBSPICE
 - Similar approach to RBSPICE for many interfaces: S/C communication, power supplies, QDACs, test port, memories, peak detects, pulsers
 - New interfaces prototyped prior to EM: TOF-D rather than TOF-C, new ADC for HK and peak detect
 - Significant previous experience with all design tools: VHDL (with tcl scripts, pdc files etc.), Synplify Pro, Actel Libero, ModelSim
- No expected areas of concern
 - No timing closure challenges expected (most of design at 10MHz, some at 40MHz)
 - Primarily synchronous design techniques with standard clock domain crossing techniques and no gated clocks
 - Straightforward reset filtering and routing network
 - Sufficient clock nets available for clocks and reset



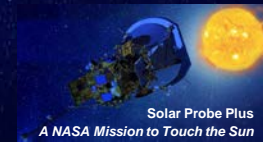
Event Board Layout

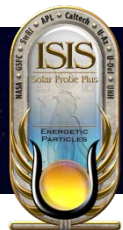


- Sensitive analog is separated from digital
 - FPGA, S/C communication, SRAM, PROM, MRAM, and oscillator on top of board
 - TOF electronics on left and right of board
 - Peak detect and ADC electronics on bottom of board
 - All critical routing isolated by ground planes from digital routing
- **X layers, X ground and power planes**
- Actel located with SRAM directly adjacent
 - Reduce track-length to SRAM to reduce noise
 - Actel on Primary side, to allow the Development Tool access to the program pins



Event Board Layout





Anode Board Description

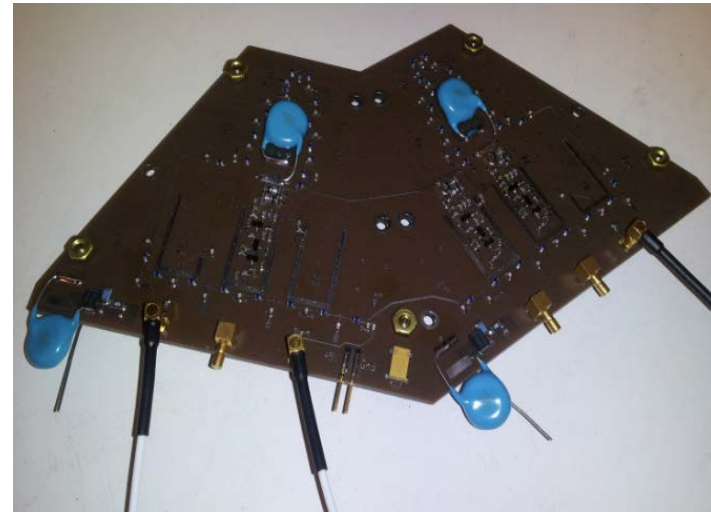
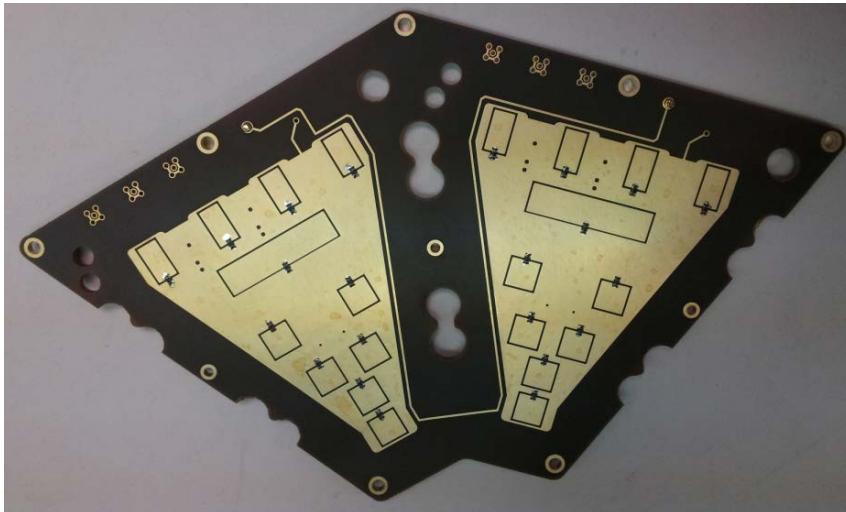


- **Functionality**
 - 3 fast discrete amplifiers
 - Stop anode and each end of the start delay line
 - 50 ohm impedance matched, designed to drive 50 ohms
 - Anode is at 3kV, PCB embedded capacitors isolate HV from LV
 - 1 start pulser and 1 stop pulser
 - Start pulser location in imaginary anode between sensor wedges
- **Interfaces**
 - 6 coax **SSMB** connectors
 - Power, 3 outputs, 2 pulsers

Show output waveform with X #
of input electrons

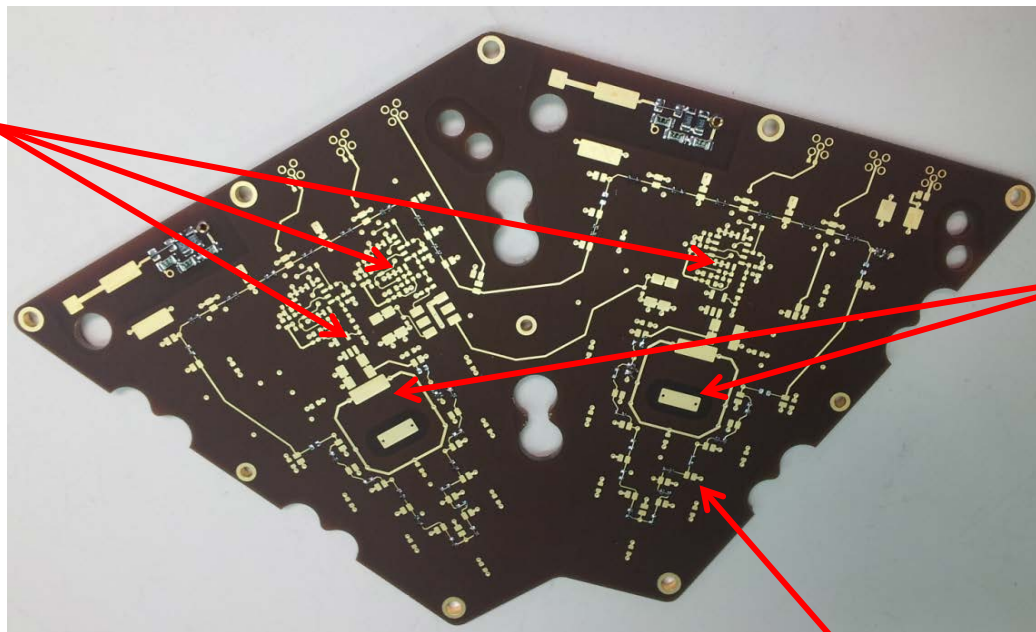
Anode Board Prototyping

- Initial prototype board fabricated, assembled, and tested
 - First implementation of embedded capacitors for HV anode
 - Verified quadrant design
- EM anode board fabricated, assembled, and tested
 - Electrical and mechanical interfaces well defined
 - Position mapping on prototype verified simulations for start pad locations
 - Kapton layer provides dielectric strength of $\sim 20\text{kV}$ for embedded capacitors
 - Passed 10 day, 2x HV standoff test (recommended by Steve Battel)
 - APL packaged transistor array



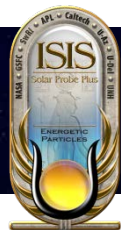
Anode Board Layout

Pre-Amps

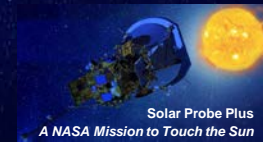


HV Filters

Delay line
elements

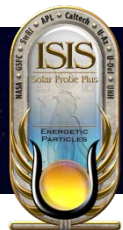


Energy Board

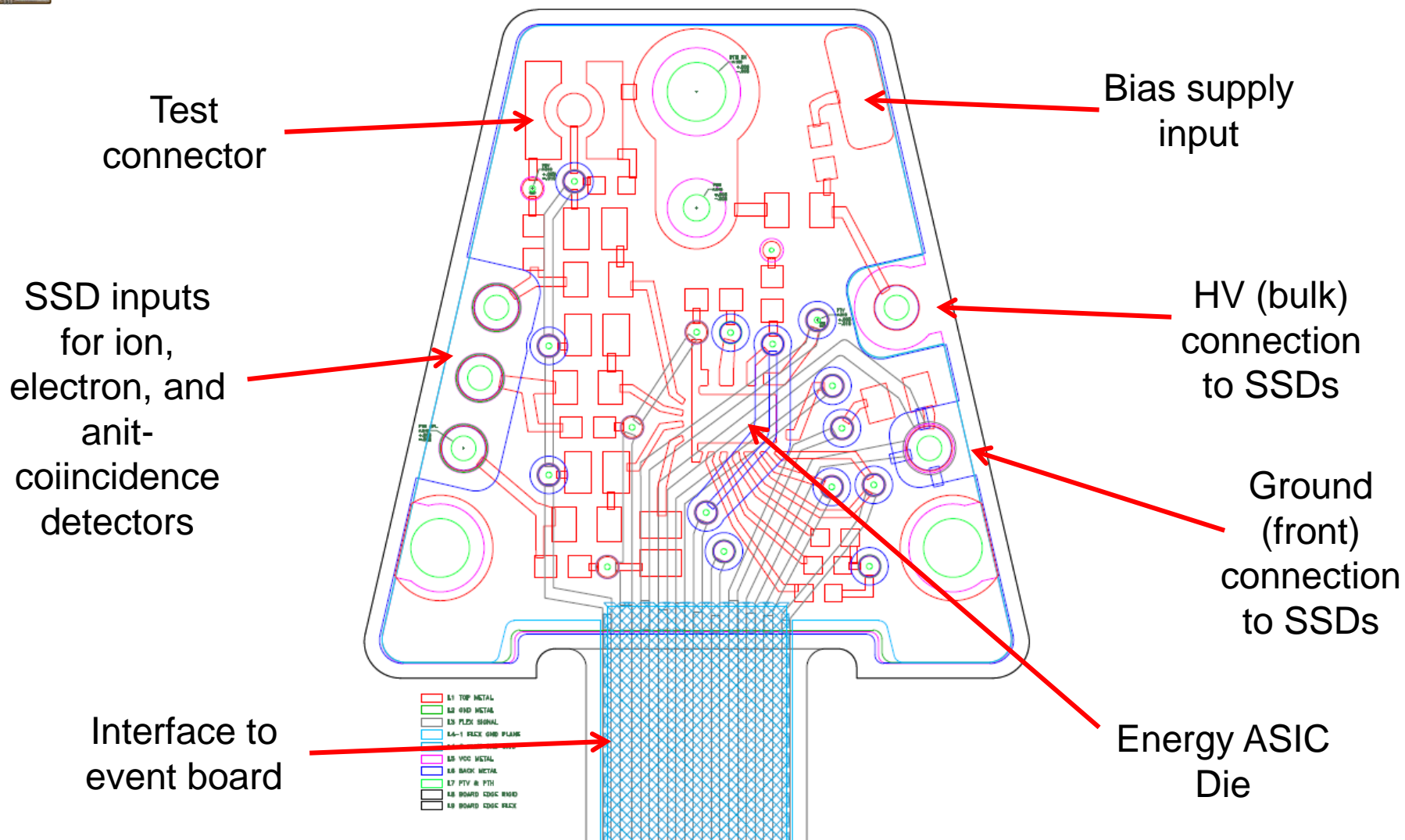


- Functionality
 - SSD Pre-amplifier and shaper
 - Energy ASIC supports 3 pre-amplifiers and MUX
 - Ion channel, electron channel, anti-coincidence channel
 - Select between Ion channel, or electron and anti-coincidence channels
 - Thermistor for temperature measurements
- Interfaces
 - 9pin ndsub connector for power, signals, pulser, and temperature monitor
 - Bias voltage from separate HV wire (<250V)
- EM energy board fabricated and tested

Will have photo of fabricated
board in 3 weeks

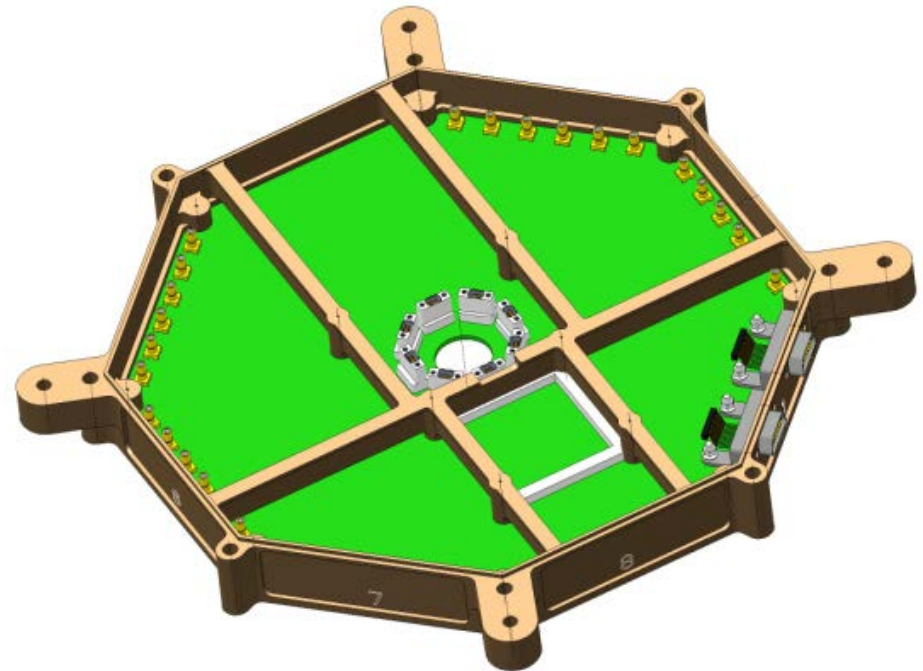


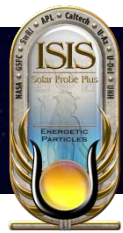
Energy Board Layout



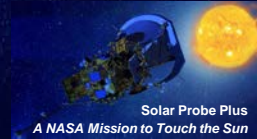
Event Board Packaging

- Packaged in octagon frame “slice”
 - Board is loaded from the bottom and has six center mounting supports and full contact around the perimeter
 - FPGA is supported on four corners
- Large number of thermal vias under the higher power parts
 - Actel, RAM, and MRAM to dissipate power into the board planes and out to the frame.
 - Total board power is ~1 watt. No thermal issues expected.



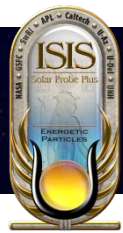


Anode and Energy Board Packaging

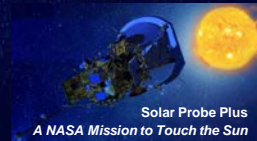


- Anode Board
 - Anode board is mounted to instrument main support structure by X #X mounting hardware
 - Total board power is 90mW, no thermal concerns
- Energy board is mounted directly behind SSD
 - Total board power is 25mW, no thermal concerns

Add images from model showing board mounting

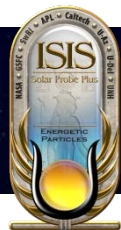


Radiation Analysis



- FASTRad analysis performed on instrument in S/C model to predict doses seen at electronics
- RESULTS:

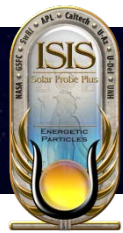
Working on updated fast-rad
analysis



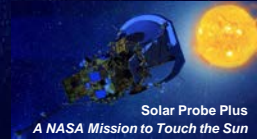
Plans for testing



- Follows APL Manufacturing Flow, these are significant highlights
 - Populate Passive Components
 - Execute Test Procedure to Verify Passive Components
 - Populate First-level Active Components
 - Voltage References, Power-on Reset, Oscillator, applicable Tailor Flags
 - Execute Test Procedure to Tailor and Verify First-level Active Components
 - Populate Actives and Install Known Tailors or Tailor Flags
 - Install into Flight Frame
 - Execute Test Procedure to Test and Tailor Entire Board
 - ESS Testing
 - Execute Functional Test Procedure
 - Photograph and Conformal Coat
 - Execute Test Procedure to Calibrate and Characterize Board (over temperature)
 - Release to Next Assembly

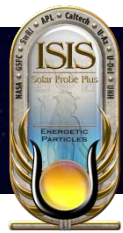


Parts

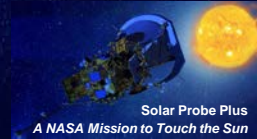


- All parts are rad-hard to 100krad
- No parts concerns

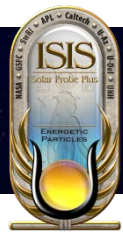
Add table of parts



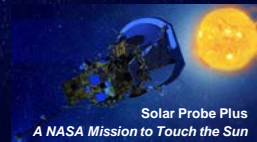
Status Summary



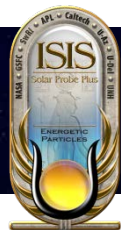
- Event board
 - EM parts placement complete
 - Routing in process
 - EM PCB expected in early December
- Anode Board
 - EM anode board fabricated, assembled and tested
- Energy Board
 - EM Board fabricated, assembled, and tested



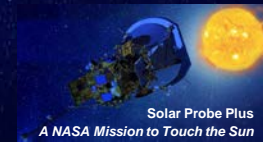
Plan Forward



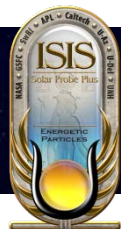
- Anode Board
 - Complete testing on Anode board
 - Fabricate flight anode board
- Energy Board
 - Complete testing on energy board
 - Fabricate flight energy board
- Event Board
 - Fabricate EM board
 - Complete testing on EM board
 - Fabricate flight Event board
- Finalize all documentation and procedures for flight build
- Build, tailor, calibrate, and qualify flight units



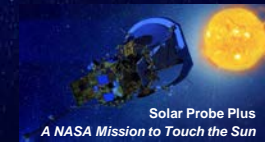
Peer Review Status



- Event Board Peer Review
 - August 21, 2013. Summarized with action items in memo TBD
 - action items were generated
 - 6 action items generated / 6 action items closed
- Anode Board Peer Review
 - TBD
- Energy Board Peer Review
 - August 26, 2013. Summarized with action items in memo TBD
 - action items were generated
 - 4 action items generated
 - TBD action items are closed
- Parts Stress Analysis
 - No issues expected
- WCA
 - No issues expected



Outline



- Driving requirements
- Block Diagram
- Electronics Design Overview
 - Anode Board
 - Energy Board
 - Event Board
 - Power Board
- Detailed description of the measurement electronics and signal processing flow
- Detailed description of the control electronics and its associated support circuitry
- Interfaces to the spacecraft
- Packaging and thermal considerations
- Plans for testing
- ASICs
- Maturity of the design (BB testing, design, analysis completed)
- Preliminary parts list and special screening considerations
- Summary and follow-up from peer reviews

Original Outline