Solar Probe Plus

A NASA Mission to Touch the Sun

Integrated Science Investigation of the Sun
Energetic Particles

Preliminary Design Review
05 – 06 NOV 2013

EMI / EMC

Reid Gurnee

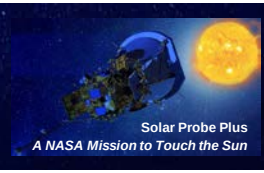
EMC Design Considerations

- Power supplies crystal controlled to a frequency window centered at n*50 kHz with n>=3 and 500 ppm wide over all operating conditions and time.
  - The LVPS is synchronized to 200kHz provided by the digital boards.
  - EPI-Hi has 60MHz oscillator and EPI-Lo has 40MHz oscillator. Both evenly divide to 200kHz. (crystal specifications?)
- Transformers and big inductors are placed as far from Box walls as possible.
  - Show this / mention it in power supply slides
- Stable currents to minimize changes in Magnetic Emissions
- Control all current paths inside your box to minimize loop area. Cannot use a solid return plane if a trace is the source. Any circuit over 100 milliamps AC or 1 amp DC will be analyzed
- All Cables outside the metal box must be twisted shielded with 360deg shields terminated to the Box with less than 20 mOhms.
  - EPI-Lo has no external cables. EPI-Hi ???

EMC Design Considerations

- EMI Backshells not required by EME but shield must cover connector fully
  - I thought we had EMI backshells on all S/C connections???
- Connector shell to Box resistance before mated < 5 mOhms
- Any cable outside the spacecraft body attached to a device must have either 13 mils shielding or DDD first circuit protection
  - EPI-Lo has no external cables. EPI-Hi ??? Are S/C cables going to be shielded, or do we depend on LVDS chips to make this ok?
- All use of Magnetic Materials (Nickel, 400 Series CRSS, etc) must be identified and approved by the project. High Phosphor Nickel coating is allowed because it is not magnetic.
  - EPI-Lo has Nickel grids. Working with project to develop magnetic mitigation plan. EPI-Hi?

EMC Grounding



- Primary power supplies isolated by >1 MΩ
- Secondary power supply returns tied to chassis with <2.5 mΩ in only the Box using the power.
- Grounding Diagrams will show all chassis grounds, primary and secondary power feeds and returns, shields, and signals with returns
- ID all connector pins with first circuits
- Connectors unused in flight shall have a conductive cover with less that 10 mΩ from cover to Box chassis
- "Conductive" Box exterior
  - Exterior will be MLI, and XXX white conductive paint, talk to shawn about other surfaces like kapton tape
- Box design must be at least tongue and groove. EMI gaskets on flat joints is acceptable.
  - Talk to Carl, he said this was not needed. Use copper tape? EPI-Hi???

EMC Testing

Early Testing (Breadboard, Card level, Engineering Model (EM)) can identify a problem when it can still be fixed without major schedule slip.

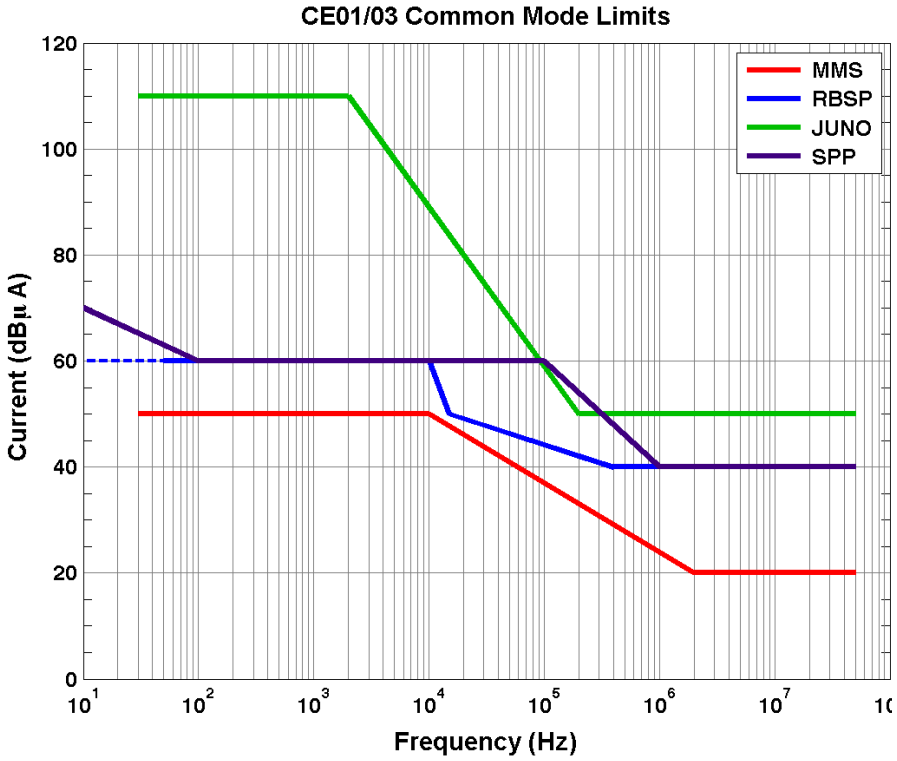
Doing conducted emissions (CE) can find most issues.

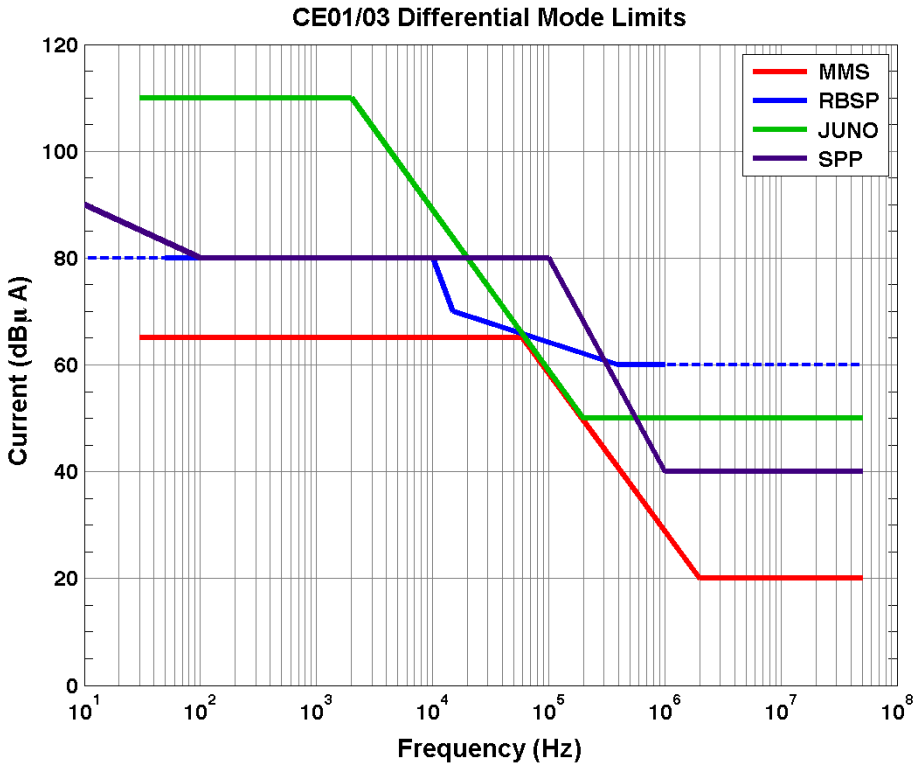
Initial CE test on LVPS will occur in Q1 2013. EPI-Hi and EPI-Lo will test EM units for CE in Q3 2013.

Required Tests:	Bonding & Isolation
Conducted Emissions:	CE-01, CE-02, CE-07
Conducted Susceptibility:	CS-01, CS-02, CS-06
Radiated Emissions:	RE-01, RE-02, Mag Sniff
Radiated Susceptibility:	RS-03, ESD

LVPS CE predicted performance

- Based on heritage supply that meets MMS requirements





Original Outline – do not present

- EMI/EMC requirements and specifications as well as descriptions of design mitigations to meet these requirements
- Include the deep dielectric discharge mitigation approach
- Testing to be performed to verify compliance and when the testing will take place