Solar Probe Plus

A NASA Mission to Touch the Sun

Integrated Science Investigation of the Sun
Energetic Particles

Preliminary Design Review
05 – 06 NOV 2013

EPI-Hi Electronics

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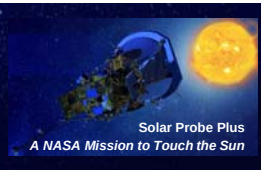
EPI-Hi Electronics SE and Lead (Caltech)

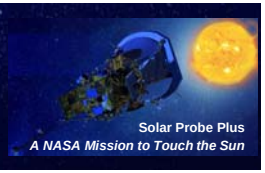
Outline



- Requirements
- Constraints
- Block Diagram
- Instrument - S/C Interfaces
- Pulse Height Analysis System Integrated Circuit
- Minimal Instruction Set Computer
- Housekeeping Chip

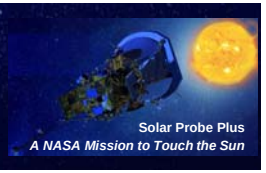
- Design/Assembly/Test Flow
- Board Status
- EEE Parts Program and Status
- Resources
- Harness Diagram
- Summary

Key Requirements



- Support 3 independent charged particle telescopes: LET1, LET2 and HET.
  - For each telescope provide for detection of coincident signals from various Si detector elements to define “events” caused by the incidence of individual nuclei, electrons and neutral particles/photons.
  - For each event, provide pulse height analysis of the signal amplitudes in the various stimulated detector elements. Large dynamic range is needed for measurement of electrons through Zn nuclei.
  - Sort and count the events according to particle type and energy.
  - Integrate the counts for the various particle/energy categories over time periods ranging from seconds to hours.
- Format the count rate data into packets and transmit them to the S/C.
- Include in data packets the raw pulse height data for a sample of events to aid in-flight calibration.
- Monitor instrument health by measurement of detector leakage currents, instrument temperatures, power supply voltages and total instrument current draw, and include this “housekeeping” data in telemetry packets.
- Respond to commands for altering threshold voltages, bias voltages, etc. and performing instrument self-tests and auxiliary functions.
- Control instrument operational heaters.

Constraints and their Implications



Constraints

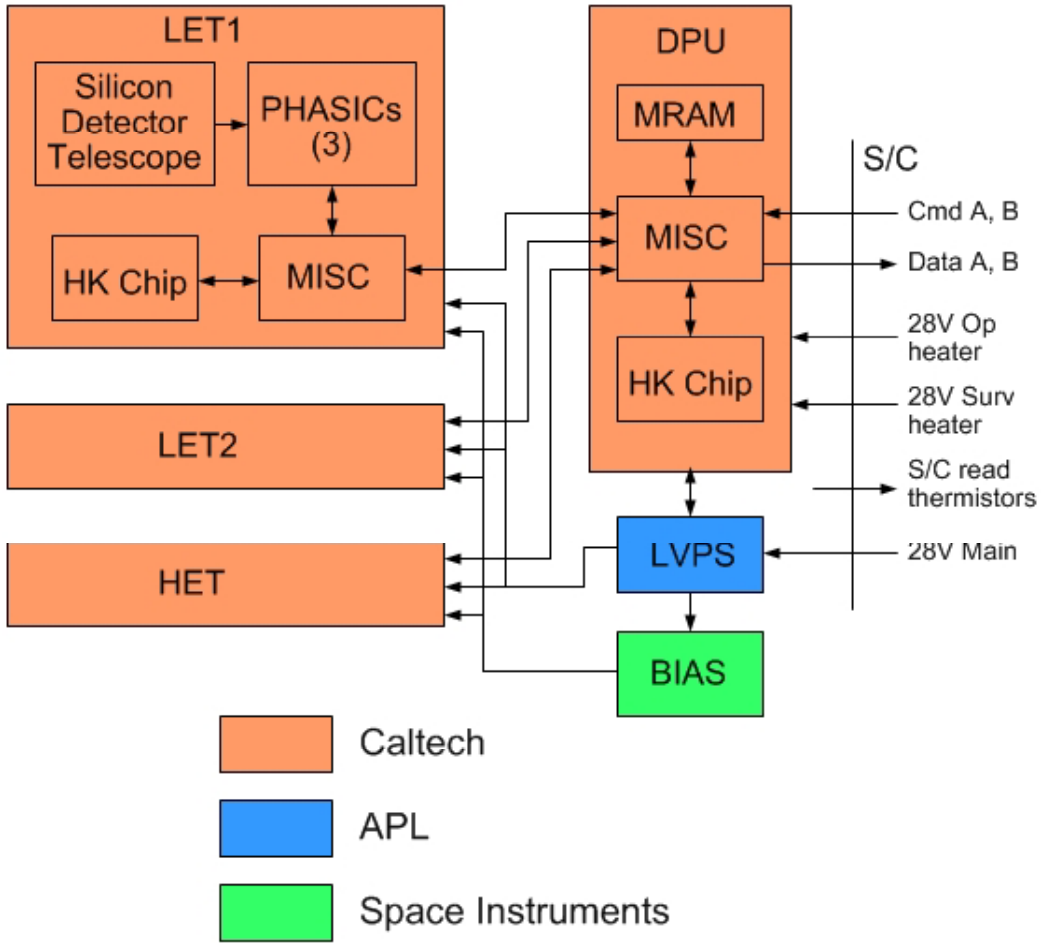
- Both power and mass are very tightly constrained.
- Design should be single string, yet reliable.
- Primary data collection occurs when S/C cannot communicate with Earth.
- Radiation environment is more severe than heritage missions.

Implications

- Reliability through minimization of parts count and use of “natural” redundancy.
- Use of custom rad-hard VLSI: PHASIC and HKCHIP.
- Design should be “bullet-proof” with regard to radiation affects: no latch-up, no processor crash due to SEU, total dose tolerant > 100 krad.
- Design should be capable of autonomous operation during primary data collection period (<0.25 AU from Sun).

EPI-Hi Block Diagram

- 6 boards
- All telescope boards same.
- DPU formats data and provides a single point interface with S/C.
- Low Voltage Power Supply (LVPS) and Bias Supply board are shared.
- Bias Supply board contains a separate supply for each telescope “end”, 5 total.
- Logic and MISCs are implemented in RTAX 250 FPGAs, 4 total.
- Heritage from earlier projects: STEREO and NuSTAR.

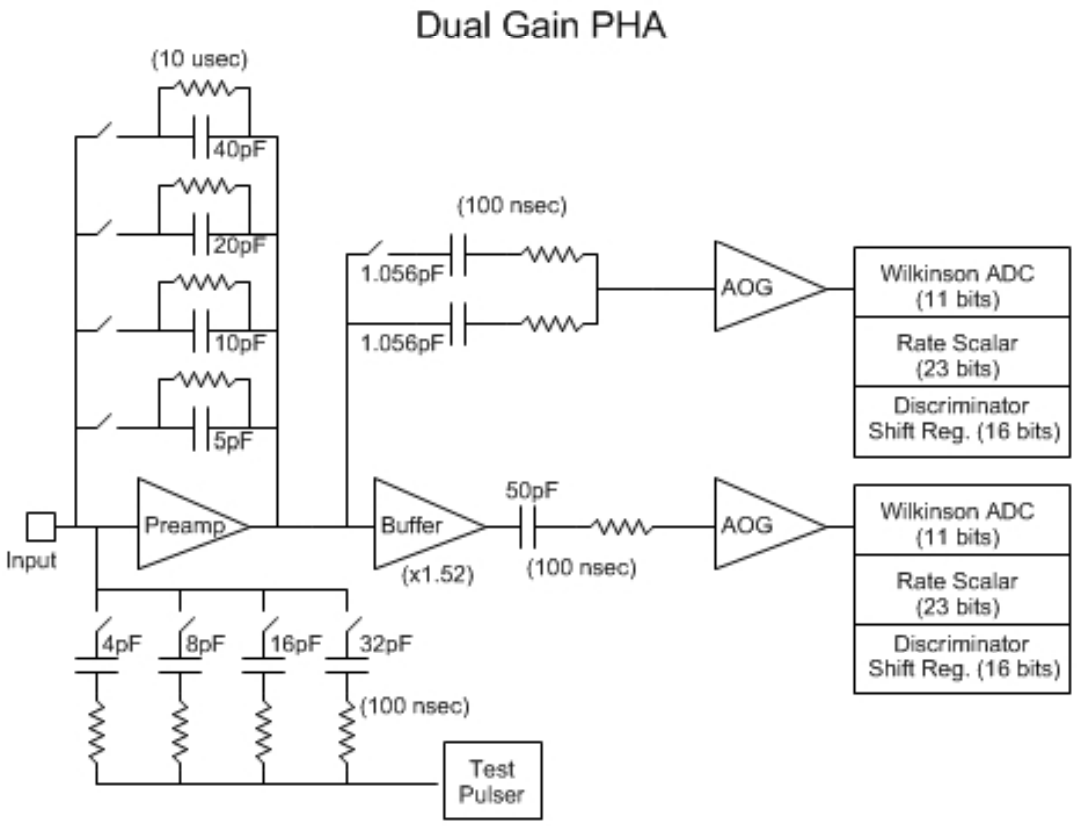


Instrument to S/C Electrical Interfaces

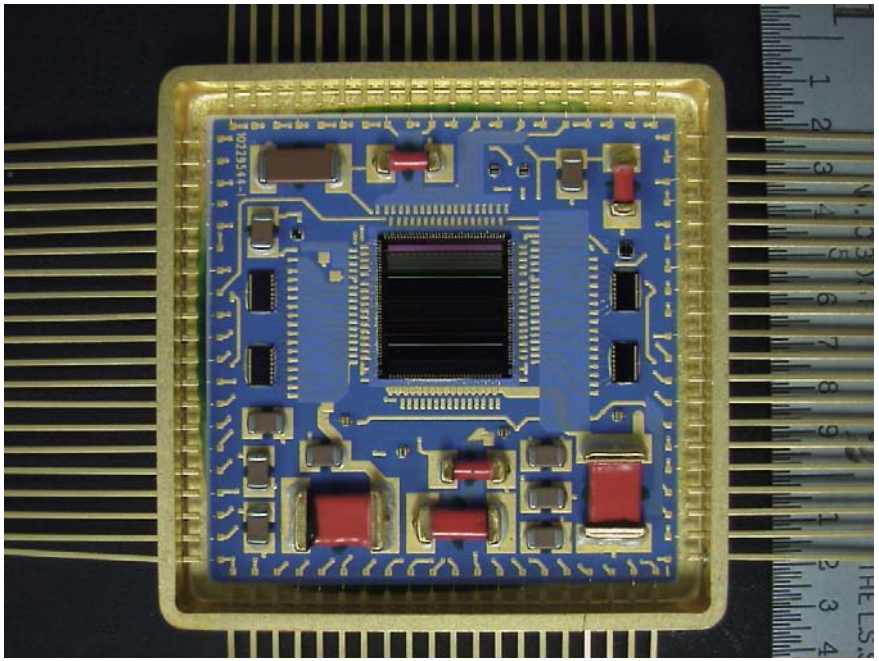
- Interfaces with S/C specified by ICD under APL control.
- Command and data interfaces are 115.2 kbaud LVDS using rad-hard drivers/receivers specified by APL.
- Redundant A and B sides.
- Reset and Timing signals removed from interface by APL for simplicity. Functions included in command signal protocol.
- MISC boot method has been modified to accommodate lack of Reset signal.
- S/C supplies separate 28V power services for survival and operational heaters.
- S/C monitors instrument temp via S/C supplied thermistors.

PHASIC Overview

- PHASIC stands for “Pulse Height Analysis System Integrated Circuit”.
- Originally developed and used in NASA’s STEREO mission.
- Each PHASIC contains 16 complete dual-gain pulse height analysis (PHA) chains.
- STEREO PHASICs still operational in space.
- Mods for SPP include widening dynamic range, and improving total dose tolerance to >100 krad.

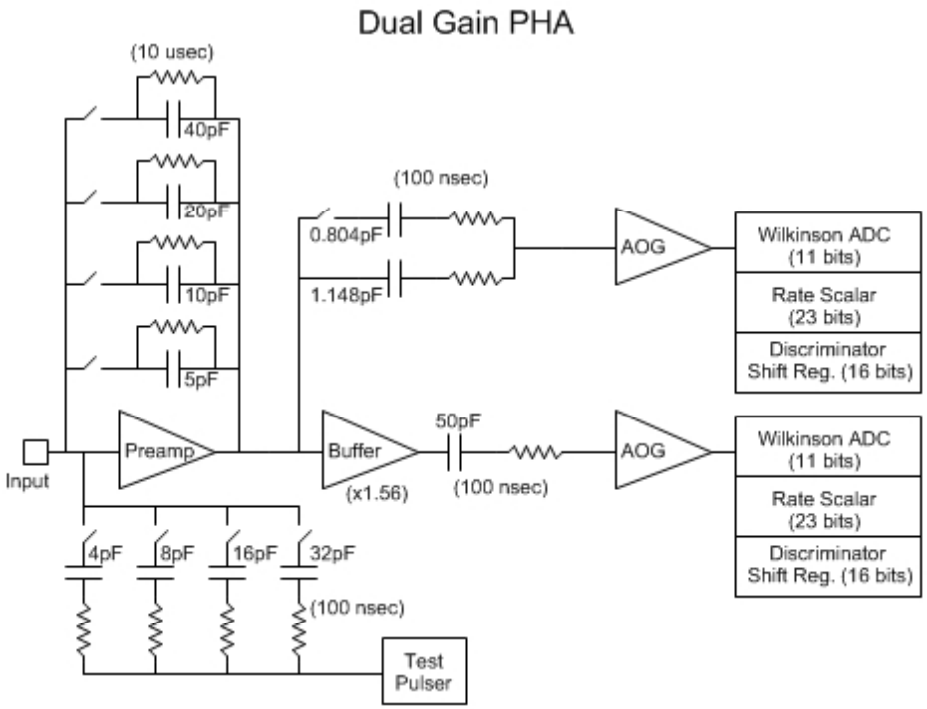


PHASIC Packaging



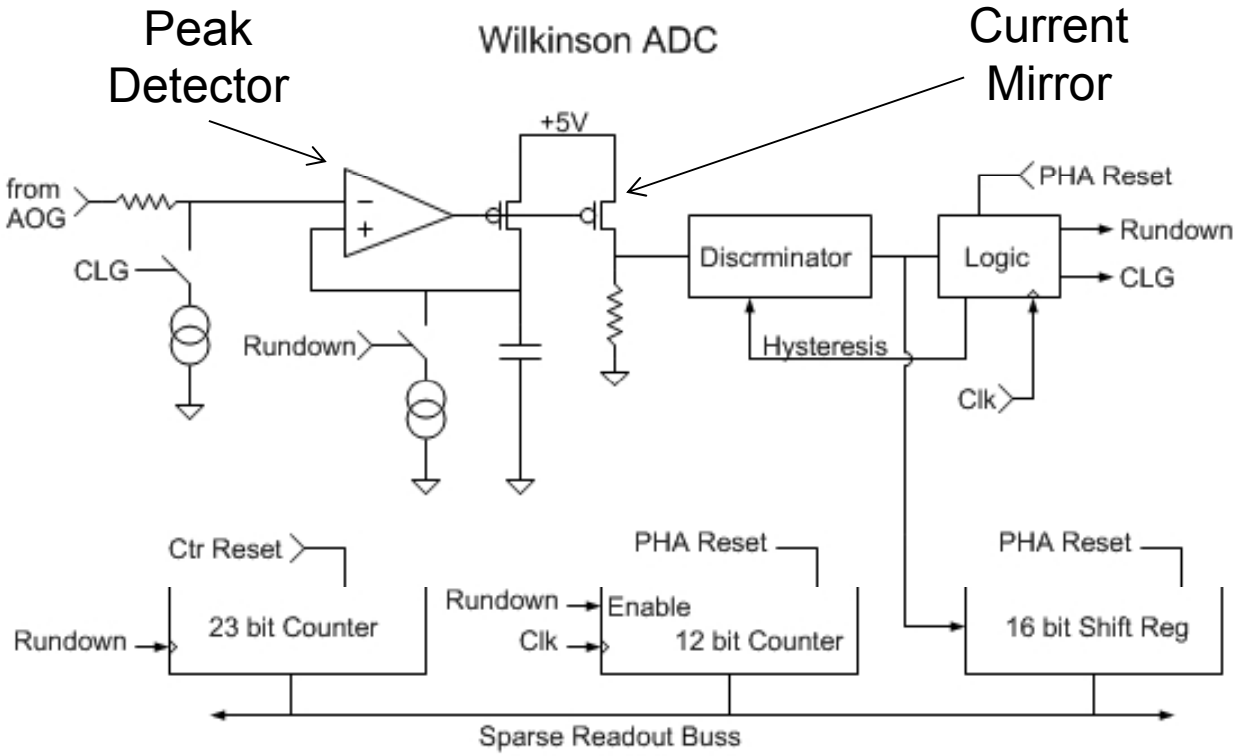
- PHASIC die is installed in an 80-pin hermetic Kovar package along with a few passive components to form a “hybrid” circuit.
- Hybrid substrate design and passives same as for STEREO.
- PHASIC hybrid to be qualified and screened to class H (as on STEREO).
- Passive components include a precision resistor for each PHA chain that sets the rundown current. Allows PHA channel gain to have low <50 ppm/degC temperature coefficient.

PHASIC Mods near Preamp



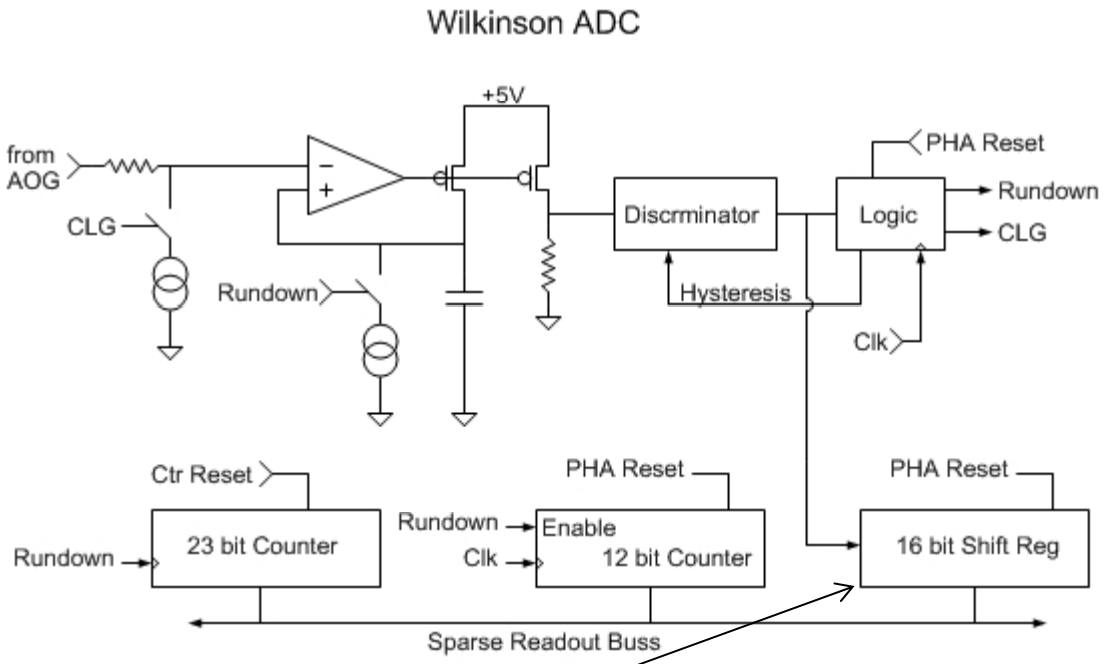
- Preamp output stage changed from “follower” to “open drain” to increase output swing.
- Preamp compensation method changed for lower noise.
- Buffer added in high gain signal chain.
- High/Low gain ratio increased from 20 to 68, with programmable option of 40.
- High/Low gain boundary falls between alphas and carbon for most detectors.

PHASIC Mods near Peak Detector (1/2)



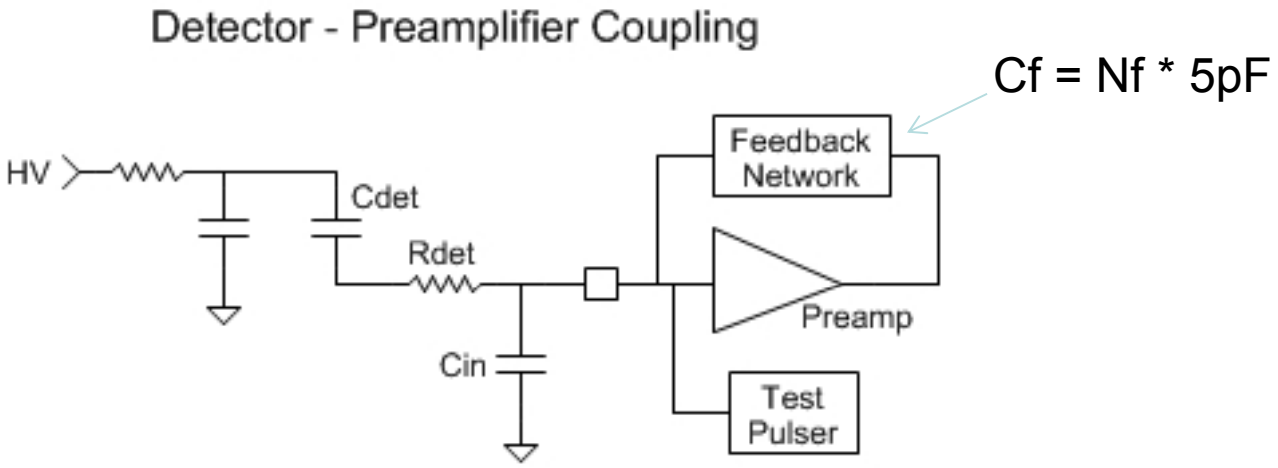
- STEREO Peak detector contained two differential amplifier stages at input. For Solar Probe Plus reduced to one stage but with higher current resulting in lower noise.
- Size of FETs in current mirror at output increased to improve matching and threshold uniformity.

PHASIC Mods near Peak Detector (2/2)



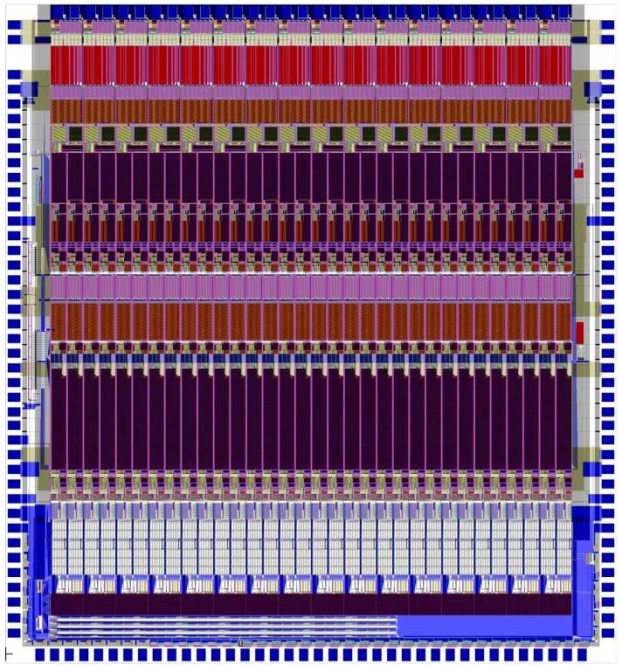
16-bit shift register added to capture time history of discriminator output to aid in cross-talk identification.

Predicted PHASIC Noise/Threshold



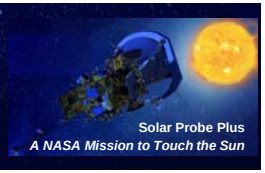
Det	Cdet (pF)	Rdet (ohm)	Cin (pF)	Nf	Threshold (MeV)	Full Scale (MeV)	Zn @ 45 degrees (MeV)	Gain Crossover Freq (MHz)	Phase Margin (deg)
L0	208	0	30	1	0.09	268	83	12.3	98
L1	93	30	40	1	0.05	268	251	13.3	65
L2(H1)	20	10000	60	6	0.12	2802	2660	13.4	60
L3(H2)	40	7500	80	9	0.19	4337	4092	10.8	61
H3	30	15000	80	13	0.28	6155	6203	10.5	56

PHASIC Radiation Tolerance



- Total dose tolerance improved by adding proven Aeroflex processing steps to commercial ON-Semi C5N CMOS process.
- Layout modified to comply with slight Aeroflex design rule differences.
- 12 krad improves to >100 krad.
- Latch-up threshold should still be >80 MeV/(mg-cm^2) due to use of guard rings.

PHASIC Status



- Engineering run though ON-Semi C5N commercial process was completed, yielding EM wafers and dice.
- EM dice installed in STEREO hybrids and tested.
- Systematic noise was issue in STEREO test fixture due to socket. (For SPP some channels need to operate at higher gain than for STEREO.)
- Completed new test fixture without socket. Residual noise was eliminated, allowing full performance testing to proceed.
- Initial test results indicate noise and dynamic range goals achieved and new 16-bit SRs are functional.
- Linearity and threshold testing in progress (should be done by PDR).
- PHASIC Manual has been updated to account for SPP mods.

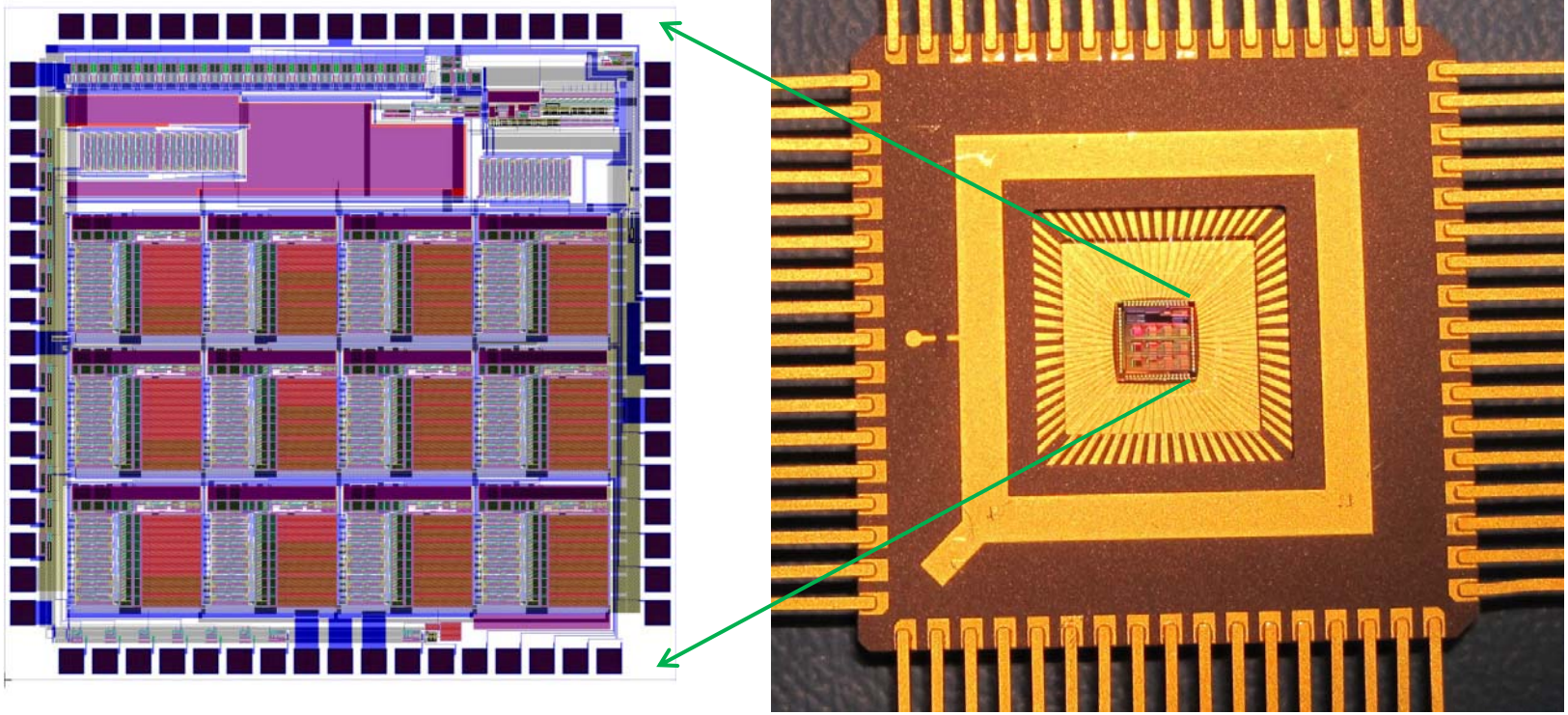
What is a MISC?

- MISC stands for “Minimal Instruction Set Computer”.
- Public domain design concept by Charles Moore, inventor of FORTH.
- Our implementation defined in 2002 for STEREO, with Dr. C.H. Ting.
- 24-bit word width; Four 6-bit instructions per word.
- All instructions execute in single clock cycle.
- Dedicated I/O bus and instructions.
- 11 prioritized interrupts.
- Both MISC design and FORTH operating system stable since 2002.
- Compact design fits nicely in RTAX250.
- Data and Return stacks implemented using “block ram” in RTAX250, with EDAC becomes SEU tolerant.
- RTAX250 implementation (flown on NuSTAR) runs @ 15 MHz.
- MISC uses 36% of RTAX250 “R cells” (flip-flops) and 63% of “C cells” (logic gates), leaving 1050 R cells and 900 C cells for application specific logic.
- Estimated app specific logic for telescope board: 500 Rcell, 300 Ccell based on similar STEREO design, i.e. < 50% of available resources.

HK Chip

- Housekeeping Chip is a new ASIC design for use in EPI-Hi.
- Includes most auxiliary functions needed for a small instrument in a 68-pin hermetic ceramic package.
- Delta sigma modulator, for making DC voltage (0-5V) measurements to monitor power supply voltages, currents, and instrument temperatures.
- 35-input analog multiplexor.
- 12 10-bit DACs with option of rail to rail buffered output.
- 12 digital outputs designed to drive opto-isolated power switches for heater control.
- DACs may be ganged for greater voltage setting resolution.
- DAC outputs may be internally routed to modulator for precision measurement => low precision DACs can be used to generate high precision voltages and improved in-flight PHASIC calibration.

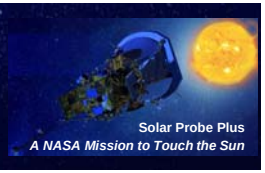
HK Chip Packaging



- HK Chip packaged in hermetic 68-pin ceramic package.
- HK Chip to be qualified and screened to level Q, with PIND test included.

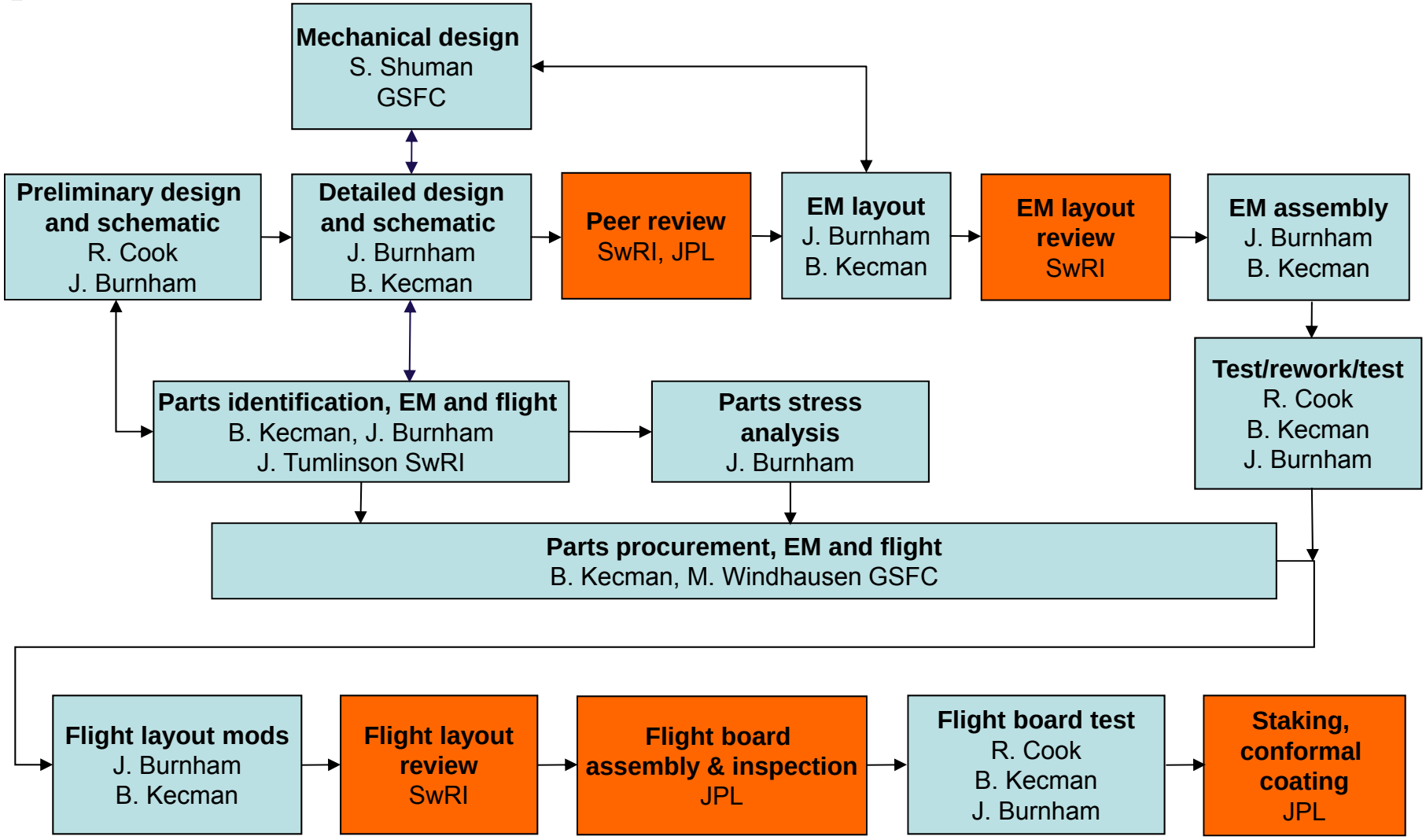
HK Chip Status

- HK Chip was laid out using Aeroflex design rules.
- Fabrication of EM parts was done first with ON-Semi C5N process through MOSIS. The 2nd run was on shared wafers with EM PHASIC fab directly through ON-Semi.
- Test results: DAC linearity limited to 8 bits; Delta sigma modulator can provide up to 18-bit performance. Buffer amps, digital outputs and power on reset circuit all perform properly.
- Design judged adequate for flight re-spin with Aeroflex radiation hardening.
- Flight re-spin will occur simultaneously with PHASIC flight fab on same wafers.

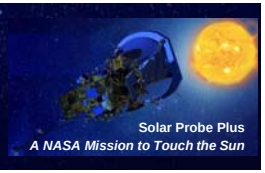


Implementation and Status

Design/Assembly/Test Flow



Board Status

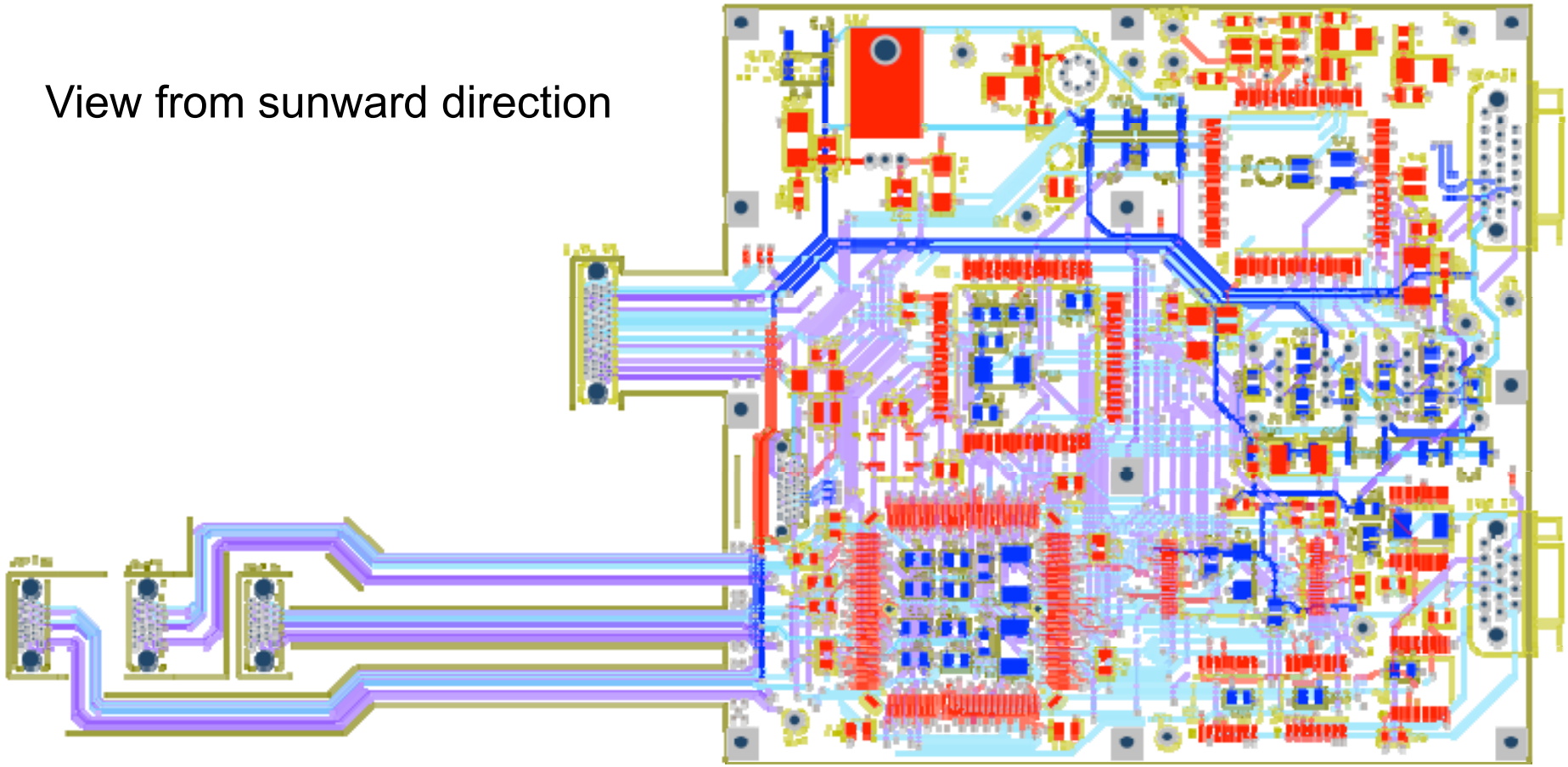


Board	Spec	Schem	Peer review	EM layout	EM fab began	EM parts procured	EM test starts at Caltech
Telescope x3	L4	99%	√	20%	No	60%	Jan-Jun ‘14
DPU	L4	√	√	√	No	80%	2/28/14
LVPS	√	√	√	√	Yes	√	1/27/14
Bias Supply	√	√	√	60%	No	70%	4/7/14

Breadboard	Spec	Schem	Peer	Layout	Fab	Parts	Test
Bias Supply	√	√	N/A	√	√	90%	In progress

DPU Board Layout

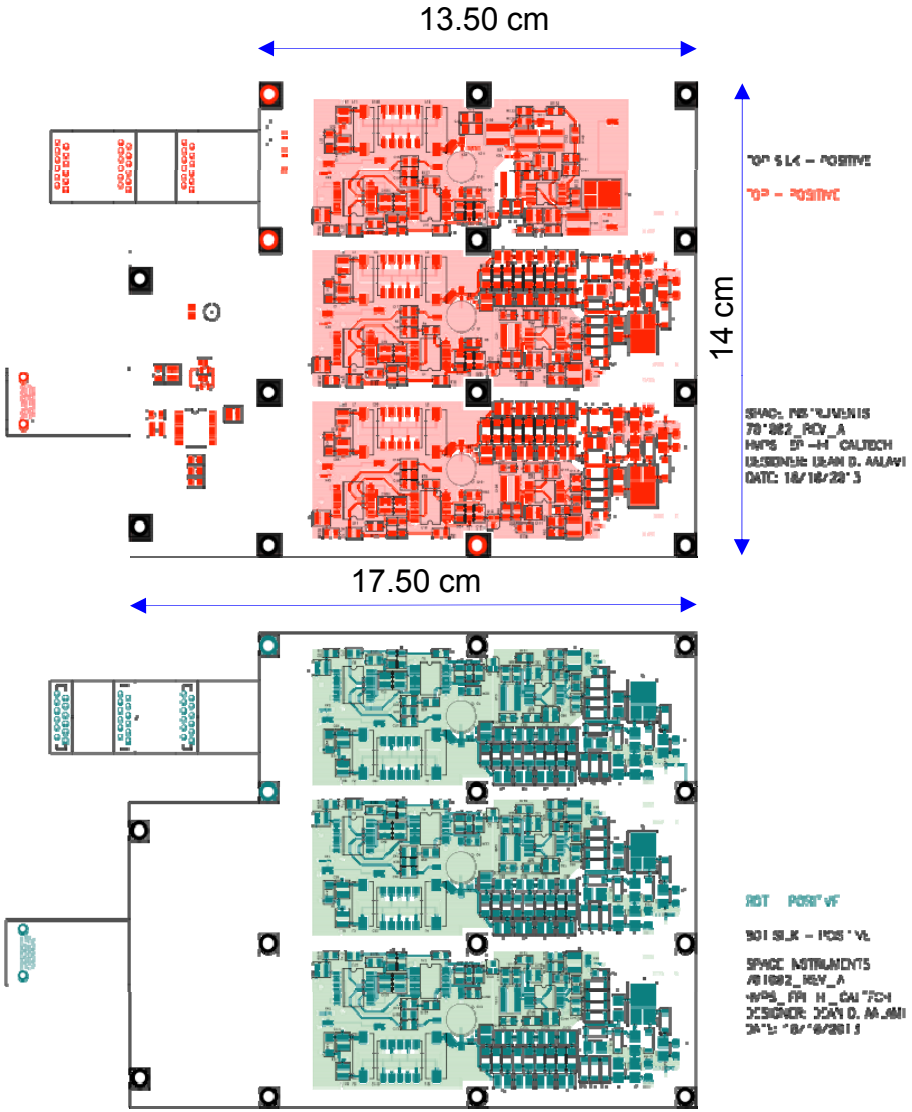
View from sunward direction



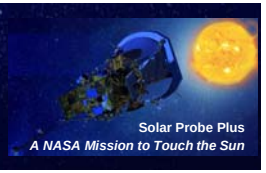
13.50 cm, square

Bias Supply Board Layout

View from sunward direction



EEE Parts Program and Status



- All parts required to meet EEE-INST-002, Level 2
  - PCB approval required for all parts
    - PCB review in process for all parts
- Existing Caltech custom databases used to track inventory and kit history for all parts
- Procurement in process now for prototype/EM parts
- Where possible, flight parts will come from Caltech, GSFC, SwRI and JPL inventory
  - Parts more than 5 years old will have additional testing performed as required by the PCB

Significant Parts

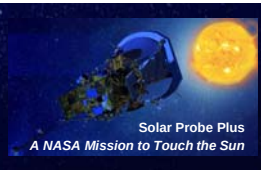
Part Number Part Type	Manufacturer	Heritage	Notes
RTAX250SL-CQ208B FPGA	Microsemi SoC (Actel)	NuSTAR	Existing stock at Caltech
5962R0323601QXC SRAM, 4Mb (128k x 32)	Aeroflex	NuSTAR	Existing stock at Caltech
5962R0422701QXC SRAM, 16Mb (512k x 32)	Aeroflex		
5962R1222201VXC MRAM, 16Mb (2M x 8)	Aeroflex		Common buy with S/C
10229545 PHASIC, Hybrid ASIC	JPL	STEREO	Existing stock at Caltech Modification required
TBD HKchip, ASIC	JPL		Will follow similar process as PHASIC

ASICs: PHASIC and HKchip

- PHASIC: Hybrid ASIC developed for STEREO
  - Using existing stock with modifications
    - New rad-hard wafers will be produced
      - TID and SEL testing planned
    - Heritage die will be removed and replaced
    - Packaging will be performed by JPL Hybrid Lab
    - Assembled part will undergo full screening and qualification performed by JPL and Caltech

- HKchip: New part, monolithic ASIC
  - Will follow the same wafer procurement, packaging and test plan as the PHASIC

Resources - Power



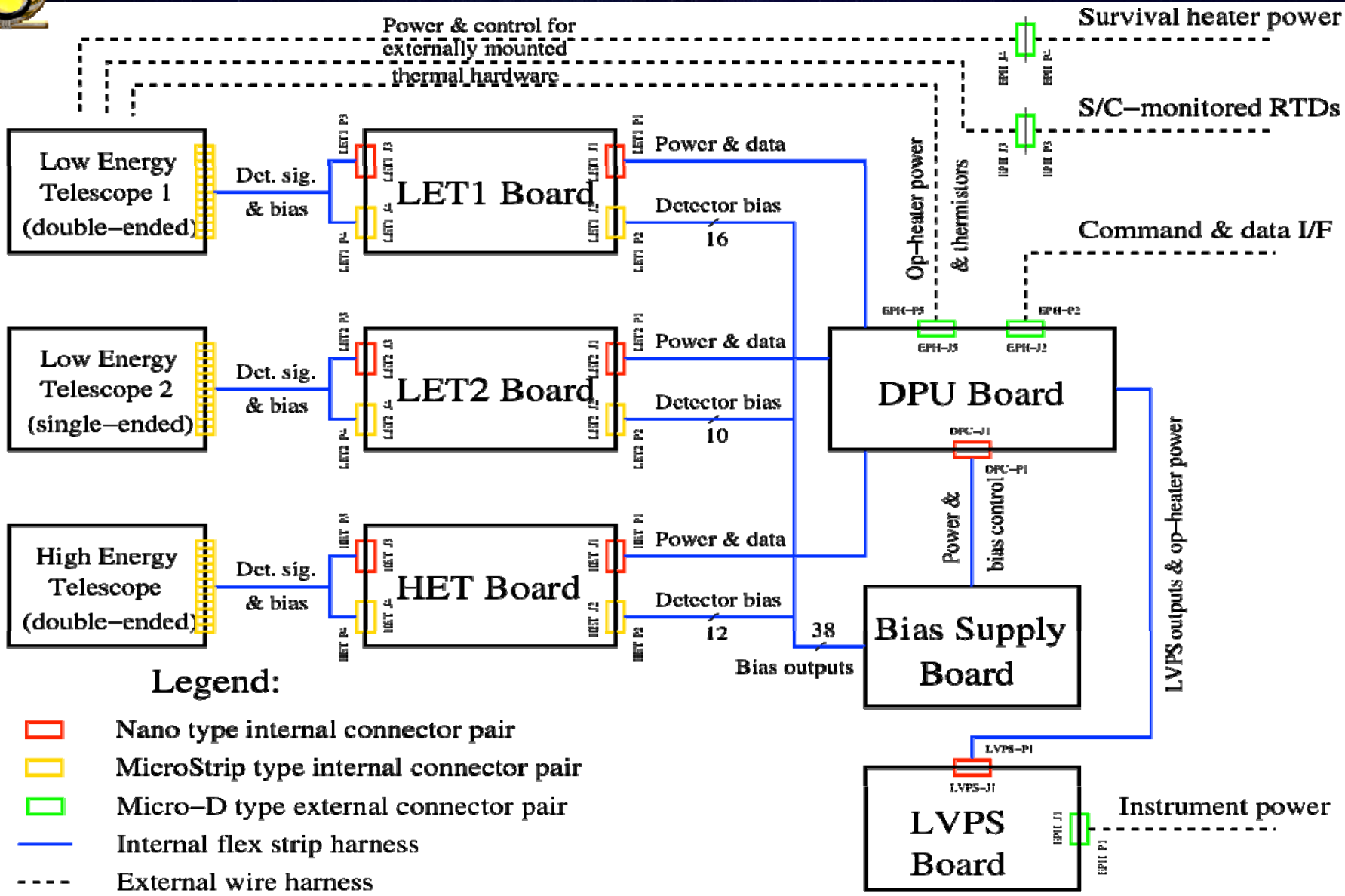
Subsystem	Power [W]
LET1 board	1.06
LET2 board	0.76
HET board	0.95
DPU board	0.62
Bias Supply @ Beginning Of Life	0.12
LVPS @ BOL (70% efficiency)	1.50
Total @ BOL	5.0

End Of Life	
Bias Supply @ End Of Life	0.68
LVPS @ EOL (70% efficiency)	1.74
Total @ EOL	5.8

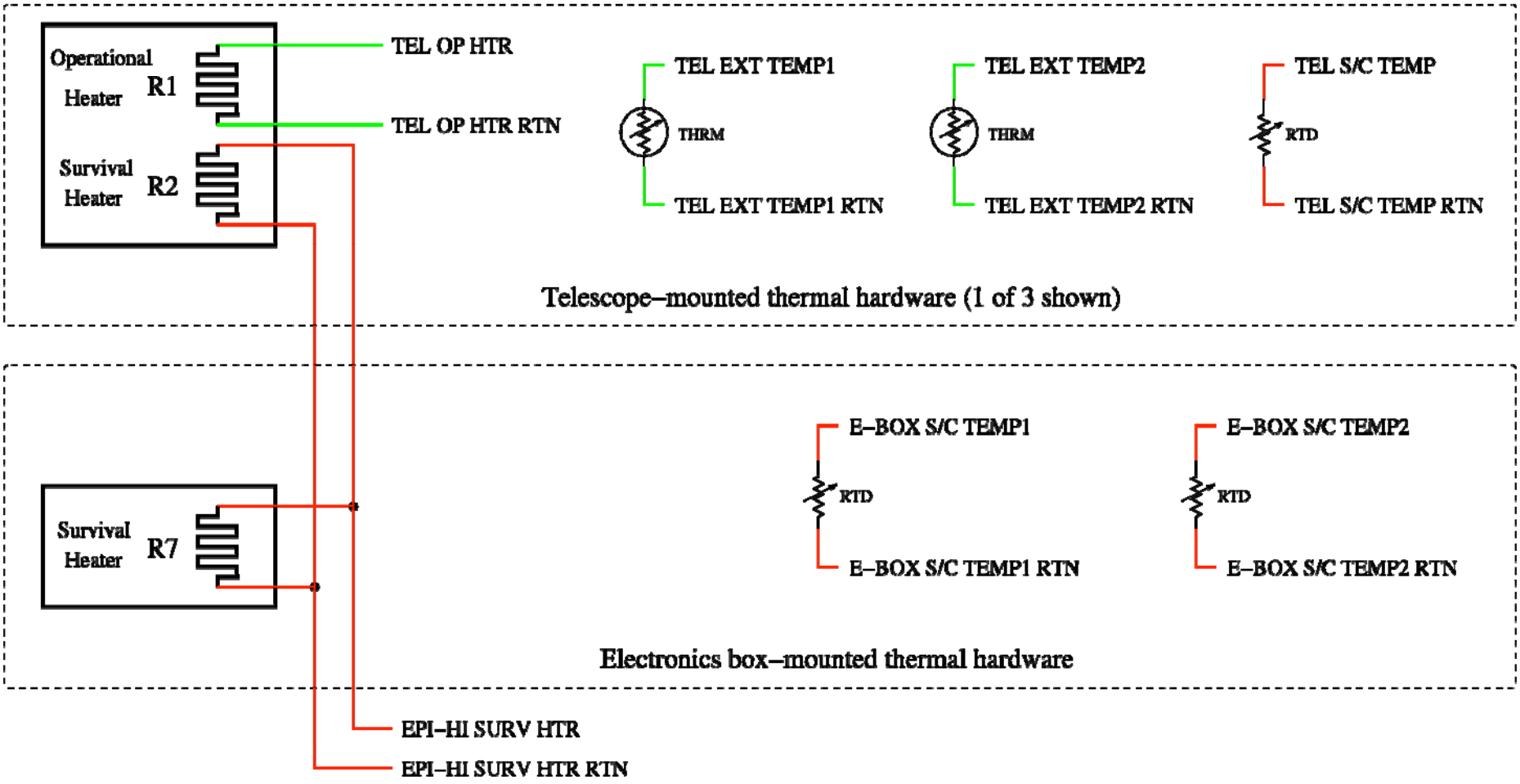
Resources - Mass

Subsystem	Mass [g]
LET1 telescope LET1 board	225 258
LET2 telescope LET2 board	145 233
HET telescope HET board	120 250
DPU board Bias Supply & RF shields LVPS & RF shields	197 225 + 130 160 + 100
Elec. box, hardware & shielding Telescope brackets Thermal hardware MLI blankets	925 + 250 +100 160 50 100
Total	3,628

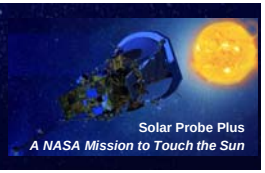
Harness Diagram



Thermal Harness Diagram



Summary



- Peer Reviews conducted on designs
  - PHASIC – Dec 2012 – all Action Items closed
  - DPU and Telescope Boards – Sep 2013 – all Action Items closed
    Schematics updated and layouts in process
  - Bias Supply Board – Sep 2013 – all Action Items closed
    Schematic updated and layout in process
- Testing of ASICs has shown good performance that will meet our requirements
- No issues with Parts List
- When all layouts completed and reviewed, fabrication and testing of EM begins