Solar Probe Plus

A NASA Mission to Touch the Sun

Integrated Science Investigation of the Sun
Energetic Particles

Preliminary Design Review

05 – 06 NOV 2013

EPI-Lo Electronics

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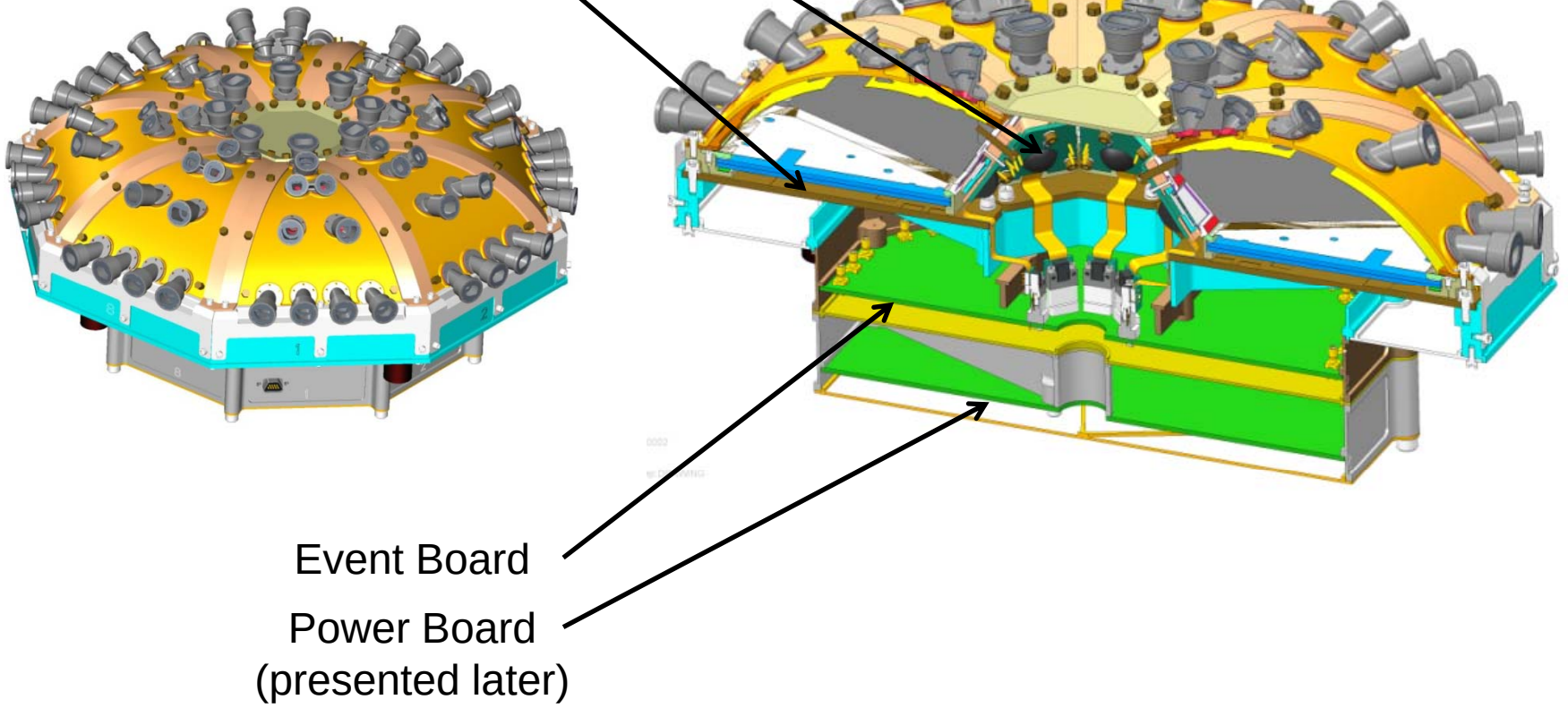
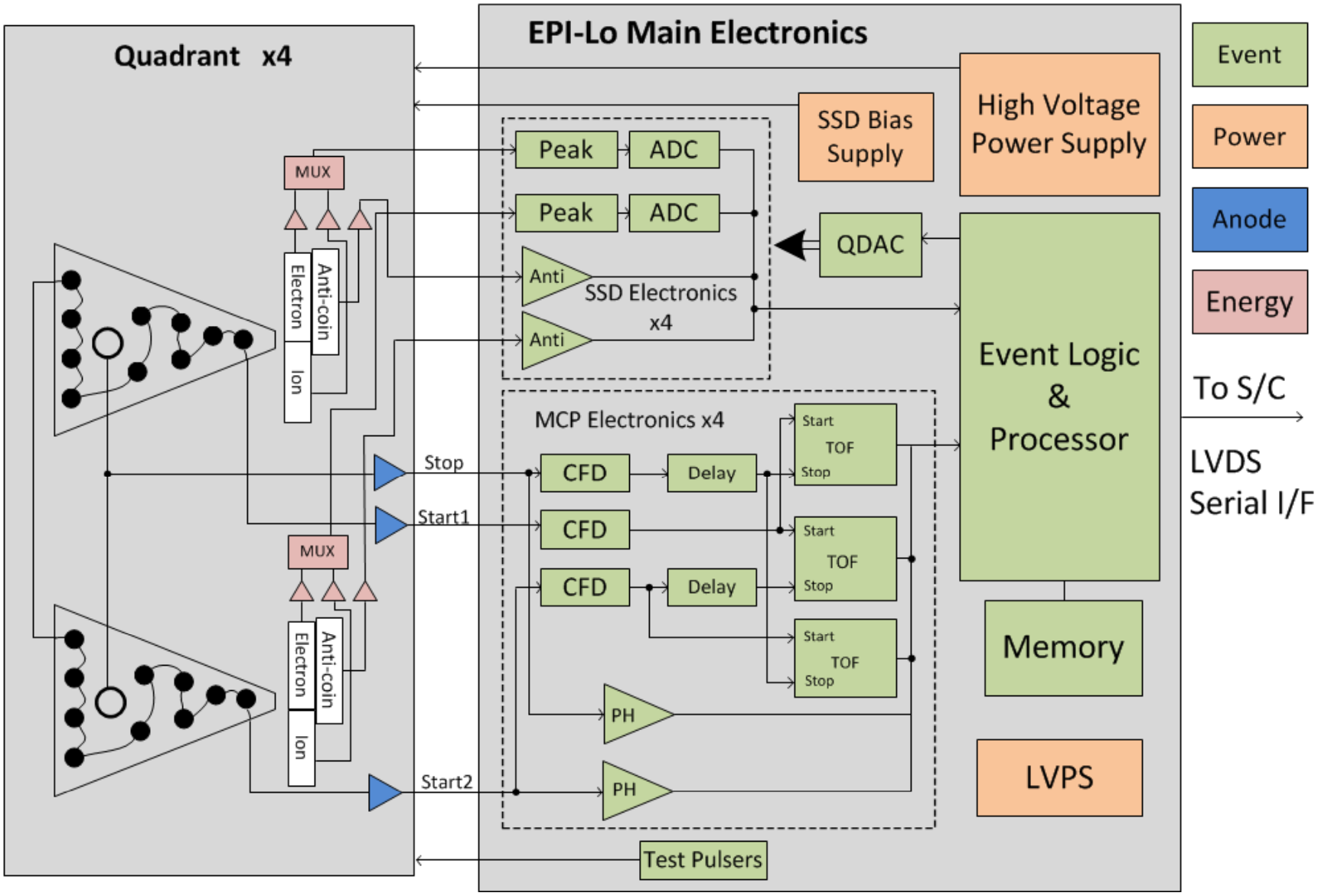
Outline

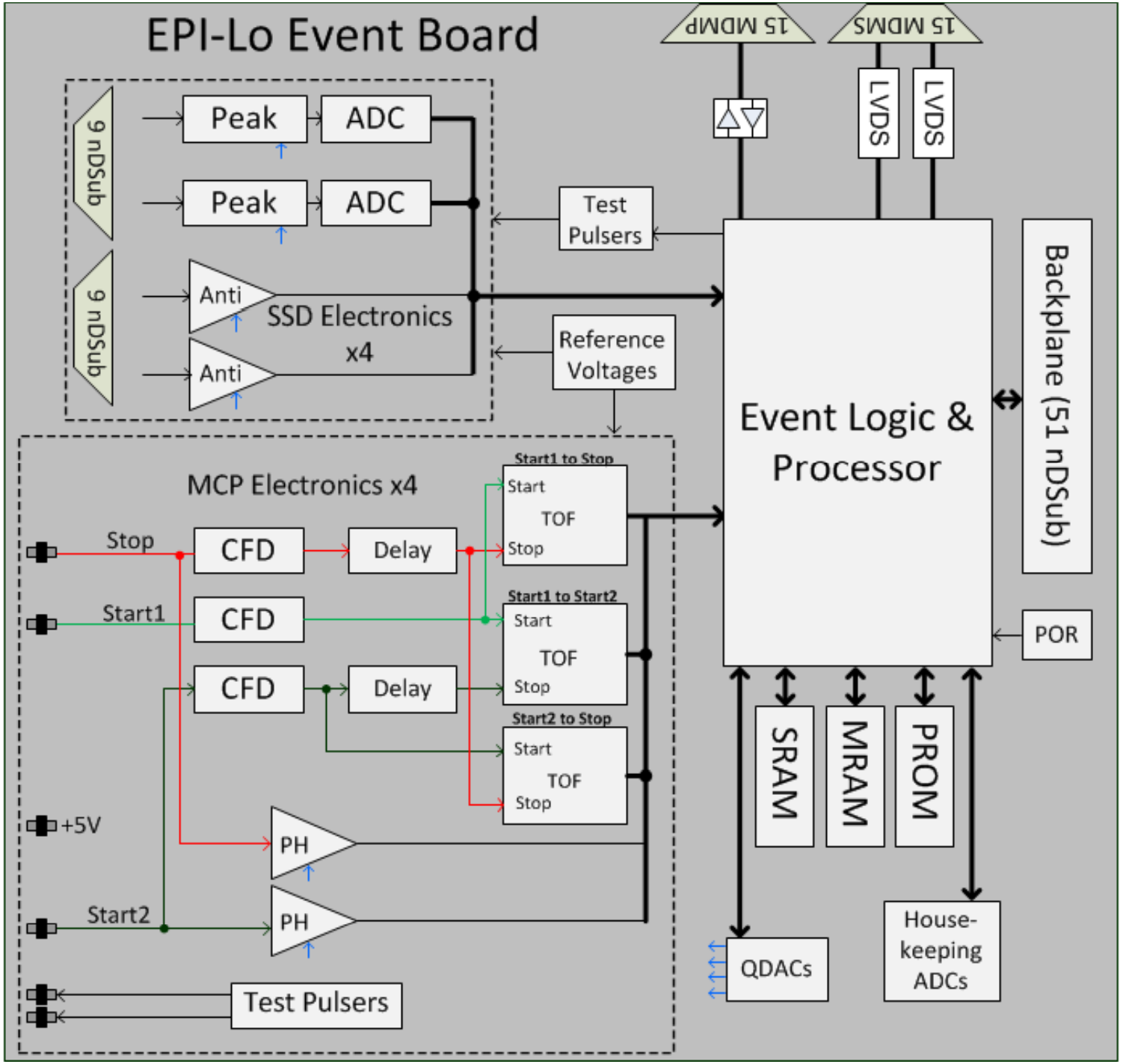
- Electronics Overview
- Block Diagrams
- Driving Requirements
- Event Board
  - Functionality, Interfaces, prototyping, FPGA, layout
- Anode Board
  - Functionality, Interfaces, prototyping, layout
- Energy Board
  - Functionality, Interfaces, prototyping, layout
- Packaging and Thermal Considerations
- Radiation Analysis
- Plans for Testing
- Preliminary Parts List and Special Screening Considerations
- Status Summary
- Plan Forward
- Peer Review Status

EPI-Lo – Electronics Overview



EPI-Lo Block Diagram




EPI-Lo Event Board
15 MDMP
15 MDMS
LVDS
LVDS
9 nDSub
9 nDSub
Peak
ADC
Peak
ADC
Anti
Anti
SSD Electronics x4
Test Pulsers
Reference Voltages
Event Logic & Processor
Backplane (51 nDSub)
POR
MCP Electronics x4
Start1 to Stop
Start
TOF
Stop
Start1 to Start2
Start
TOF
Stop
Start2 to Stop
Start
TOF
Stop
Stop
Start1
Start2
+5V
CFD
CFD
CFD
Delay
Delay
PH
PH
Test Pulsers
SRAM
MRAM
PROM
QDACs
House-keeping ADCs

Electronics Driving Requirements

- Analog Performance
  - Timing resolution < 400 ps FWHM
  - Energy resolution < 15 KeV FWHM
- MCP timing system dynamic range of 500 k to 25 M electrons
- Energy system dynamic range of 50 keV to 15 MeV
  - Higher energies (>1 MeV) use pulse width mode
- Temperature
  - Survival: -55°C to +85°C
  - Operational: -35°C to +65°C
- Radiation
  - TID: 25 kRad (based on FASTRad analysis)
  - SEL: 80 MeV-cm^2/mg
- Event board very similar to previous programs (RBSPICE, JEDI, EIS). All major changes have been prototyped.

Event Board Functionality (1/2)

- Instrument Processor
  - Embedded processor in RTAX2000
    - Execute flight code, accumulating and formatting telemetry, commanding, and alarm detection and action
  - Spacecraft Communication
  - Boot code in PROM, classification tables and application code in MRAM
  - Accumulate data into classification tables
- Event Processing
  - Communicate and handle timing with ADCs, TOF-Ds
  - Pre-process and accumulate event data
  - Accumulate rates
- HVPS Control
  - Control four opto-coupler generated HVPS outputs
  - Provide high speed safing of HVPS in response to over current

Event Board Functionality (2/2)

- Time-of-flight based on APL TOF-D and CFD-D ASICs
  - New ASICs developed for future programs
  - Improved size and performance from previous ASICs
  - 12 CFD-Ds and 4 TOF-Ds for timing system
- Solid-State Detector Energy Measurements
  - 8 Peak detect ASICs and A/D converters for energy system
  - Peak detect chips are APL ASICs flown on previous missions (PEPSSI, Jedi, RBSPICE)
- MCP pulse height comparators
- Pulsers
  - Independent pulsers for start and stop signals on each anode board
  - 2 pulsers for Energy system

Event Board Interfaces

- Solid-State Detector Interface
  - 8, 9-pin ndsub connectors to energy boards
  - ~10 mV to over 1 V unipolar-shaped pulses
  - Control, pulser, and power lines
- Anode Board Interface
  - 12 Time-of-Flight Coax connectors
    - ~10 mV to over 1 V fast-shaped pulses
  - 4 power and 8 pulser Coax connectors
- Test Port Connector
  - 2 test inputs (to aid in end-to-end timing tests)
  - 5 test outputs
- Spacecraft Data Connector
  - Redundant LVDS interface (2 drivers, 2 receivers)
- Power Board Connector
  - 51 pin ndsub connector for power and communication

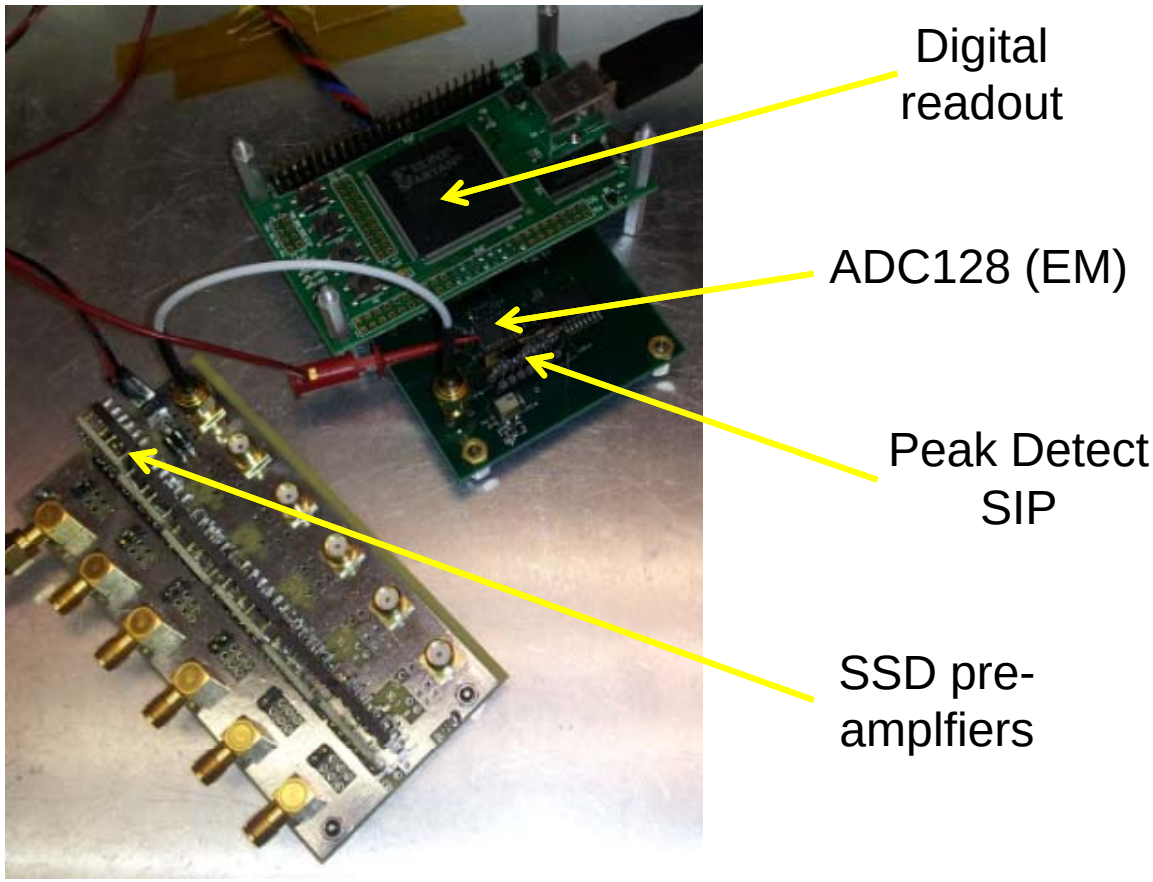
Energy System Updates

- Energy system re-designed from previous instruments
  - 8 ADC121s read out the 8 peak detect chips
  - Prior designs used MUX and one fast ADC
  - New design allows de-coupling of quadrants – each quadrant has completely independent readout electronics and can be operated as an individual instrument
  - Event logic will be identical for each quadrant, and then the data will be combined
  - New approach significantly simplifies event logic design and increases data processing rates and redundancy

Energy System Prototype

- Fully tested interface of energy chip to peak–detect SIP to ADC using flight-like components
- Energy resolution of test setup far exceeds requirement (15keV)

atten. DB	KeV	FWHM (KeV)
-6	912.161	8.78712
-7	812.964	6.26275
-8	724.555	6.08932
-9	645.760	5.81954
-10	575.535	5.5883
-15	323.647	4.91385
-20	182.000	4.64407
-25	102.346	4.50918
-30	57.553	4.29721
-35	32.365	4.14305
-40	18.200	4.54772



FPGA Functionality

- FPGA contains all event logic and event processing
  - SCIP: 16-bit 10 MIPS processor (reused custom embedded processor based on Harris RTX2010 and APL's FRISC)
  - Processor memory interface to PROM, MRAM, SRAM
  - Support I/O
    - Provide voltage supply clocks, read safing status, set thresholds, monitor housekeeping, etc.
    - LVDS spacecraft communication interface
    - Processor test port interface
  - Event Logic
    - Count sensor basic rates and diagnostic rates
    - Provide pulser stimulus
    - Collect and process TOF values to generate start direction and particle time-of-flight
    - Select appropriate SSD channel and record energy deposited
    - Detect anti-coincidence (electron only) and pulse-height over-threshold (start and stop)
    - Send selected valid events based on commanded event criteria to processor event buffer
    - Event logic test port for ground testing

FPGA Resources

- Actel RTAX2000SL -1 speed CCGA-624 (common buy part)
  - Estimate ~40% resource utilization based on RBSPICE design
  - Internal RAM for event FIFO only
    - No minimum size required and soft memory is fine (parity check)
  - 418 user I/O total, 18 spares
    - 3 spares to power board + 7 spares through Schmitt triggers to test connector + 8 true spares = 18 spares
    - Note: At the FPGA requirement review, moderate reuse designs are green for at least 17 uncommitted I/O pins
  - 1.5 V Core Voltage, 3.3 V I/O supply voltage
    - +/-5% voltage tolerance
    - Supplies can be powered up or powered down in any sequence as long as some app note details are considered
    - I/O are tri-stated during power-up

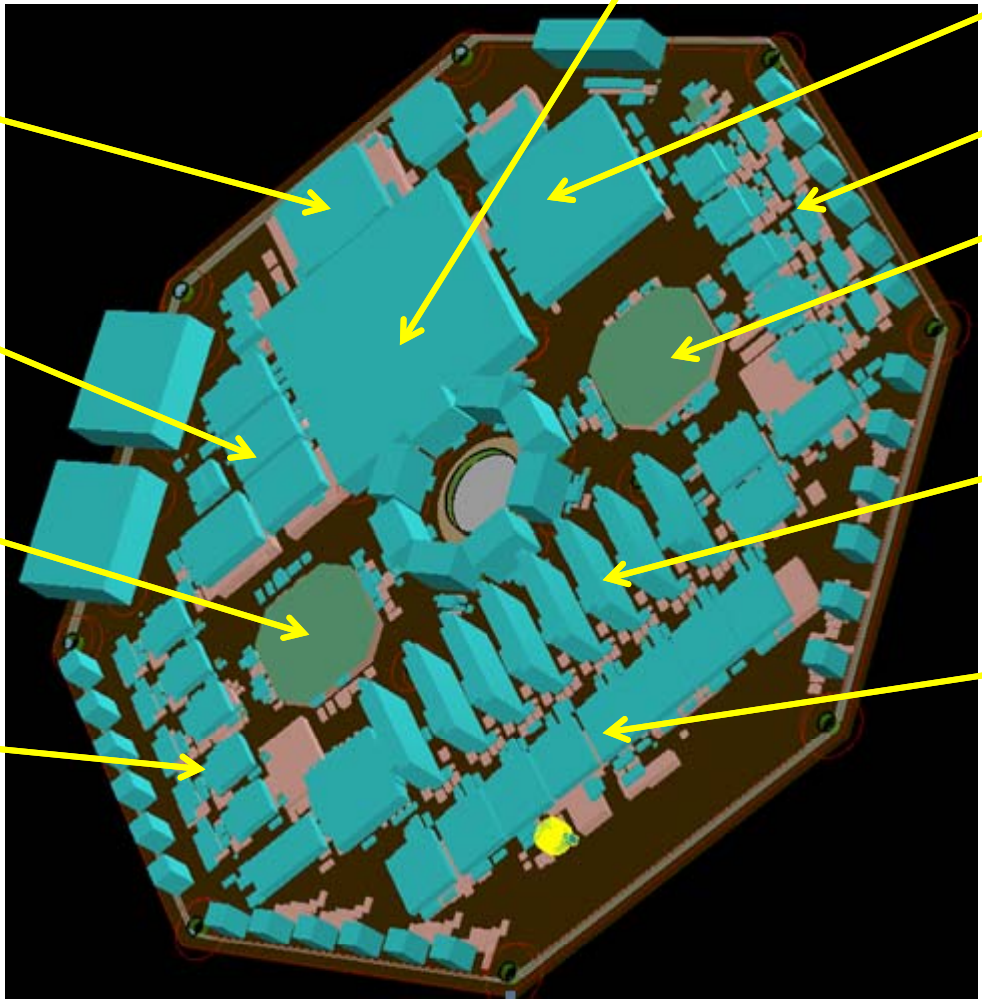
FPGA Development

- Part prototyping
  - Reprogrammable Aldec/Actel system for EM
  - Board layout also accommodates commercial socket if needed
- Design prototyping/reuse
  - SCIP is identical to RBSPICE
  - Similar approach to RBSPICE for many interfaces: S/C communication, power supplies, QDACs, test port, memories, peak detects, pulsers
  - New interfaces prototyped prior to EM: TOF-D rather than TOF-C, new ADC for HK and energy readout
  - Significant previous experience with all design tools: VHDL (with tcl scripts, pdc files etc.), Synplify Pro, Actel Libero, ModelSim
- No expected areas of concern
  - No timing closure challenges expected (most of design at 10 MHz, some at 40 MHz)
  - Primarily synchronous design techniques with standard clock domain crossing techniques and no gated clocks
  - Straightforward reset filtering and routing network
  - Sufficient clock nets available for clocks and reset

Event Board Layout

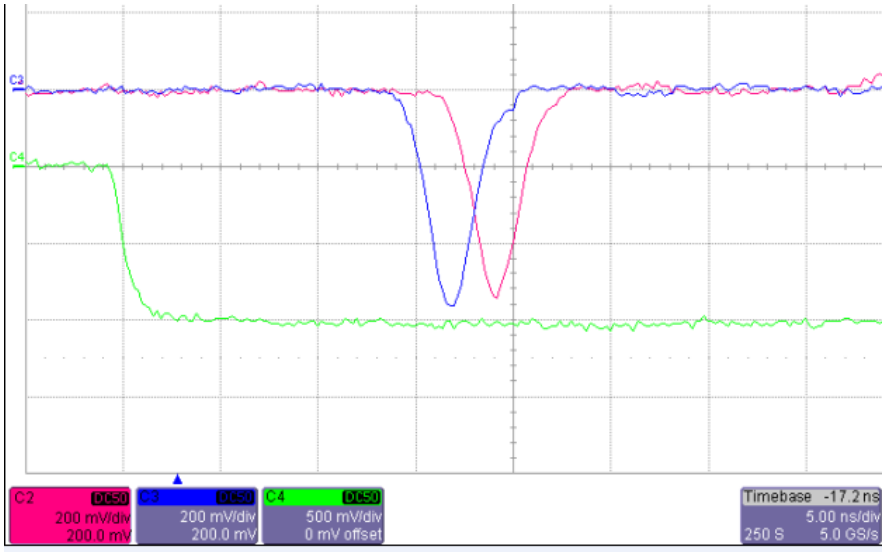
- Sensitive analog is separated from digital
  - FPGA, S/C communication, SRAM, PROM, MRAM, and oscillator on top of board
  - TOF electronics on left and right of board
  - Peak detect and ADC electronics on bottom of board
  - All critical routing isolated by ground planes from digital routing
- 12 layers, 2 ground planes, 2 power planes, 8 routing planes
- Actel located with SRAM directly adjacent
  - Reduce track-length to SRAM to reduce noise
  - Actel on Primary side, to allow the Development Tool access to the program pins

Event Board Layout



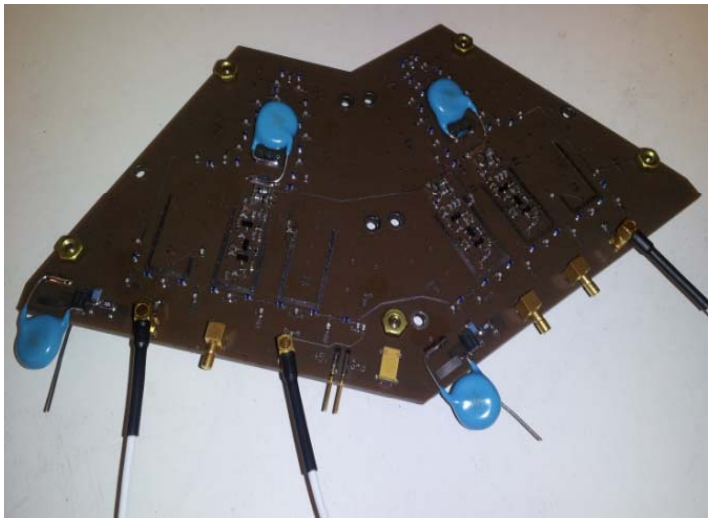
Anode Board Description

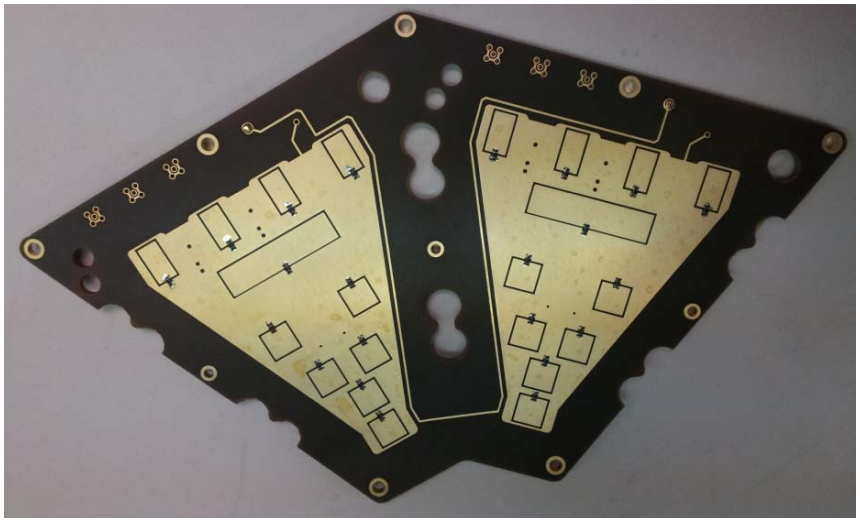
- Functionality
  - 3 fast discrete amplifiers
    - Stop anode and each end of the start delay line
    - 50 ohm impedance matched, designed to drive 50 ohms
  - Anode is at 3kV, PCB embedded capacitors isolate HV from LV
  - 1 start pulser and 1 stop pulser
    - Start pulser location in imaginary anode between sensor wedges
- Interfaces
  - 6 coax SSMB connectors
  - Power, 3 outputs, 2 pulsers
  - HV connection for anode



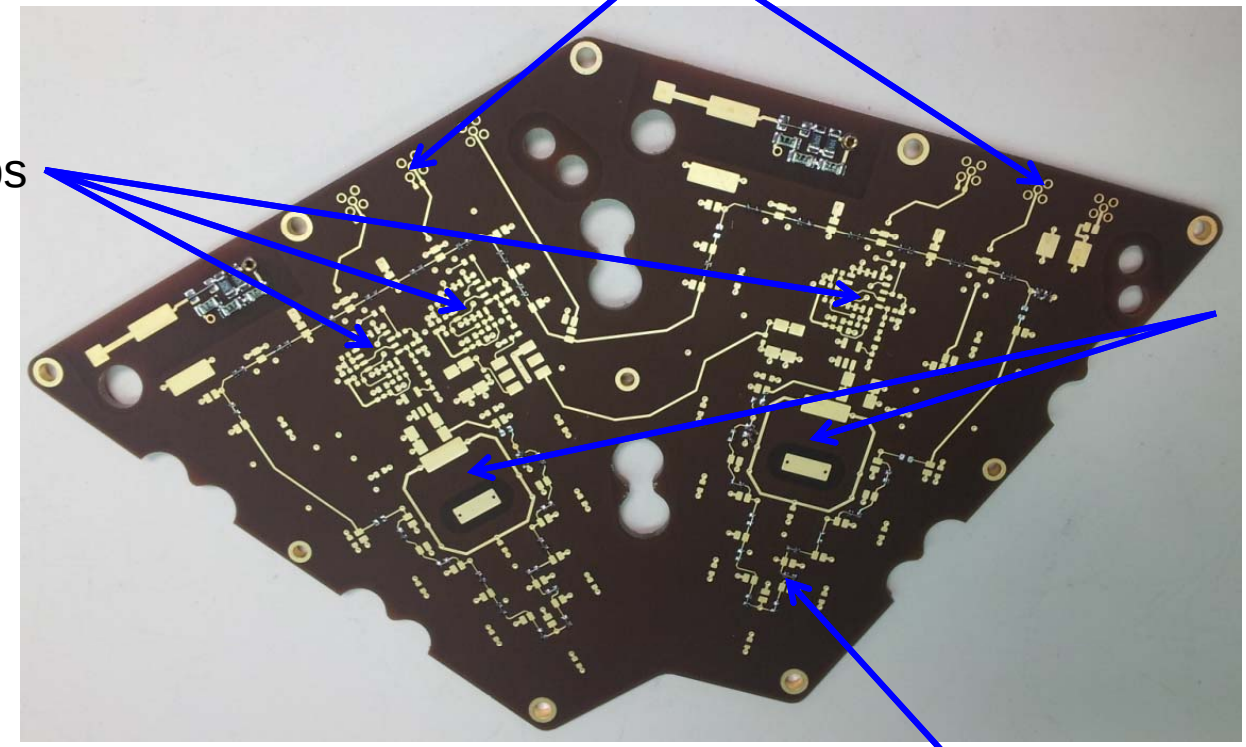
Anode Board Prototyping

- Initial prototype board fabricated, assembled, and tested
  - First implementation of embedded capacitors for HV anode
  - Verified quadrant design
- EM anode board fabricated, assembled, and in testing
  - Electrical and mechanical interfaces well defined
  - Position mapping on prototype verified simulations for start pad locations
  - Kapton layer provides dielectric strength of ~20kV for embedded capacitors
    - Passed 10 day, 2x HV standoff test (recommended by Steve Battel)
  - APL packaged transistor array



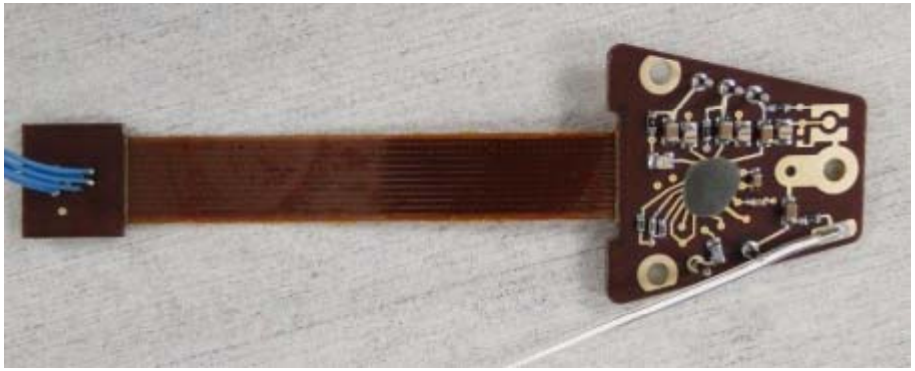


Anode Board Layout

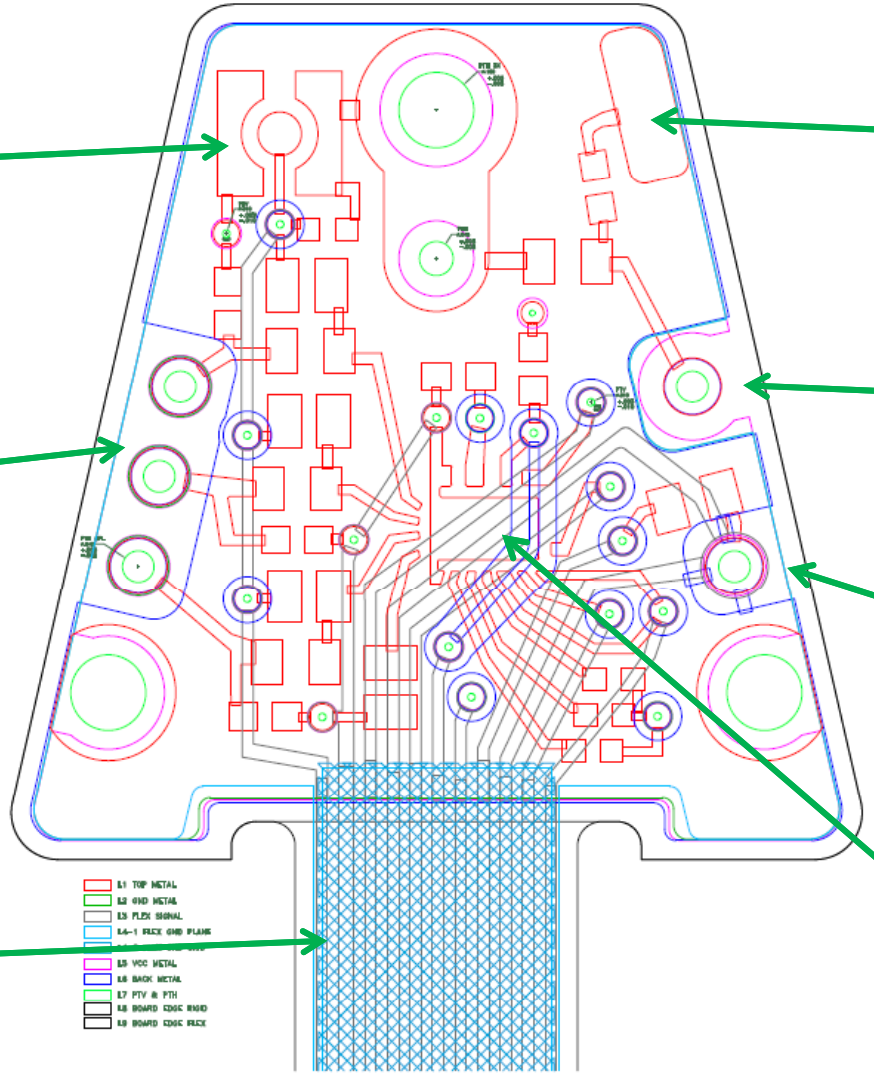


Energy Board

- Functionality
  - SSD Pre-amplifier and shaper
  - Energy ASIC supports 3 pre-amplifiers and MUX
    - Ion channel, electron channel, anti-coincidence channel
    - Select between ion channel or electron and anti-coincidence channels
  - Thermistor for temperature measurements
  - Test connector for pulser inputs
- Interfaces
  - 9 pin ndsub connector for power, signals, pulser, and temperature monitor
  - Bias voltage from separate HV wire (<200V)
  - Test connector (MMCX)
  - SSD connections (Mill-Max Socket)
- EM energy board fabricated and in testing

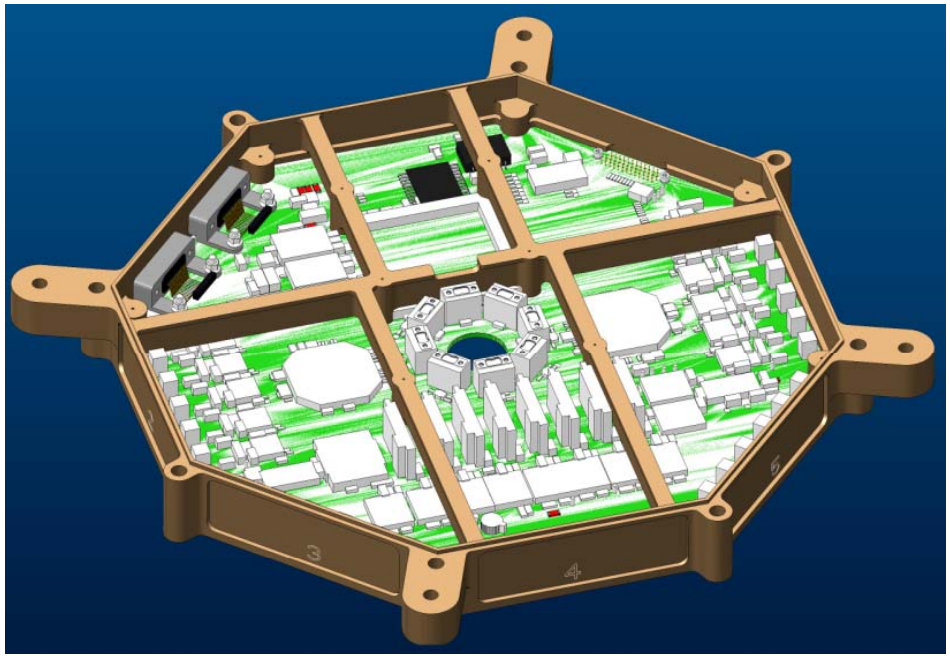


Energy Board Layout



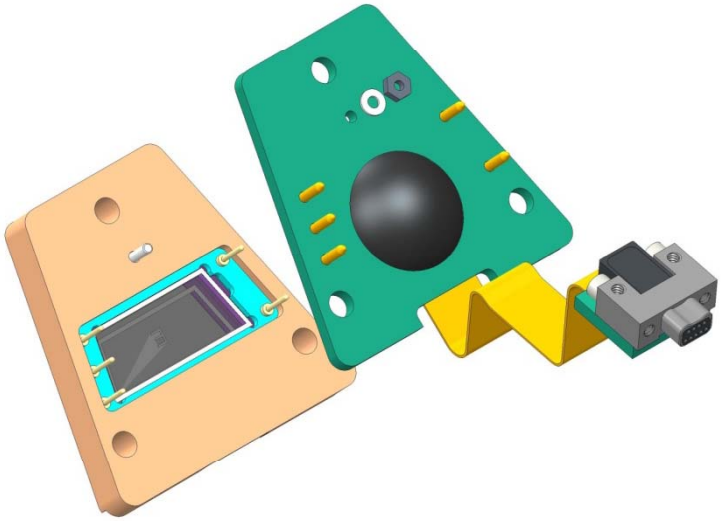
Event Board Packaging

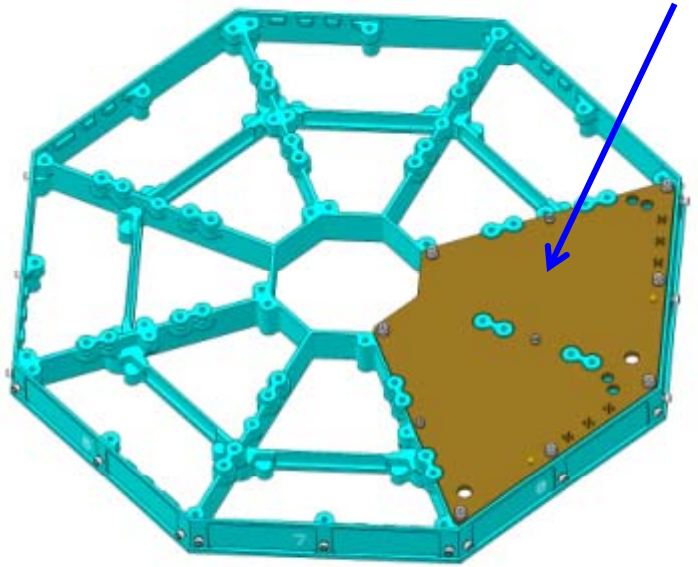
- Packaged in octagon frame “slice”
  - Board is loaded from the bottom and has six center mounting supports and full contact around the perimeter
  - FPGA is supported on four corners
- Large number of thermal vias under the higher power parts
  - Actel, RAM, and MRAM to dissipate power into the board planes and out to the frame.
  - Total board power is ~1 watt. No thermal issues expected.



Anode and Energy Board Packaging

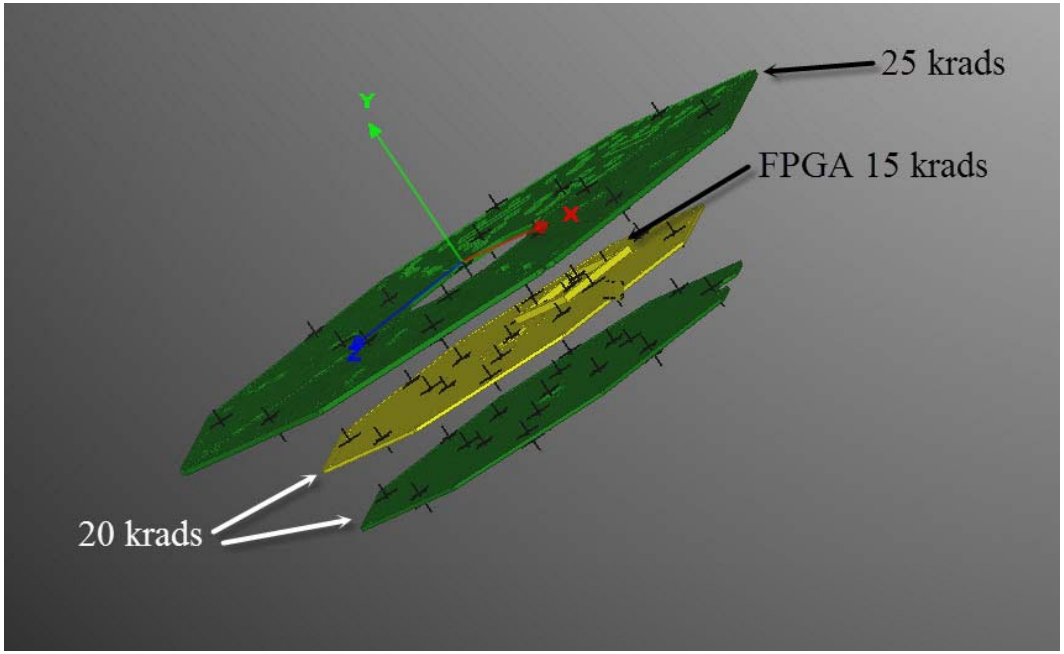
- Anode Board
  - Mounted to instrument main support structure
  - Total board power is 90 mW, no thermal concerns
- Energy board is mounted directly behind SSD
  - Total board power is 25 mW, no thermal concerns





Radiation Analysis

- FASTRad analysis performed on instrument in S/C model to predict doses seen at electronics (bracket, instrument, and S/C modeled)
- Electronics boards: <25 krad
- Detectors: <40 krad



Plans for Testing

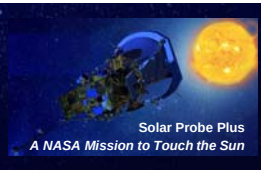
- Follows APL Manufacturing Flow, these are significant highlights
  - Populate Passive Components
  - Execute Test Procedure to Verify Passive Components
  - Populate First-level Active Components
    - Voltage References, Power-on Reset, Oscillator, applicable Tailor Flags
  - Execute Test Procedure to Tailor and Verify First-level Active Components
  - Populate Actives and Install Known Tailors or Tailor Flags
  - Install into Flight Frame
  - Execute Test Procedure to Test and Tailor Entire Board
  - ESS Testing
  - Execute Functional Test Procedure
  - Photograph and Conformal Coat
  - Execute Test Procedure to Calibrate and Characterize Board (over temperature)
  - Release to Next Assembly

Preliminary Parts List

- Investigating ADC for single event transients
- ADCMP600 being qualified by project
- Transistor array die being packaged by APL into ceramic 16 pin LCC

Function	Preliminary Part Number	Manufacturer
Event Board		
RTAX2000	RTAX2000SL-CGS624E	Actel
RAM	HLXSR01632	Honeywell
MRAM	UT8MR2M8-40YPC	Aeroflex
PROM	UT28F256LVQLE-65UPC	Aeroflex
Oscillator	1103D40M00000BX	Vectron
LVDS	UT54LVDS032LV-UPC	Aeroflex
LVDS	UT54LVDS031LV-UPC	Aeroflex
Schmitt Trigger	UT54ACS14E	Aeroflex
Comparator	ADCMP600BKSZ	Analog Devices
Op-amp	RH1078MW	Linear Technology
MDM connector (test)	MWDM2L-15PSMRTN	Glenair
MDM connector (data)	MWDM2L-15SSMRTN	Glenair
ndsub for SSDs	891-007-9S-__-BST-_-T	Glenair
ndsub for inter-board	891-006-51P-__-BST-_-T	Glenair
coax for anode board	050-451-0000-220	ITT Canon
Reference	RH1009MH	Linear Technology
ADC	ADC128S102WGMPR	TI
POR IC	ISL706ARHF	Intersil
Level Shifter	UT54ACS164245S-UPC	Aeroflex
CFD ASIC	10946-CFD-D-03	APL ASIC
TOF ASIC	10946-TOF-D-03	APL ASIC
DAC ASIC	10946-QDAC2B-01	APL ASIC
Energy Board		
Energy Chip	7425-5214-01	APL ASIC
Anode Board		
Transistor Array	ISL73096	Intersil

Status Summary



- Event Board
  - EM parts placement complete
  - Routing in process
  - EM PCB expected in December
  - All critical circuits have been prototyped
- Anode Board
  - Prototype anode board fabricated, assembled and tested
  - EM anode board fabricated, assembled and testing in process
  - 10 day, 2x HV standoff test successfully completed on EM
- Energy Board
  - EM board fabricated, assembled, and testing in process

Plan Forward

- Anode Board
  - Complete testing on anode board
  - Fabricate flight anode board
- Energy Board
  - Complete testing on energy board
  - Fabricate flight energy board
- Event Board
  - Fabricate EM board
  - Complete testing on EM board
  - Fabricate flight Event board
- Finalize all documentation and procedures for flight build
- Build, tailor, calibrate, and qualify flight units

Peer Review Status

- Event and Power Board Peer Review
  - August 21, 2013
  - Summarized with action items in memo SRI-13-029
  - 11 action items generated / 11 action items closed (6 for event board)
- Anode Board Peer Review
  - June 21, 2013
  - Summarized with action items in memo SRI-13-025
  - 6 action items generated / 6 action items closed
- Energy Board Peer Review
  - August 26, 2013
  - Summarized with action items in memo SRI-13-030
  - 4 action items generated / 4 action items are closed
- Parts Stress Analysis
  - No issues expected
- WCA
  - No issues expected