Solar Probe Plus

A NASA Mission to Touch the Sun

Integrated Science Investigation of the Sun
Energetic Particles

Preliminary Design Review

05 – 06 NOV 2013

EPI-Hi Technology Development

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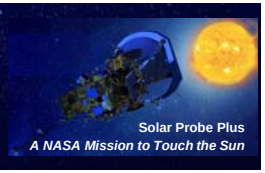
EPI-Hi Lead Co-I

Outline



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- Radiation Tolerance Testing
- Mechanical Robustness
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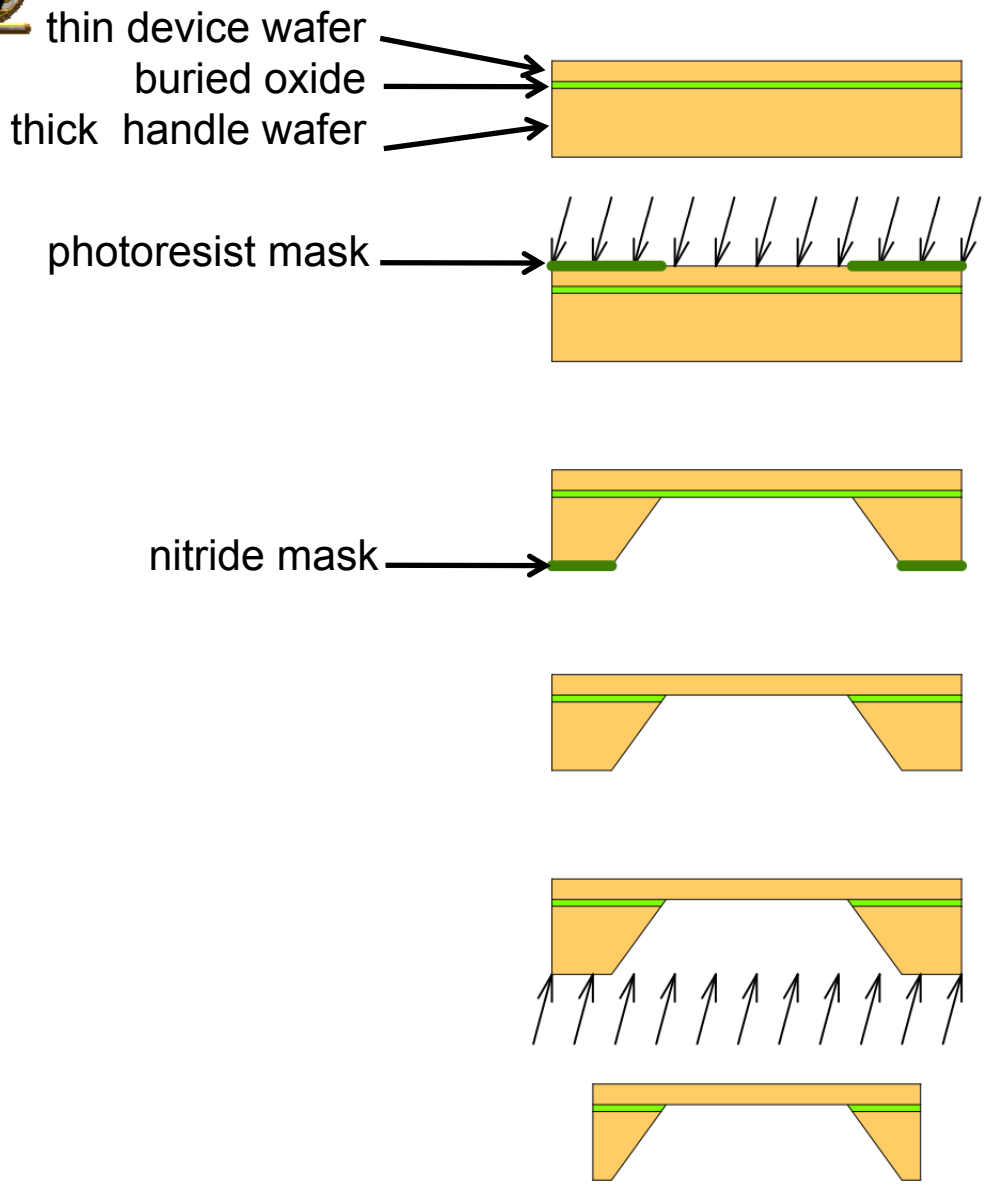
- Summary

Objective

Develop a new approach to fabricating multi-element ion-implanted silicon solid-state detectors thinner than ~30 μm with the following features:

- Thicknesses in the range ~10 to 30 μm
- Good control of absolute thickness and detector-to-detector variation (±1 μm)
- Good thickness uniformity (~0.2% or better rms variation) to allow good species resolution (e.g., He isotope separation)
- Mechanical robustness to provide good manufacturing yield and to survive launch environment without breaking

Thin Silicon Detector Fabrication Process Summary



silicon-on-insulator (SOI) wafer is a commercial product with excellent device layer uniformity and control

ion implant to produce diode pn junctions on device layer

wet etch to remove handle layer under active area—oxide acts as etch stop and preserves the thickness uniformity of the device layer

etch away oxide from underneath the active area using HF, which has negligible effect on the silicon

ion implant from back to produce detector's ohmic contact

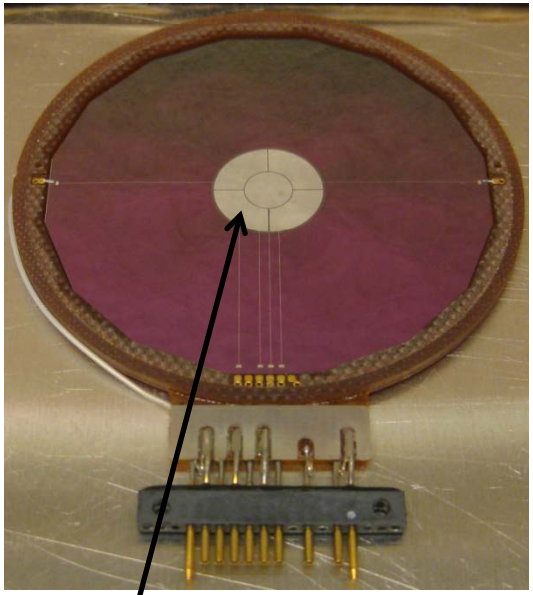
dice wafer into individual thin detectors with thick supporting frames

Development Strategy and Status

- Background
  - Prototyping studies carried out by a collaboration between LBNL (diode fabrication) and Caltech/JPL since 2003
  - Prior Caltech/JPL collaboration with Micron Semiconductor (Lancing, Sussex, England) allowed them to develop the capability for making thin, supported detectors from conventional silicon wafers; thickness control and uniformity did not meet specifications
- Phase B Activity
  - Efforts to prototype EPI-Hi thin detectors from SOI wafers have been funded during phase B both at Micron and LBNL
  - Testing and evaluation being carried out by the manufacturers and by Caltech/JPL and GSFC
- Flight Detectors
  - Plan to down-select to a single source for flight detectors based on test results

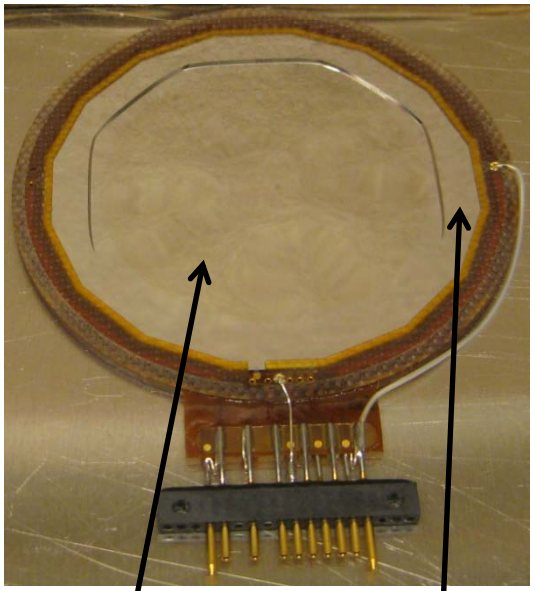
Prototype Thin Detectors

L0 Detector from Micron Semiconductor



front

active area
(1 cm^2)

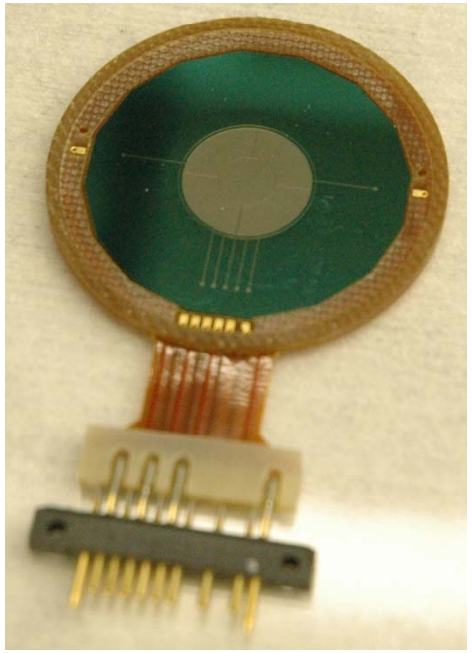


back

12 μm
membrane

thick
frame

L1 Detector from LBNL



Note: thick frames on L1 detectors extend inward nearly to the edge of the active area.

Tests Required to Achieve TRL6

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Determining that this technology for fabricating thin silicon detectors has achieved TRL6 (prototype demonstration in a relevant environment) requires demonstration that:

- The detectors yield the expected charge signals proportional to deposited energy that is characteristic of conventional silicon solid-state detectors when exposed to energetic ions
- A detector telescope using the detectors for measuring dE/dx can resolve elements and He isotopes
- The detectors have depletion and breakdown voltages acceptable for use in a solid-state detector telescope
- The detector characteristics are stable over an extended period (weeks) in vacuum at a nominal maximum temperature of 40°C
- The detectors can survive high radiation doses without degradation beyond that expected from displacement damage in conventional silicon detectors
- The detectors are mechanically robust enough to survive the acoustic loads expected at launch

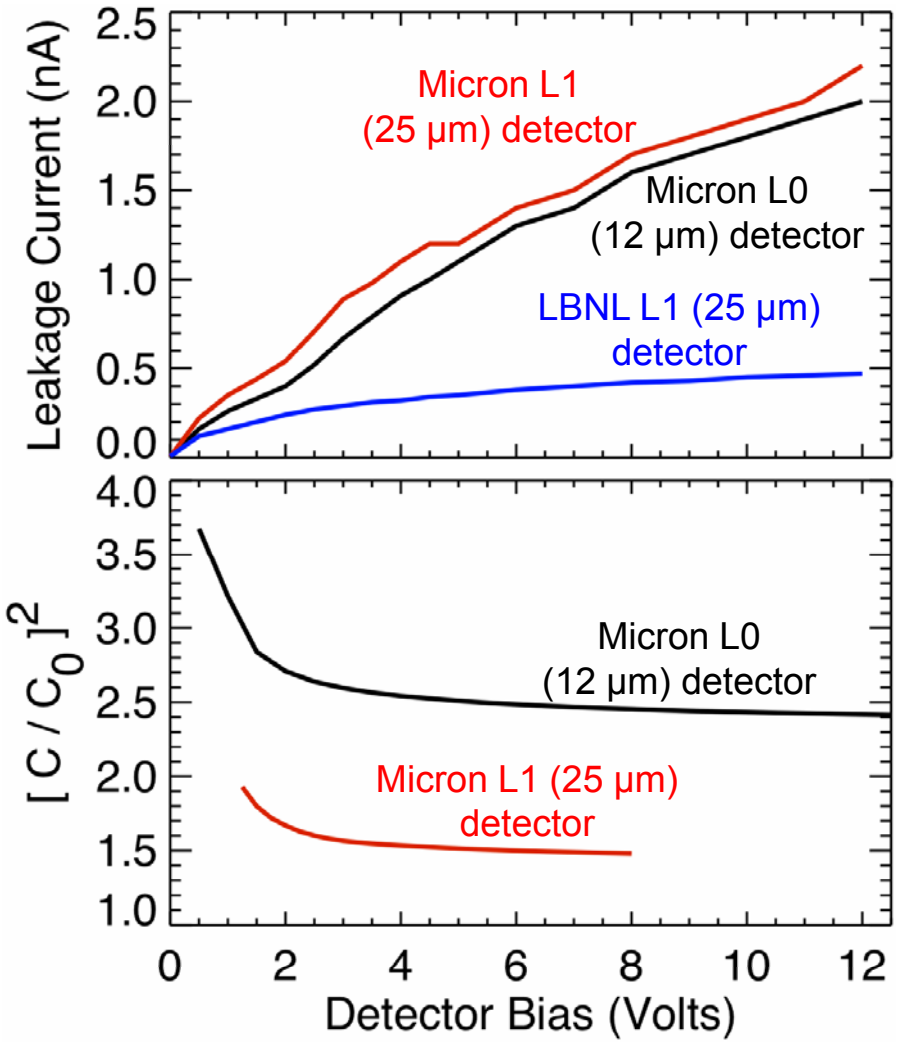
Fidelity of the Test Article

- Flight detectors are expected to be identical to the prototypes
  - The same photolithography masks will be used
  - No changes are anticipated in process parameters (ion implantation energy, annealing temperature and time, etc.)
  - It presently appears that a sufficient supply of SOI wafers may be left over from the phase B work to allow fabrication of all of the flight detectors and spares
  - No changes are anticipated in the detector mounts (provided by GSFC to both LBNL and Micron)
- Possible exceptions
  - If LBNL is selected to make flight detectors, adhesive used for gluing detectors into mounts may be changed to that conventionally used by Micron

Tests Performed

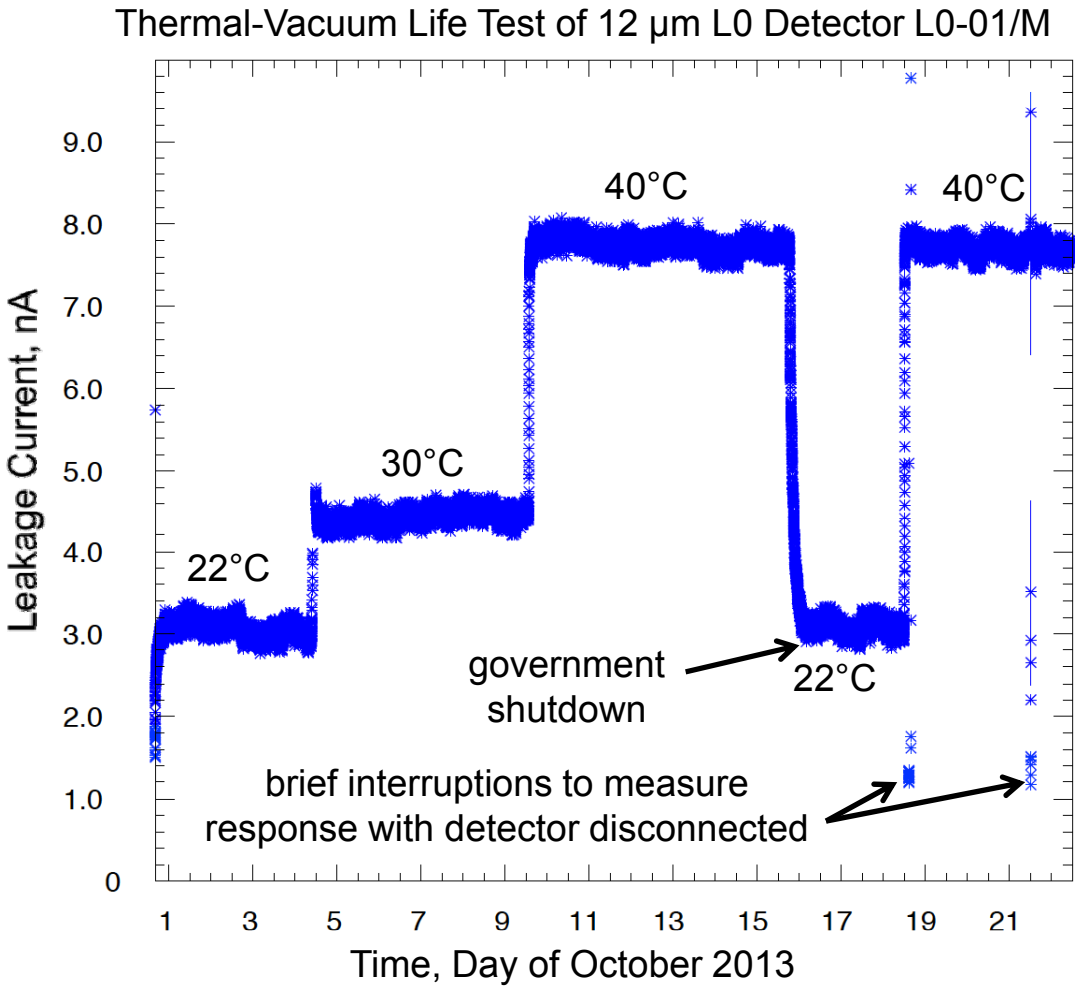
- Electrical characteristics
  - Leakage current versus bias (IV) —> maximum operating voltage
  - Capacitance versus bias (CV) —> bias required for full depletion
- Particle response
  - Alpha particles from ^{244}Cm source (5.8 MeV —> 1.45 MeV/nuc)
  - Accelerator beams of heavy ions
  - Thickness characteristics inferred from particle data
- Stability in expected environment
  - Thermal-vacuum life test at GSFC—our standard test for flight qualification of all silicon detectors
  - Total dose testing using ^{60}Co gamma-ray source at JPL
- Mechanical robustness
  - Acoustic test of mechanical model made from thinned SOI

Electrical Characteristics



- Measurements of leakage current versus applied bias (IV curves) are used to determine the highest allowed bias voltage before onset of electrical breakdown
- breakdown voltages are found to be >25V for both the L0 and L1 detectors
- Measurements of detector capacitance versus applied bias (CV curves) are used to determine the minimum bias required to totally deplete the detector
- Depletion voltages are found to be ~2V for L0 detectors and ~3V for L1 detectors
- Capacitances at full depletion exceed those obtained from a simple parallel plate capacitor calculation (C0) due to dead layers and to the capacitance of traces connecting active elements to wirebond pads
- CV measurements have not yet been made for the LBNL detectors, but particle data indicate that depletion voltages are similar to those obtained for the Micron detectors

Thermal-Vacuum Stability Test

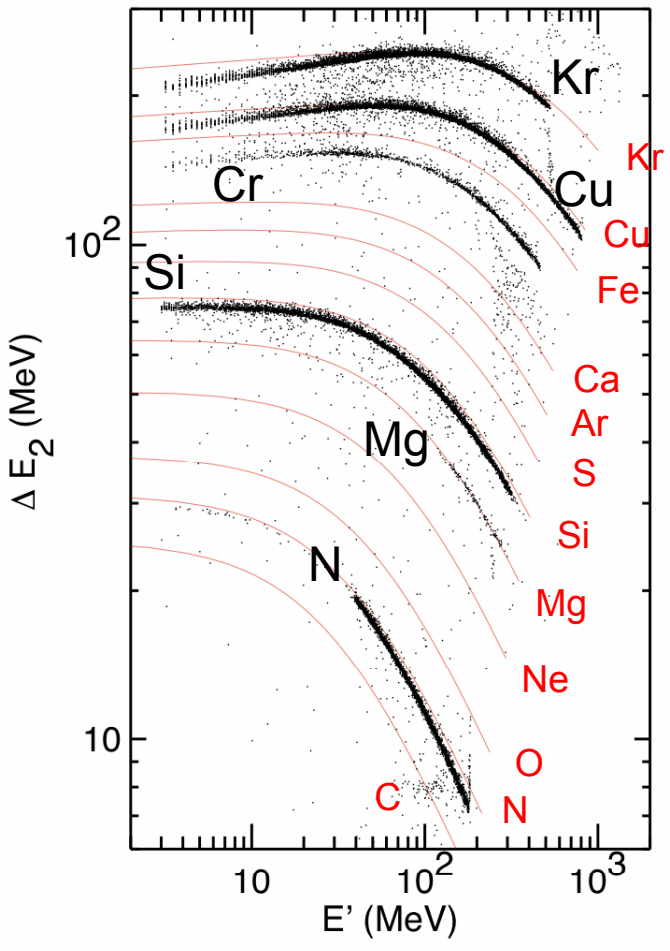


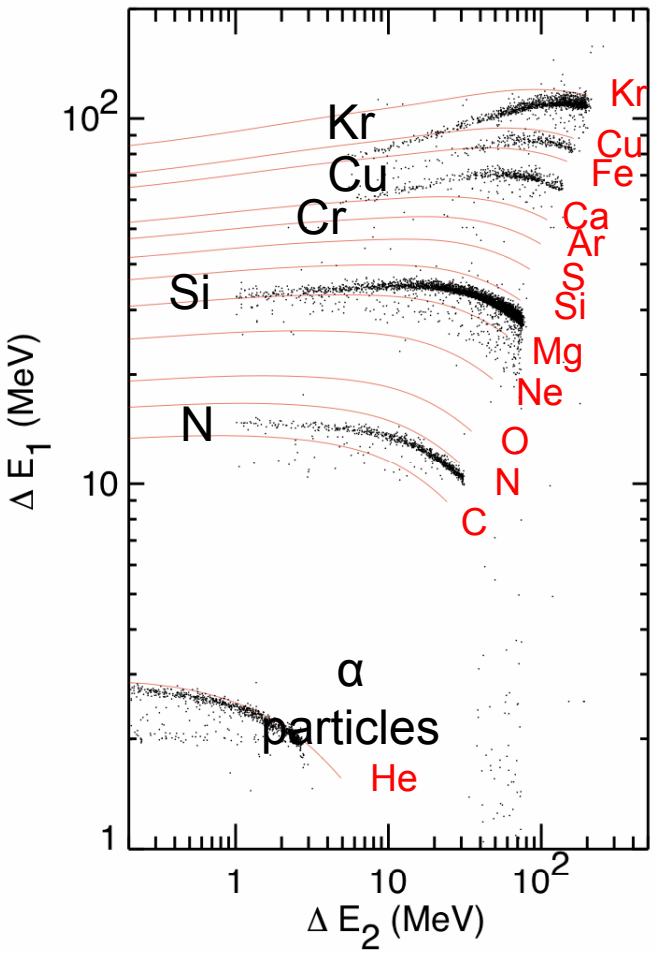
- The detector has performed stably (no indication of leakage current growth problems) over more than a week
- Test at GSFC is now continuing after the end of the October due to government shutdown
- Typical practice on previous missions has been to test candidate flight detectors for about 3 weeks at 40°C

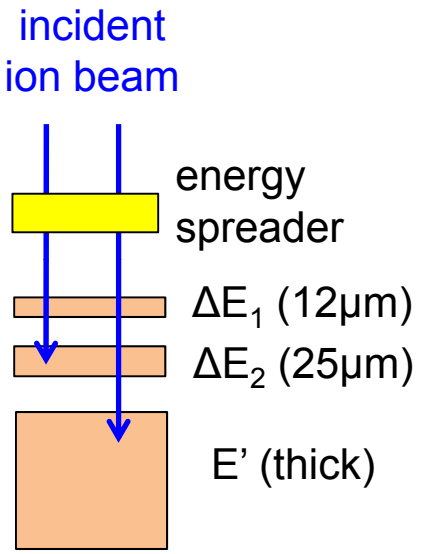
Accelerator Test Using Heavy-Ion Beams

red curves: calculated response; black points: measured events

LBNL 88-inch Cyclotron, 16 MeV/nuc Cocktail Beam, 3 Oct 2013



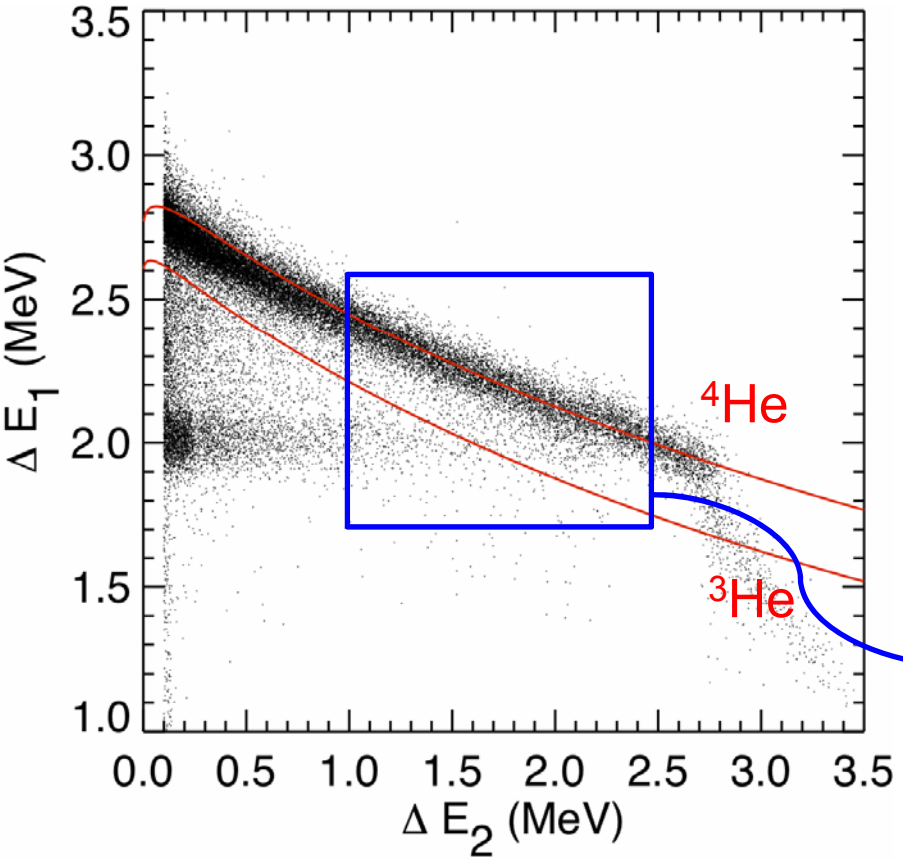




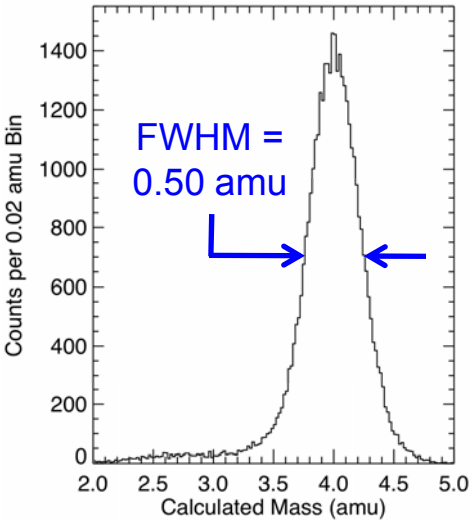
Obtained similar performance using two 12 μm detectors from Micron and two 25 μm detectors from both Micron and LBNL

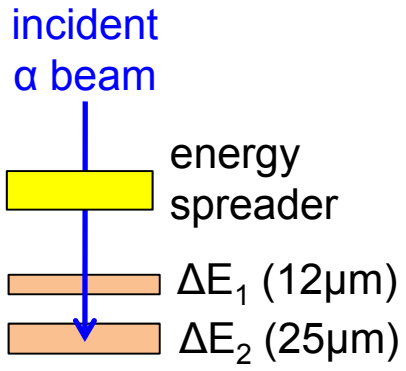
Tests with a Radioactive Source of Alpha Particles

- He track obtained using a 12 μm L0 detector to measure ΔE and a 25 μm L1 detector to measure E'
- Compare with calculated He isotope response tracks
- Adjusted ΔE thickness to 11.8 μm and dead layer to 0.1 μm to improve agreement

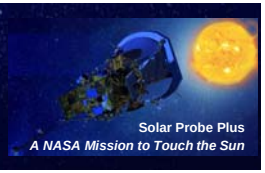


- Derived mass resolution demonstrates that detector has the required thickness uniformity
- Thickness variation measured by SOI manufacturer <0.8 μm (wafer to wafer and across individual wafers)





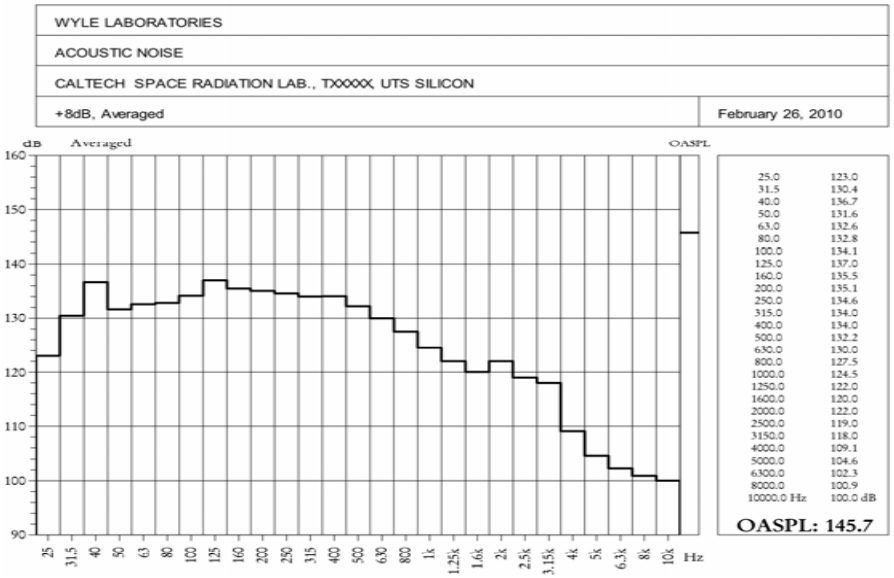
Radiation Tolerance Testing



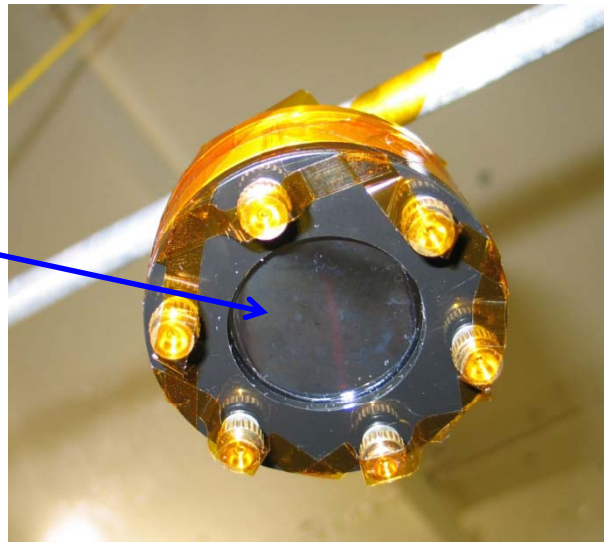
- Thin detectors will receive high radiation dose because, of necessity, there is very little shielding in front of them
- Using the 95% confidence worst-case mission fluences from the EDTRD we have estimated total doses to the L0 and L1 detectors over the SPP mission of about 10 Mrad and 2 Mrad, respectively
- One L1 detector from each manufacturer has been subjected to a total dose test at the JPL high-dose-rate facility (^{60}Co source)
- Detectors irradiated in the dark with bias applied to simulate conditions in flight
- Irradiations done in a series of increasing steps with measurements of characteristics after each step
  - step 1 (16 Oct 2013): 100 krad
  - step 2 (17-18 Oct 2013): 1 Mrad
  - one or two additional dose increments are planned
- Detector leakage currents increased as a result of the irradiations but are still at acceptable levels (<10 nA at a nominal 10 volt bias)
- Alpha particle tests of the detectors showed no degradation of charge collection efficiency or energy resolution

Mechanical Robustness

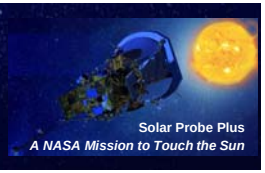
- Silicon membrane of the diameter planned for the L0 detector was fabricated from an SOI wafer with 10 μm device layer and subjected to an Atlas V acoustic test at a level significantly exceeding the SPP specification
- The sample survived without any problems



highest test level: 145 dB = SPP spec + 8 dB



Transition to Flight



- Extend selected prototype tests to cover additional detectors that have been fabricated in phase B—determine whether there are any detector-to-detector differences that might affect
  - Yield
  - Selection of manufacturer for flight detectors
  - Test program needed for flight devices
- Select manufacturer for flight detectors

Summary

- New technology for fabricating silicon solid-state detectors at least as thin as 10 μm has been developed based on the use of silicon-on-insulator (SOI) wafers as the raw material
- Detectors have been successfully produced by two manufacturers:
  - Micron Semiconductor Ltd., Lancing, Sussex, England
  - Lawrence Berkeley National Laboratory in collaboration with Caltech
- Prototypes from both sources have been subjected to all of the tests required for achieving TRL6 without problems
- Extension of a few tests is still in progress:
  - Additional time for the thermal-vacuum life test
  - Exposure to additional radiation doses
  - To date, the LBNL/Caltech fabrication has produced L1 detectors but L0 detectors remain to be completed. The LBNL/Caltech process has previously yielded good detectors as thin as 10 μm in sizes comparable to L1. Fabrication of L0 detectors has already passed the critical thinning step.