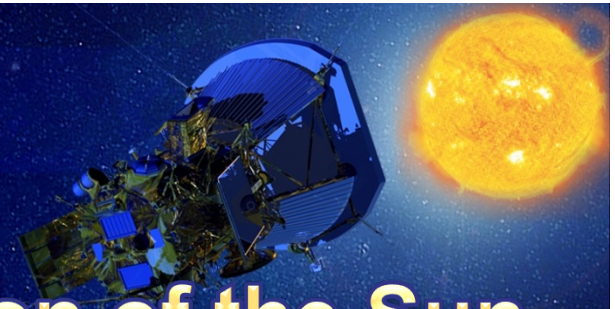
Solar Probe Plus

A NASA Mission to Touch the Sun



Integrated Science Investigation of the Sun
Energetic Particles

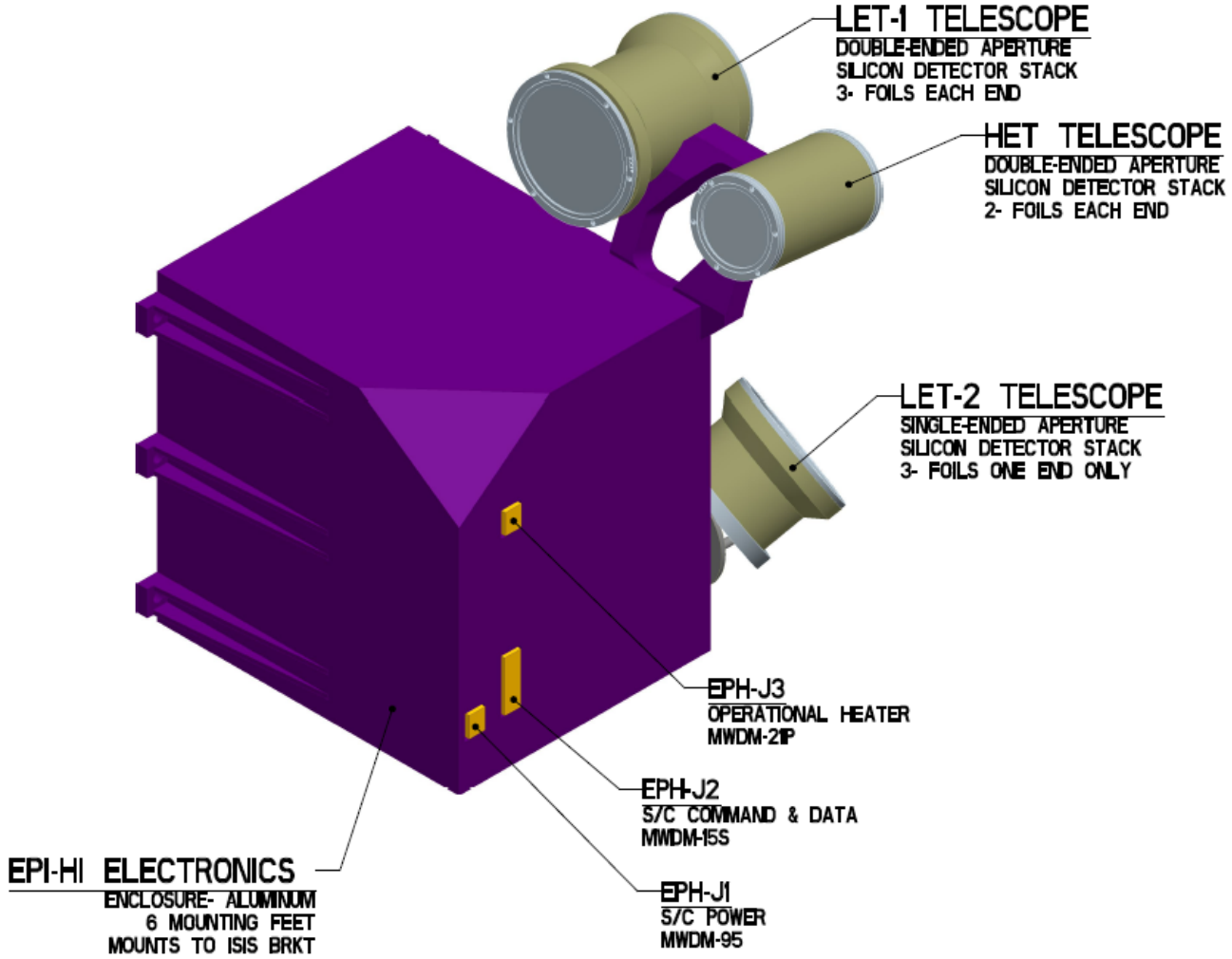
Preliminary Design Review

05 – 06 NOV 2013

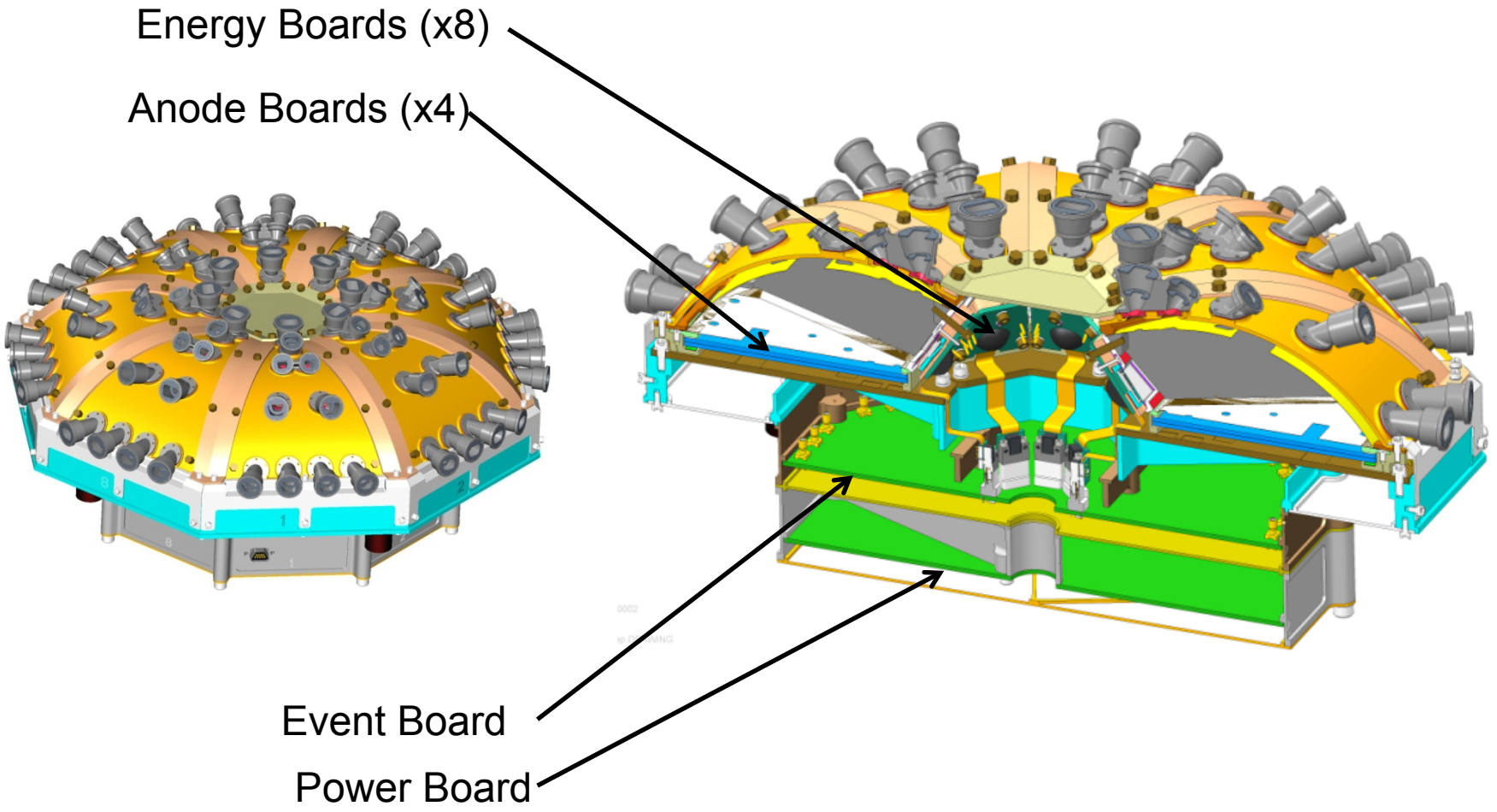
ISIS Power

David Do

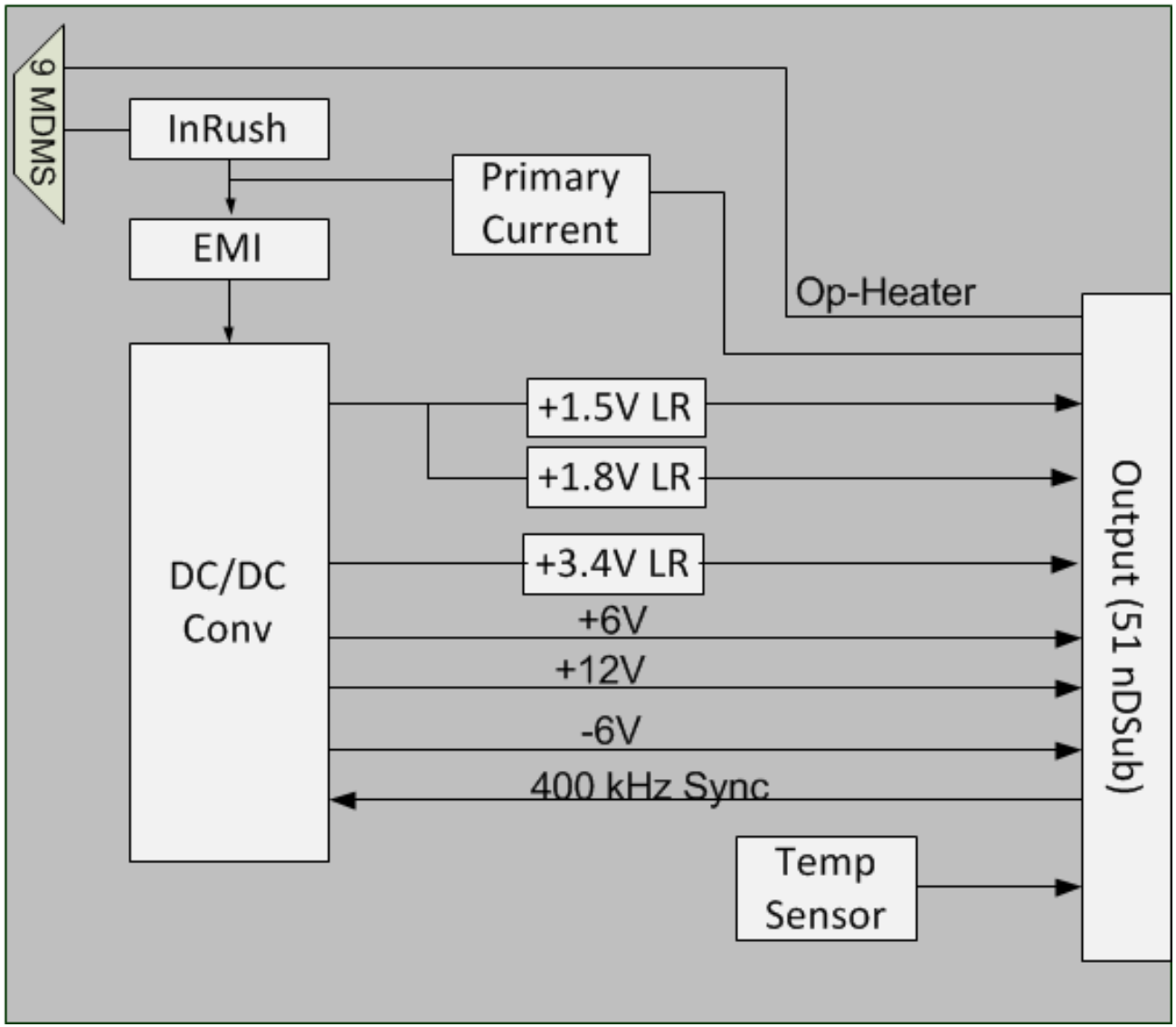
EPI-Hi Electronics Overview



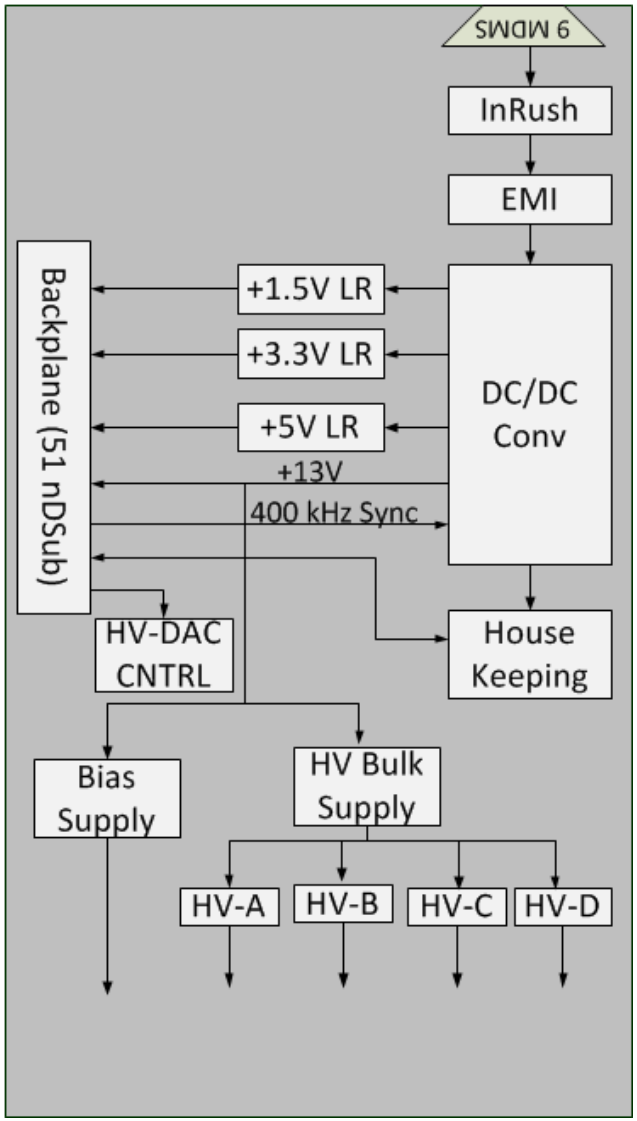
EPI-Lo Electronics Overview



EPI-Hi Block Diagram



EPI-Lo Block Diagram



Environment Requirements

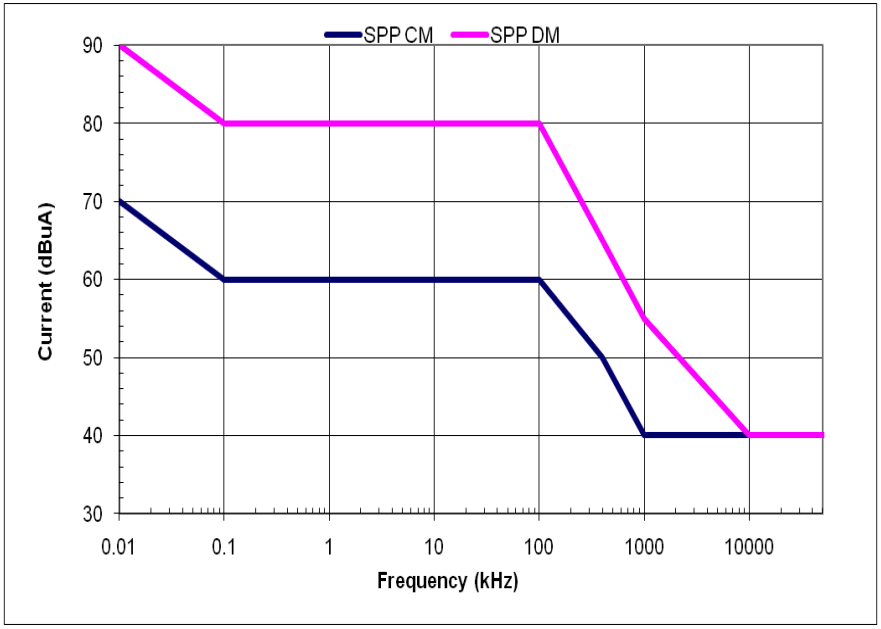
- Thermal
  - Survival is -55°C to +85°C
  - Operational is -35°C to +65°C
- Radiation
  - 25 krad (includes RDM=2 from FASTrad analysis)
  - LET > 80 MeV*cm2/mg

LVPS Major Input Requirements

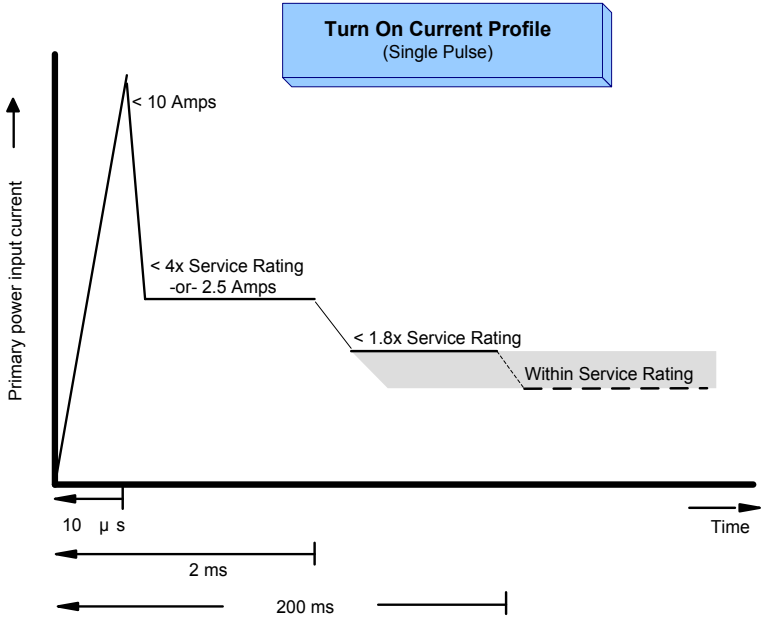
- Requirements from Solar Probe Bus
- Input Specification
  - Operate over bus voltage of 22 to 35V
  - Survive any standing or fluctuating voltage from 0 to 40V
  - Meet EMI/EMC
  - Transformer and power inductor far away from wall
  - Power supplies crystal controlled to a frequency window centered at n*50 kHz with n>=3 and 500 ppm wide over all operating conditions and time.
  - Inrush current limit
  - Primary Secondary isolation >1MOhm
  - Overall efficiency > 70%

Input Power Requirement

- EMI/EMC
- Inrush Current



CE01& CE03 Limit



In-Rush Current Limit

Interface

- EPI-Hi
  - Input connector: MWDM2L-9SCBRR2-.110-429
  - Output connector: 891-008-51PSBRT1T-429TH

- EPI-Lo
  - Input connector: MWDM_L-9SSMR
  - Inter board connector: 891-008-51PSBRT1T-429
  - Safing connector: 803-005-07M5-3EN
  - Bias voltage connector: 09-9001-1
  - High voltage: Pig tails

Power Topology

- Common for EPI-Hi and EPI-Lo:
  - Main converter is forward with resonant reset operating at 200kHz. Efficiency is >80%.
  - Digital voltages are linear regulated

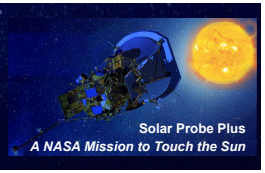
- EPI-Lo HVPS:
  - Bulk high voltage is set at 3.4kV
  - High voltages of up to 3.3kV are controlled through Opto-couplers
  - Bias voltage is up to 200V

Output Requirements

- EPI-Hi:
  - Generate low voltages: +12V, +6V, +3.3V, +1.8V, +1.5V & -6V
  - Primary input current telemetry
  - Temp sensor
  - Provide path for Op-heater voltage

- EPI-Lo:
  - Generate low voltages: +13V, +5V, +3.3V and +1.5V
  - House keeping through ADC for primary input current, temperature, output currents and output voltages
  - Generate high voltages and bias voltages to sensors
  - Hard and soft high voltage safing

EPI-Hi Output Requirements

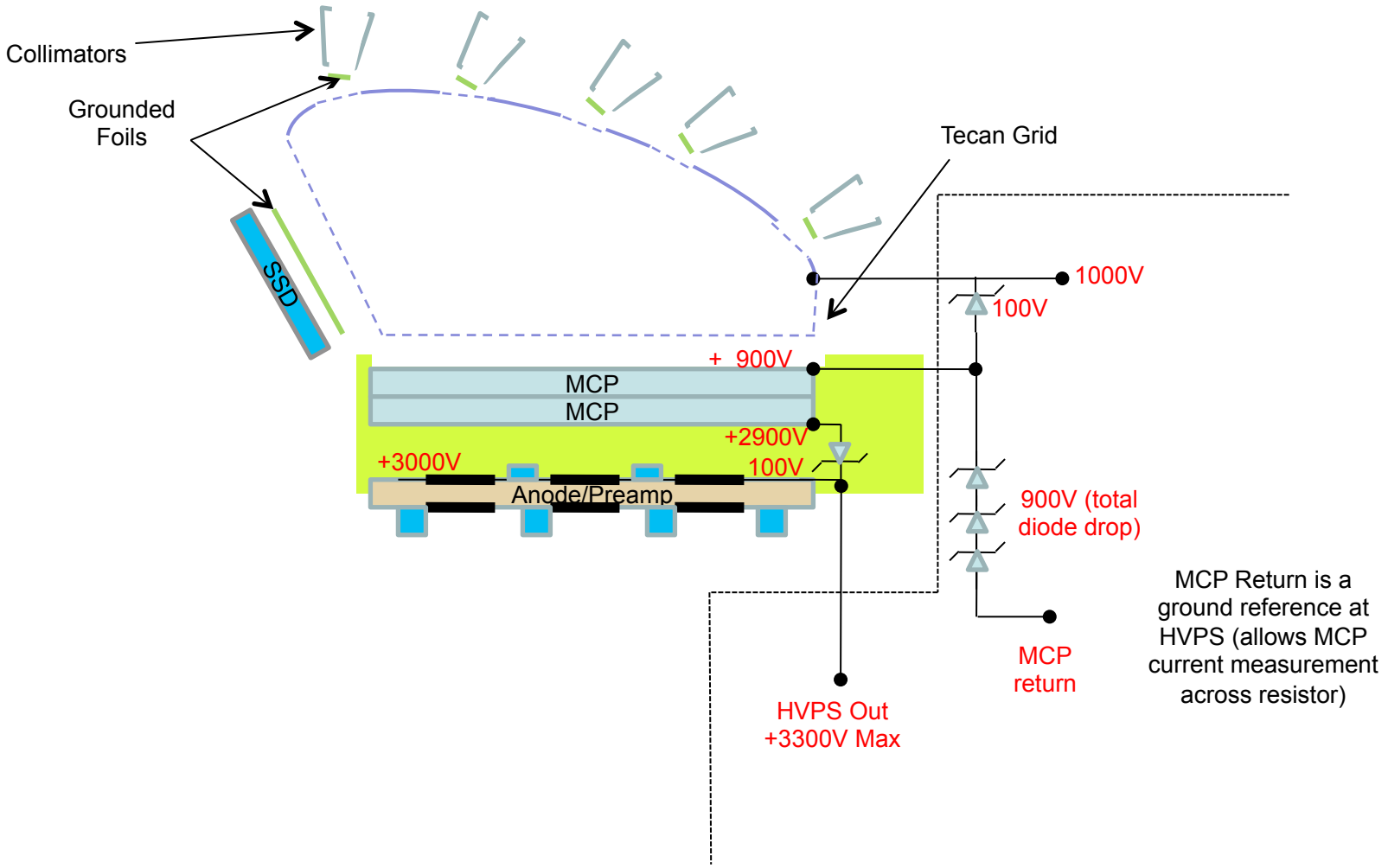


	Output Regulation	Min Load (mA)	Nom Load (mA)	Max Load (mA)
+1.53V	±2.5%	50	100	150
+1.82V	±2.5%	20	40	60
+3.41V	±2.5%	145	287	430
+6V	±7%	79	338	500
+12V	±7%	8	16	64
-6V	±5%	6	12.6	19

EPI-Lo Output Requirement

	Outputs Regulation	Min Load (mA)	Nom Load (mA)	Max Load (mA)
+1.5V	±3%	45	80	200
+3.3V	±3%	150	200	460
+5V	±5%	115	135	160
+13V	±5%	10	63	90

Sensor Voltages



EPI-Lo HVPS Requirements

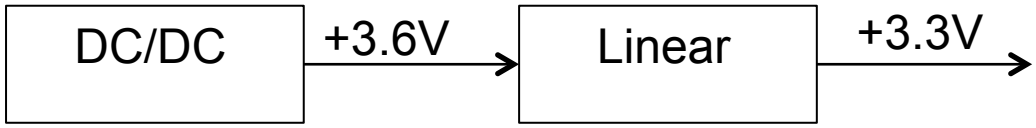
	Max Output Voltage (V)	Min Load (uA)	Max Load (uA)
Bias	200	0	20
Bulk	3400	0	250
HVPS	3300	0	50
Grid	1000	0	1
MCP	900	0	50

HVPS Current Limit

- Control range: 0uA to 200uA
- Control granularity: <1uA
- Response time: <1ms
- LVPS sends over-current signal to event board
- Event board turns off high voltage output and resets DAC

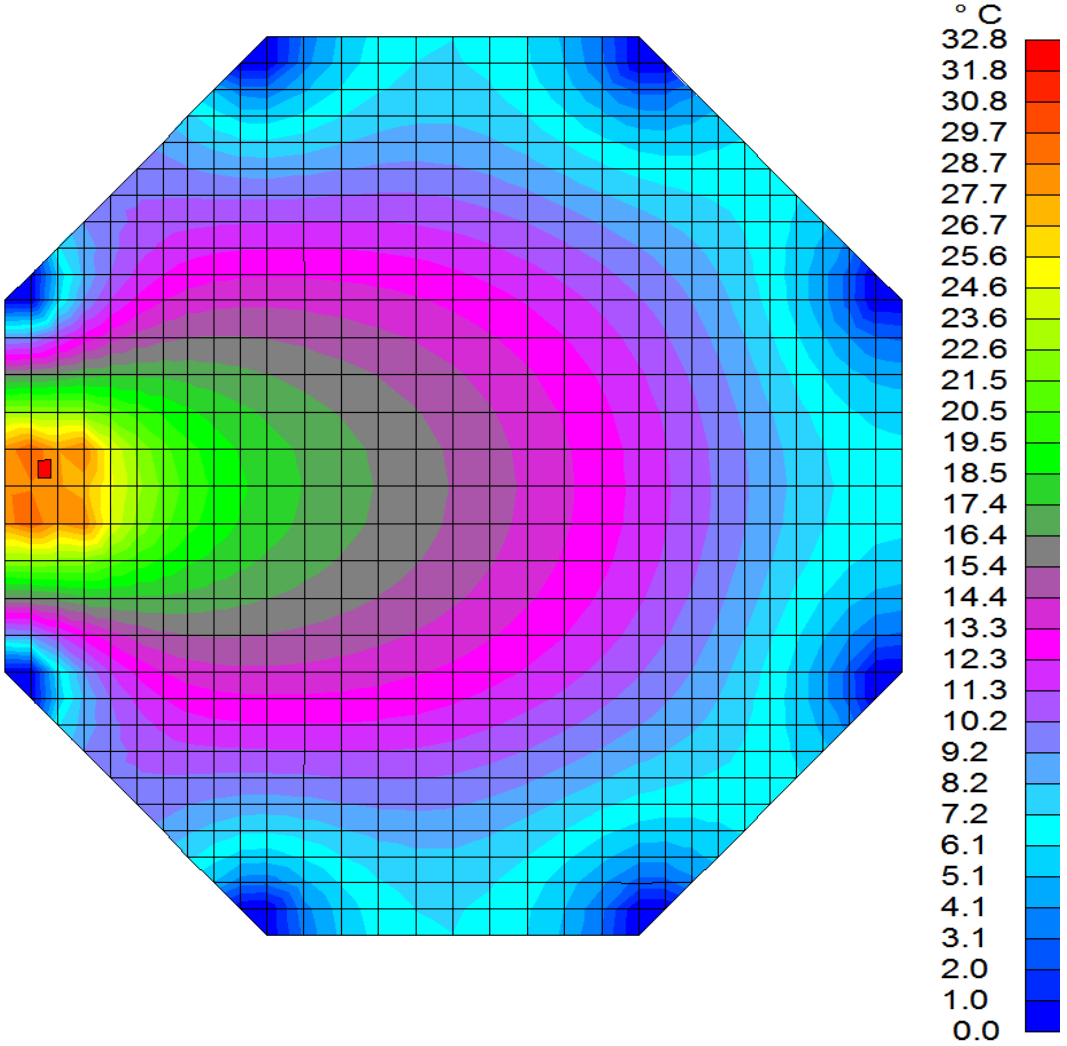
LVDS Fault Mitigation

- Transformer: primary and +3.3V winding is well isolated by +13V and +6V windings
- +3.3V is linear regulated from +3.6V
- Linear pass transistor is rated for 100V
- Worse case fault LVPS goes to full duty cycle which results in +7.5V output on +3.6V
- Preliminary thermal analysis shows 33°C rise in linear regulator

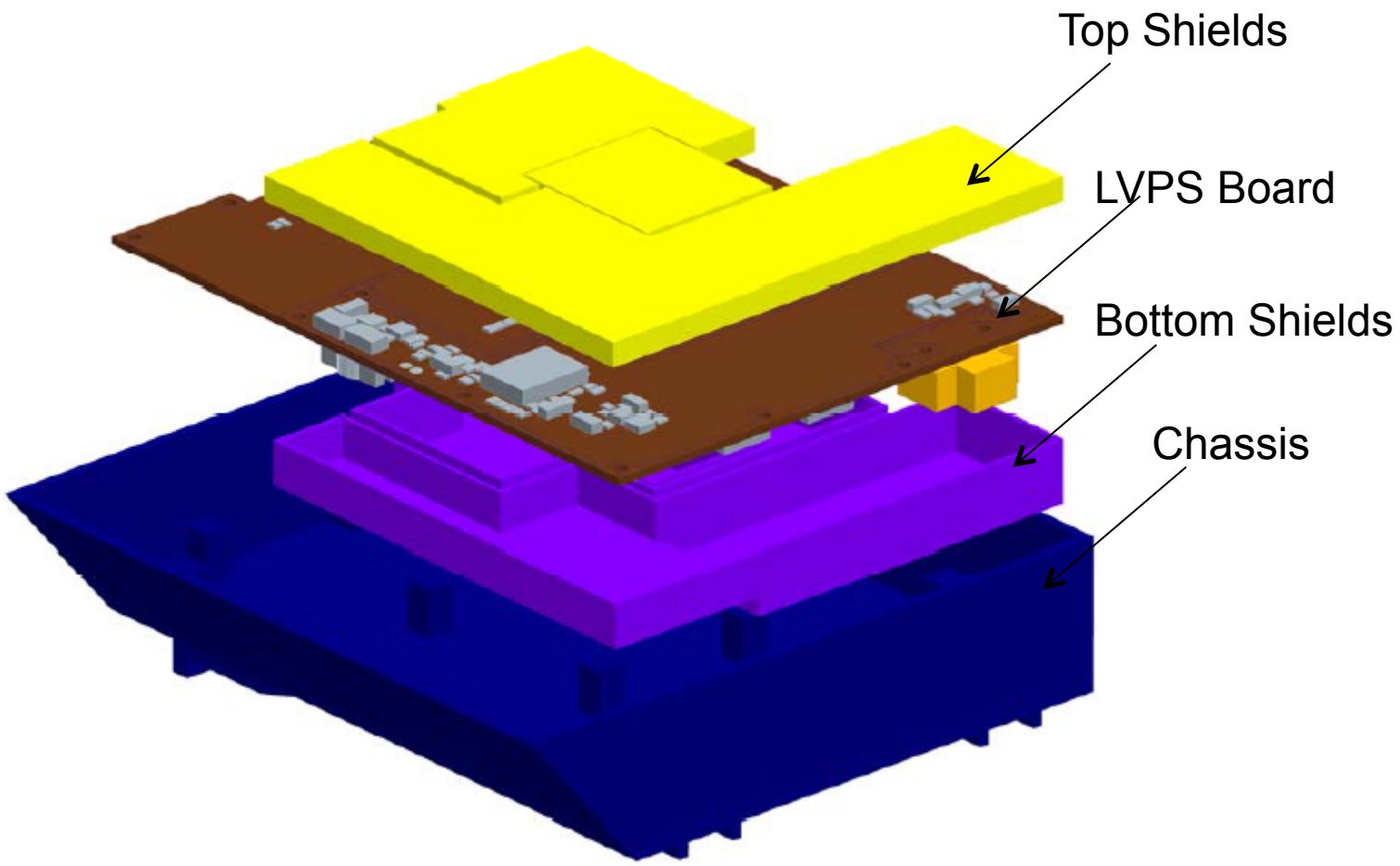


Worst Case Thermal Analysis

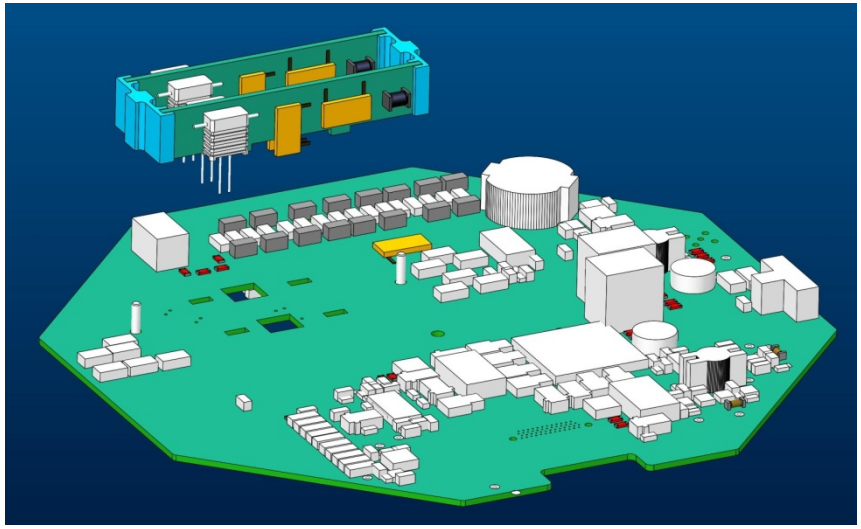
- 6oz Cu in PWB
- Thermal contours plot shown with 8W total power dissipation
- Actual power dissipation <2.5W
- TO-254 temps for 6oz
  - Junction = 32.8°C
  - Case = 13.2°C



EPI-Hi Package



EPI-Lo Packaging

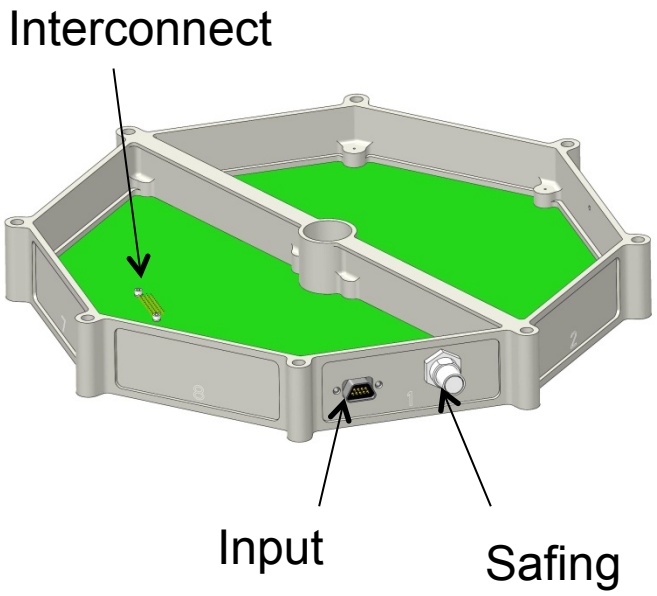


Packaged in octagon frame

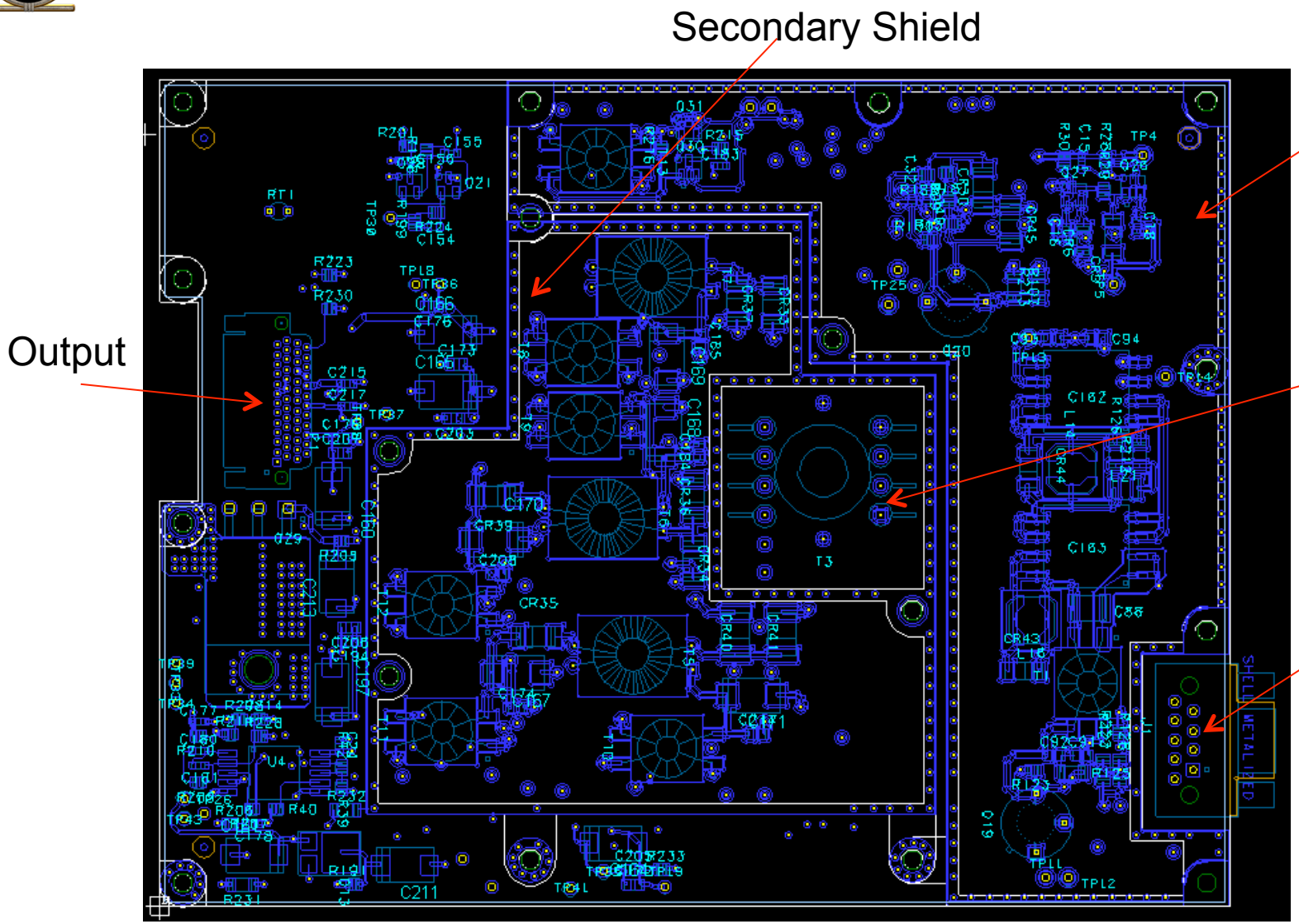
2 daughter boards for high voltages

Stiffener goes across the board

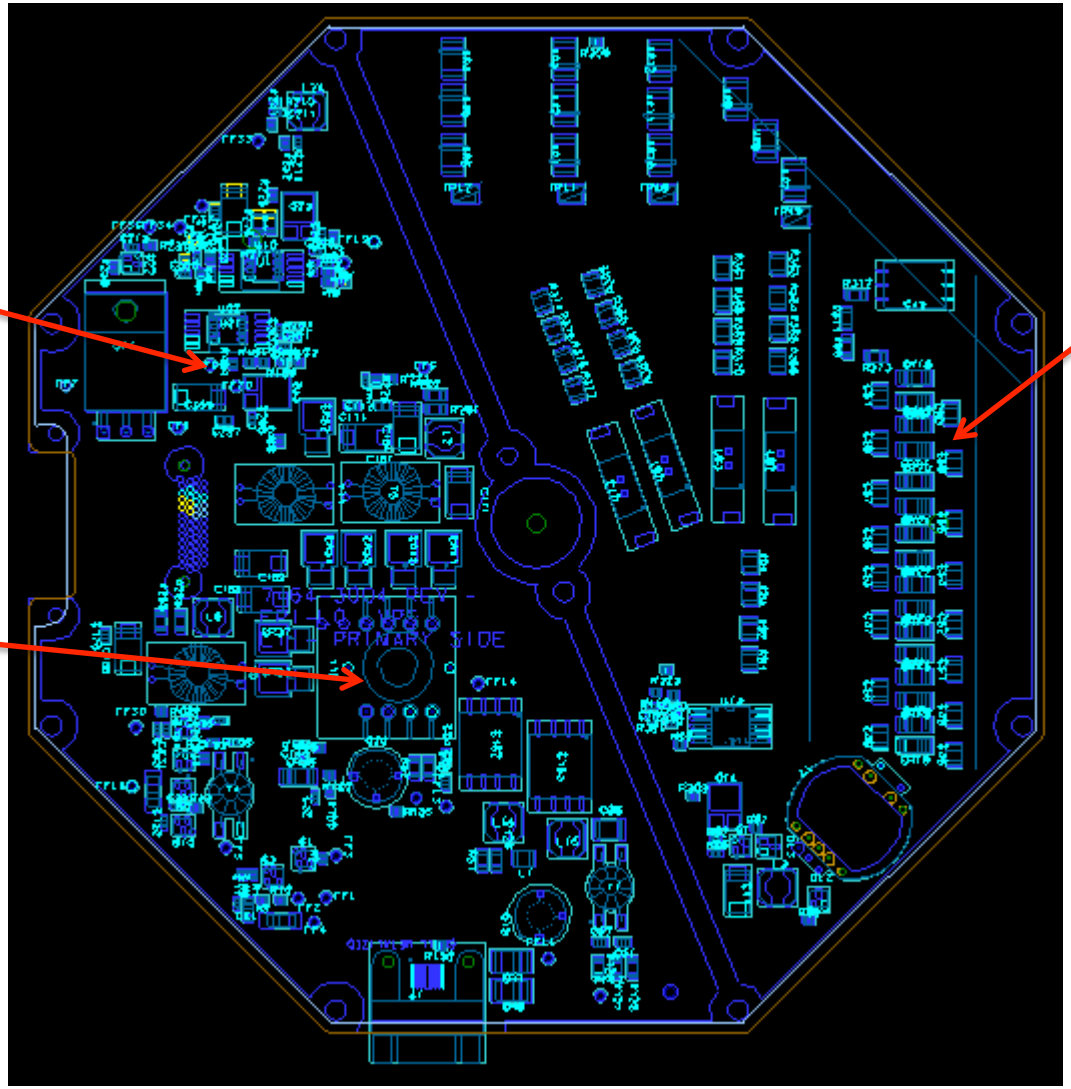
Power dissipation is estimated <2.5W



EPI-Hi Board Layout



EPI-Lo Board Placement



Nominal Output Regulation and Efficiency

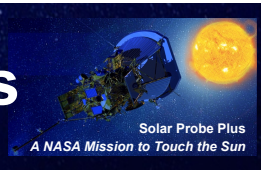
	Load(A)	Regulation(V)	Power(W)
+1.53V	0.14	1.505	0.2107
+3.41V	0.287	3.69*	0.9758
+6V	0.338	5.97	2.01786
+12V	0.016	11.98	0.19168
-6V	0.012	5.95	0.0714
input	0.159	28	4.452
			78%

- *+3.41V shown pre-regulated. Efficiency is calculated using +3.4V.
- +3.41V and +1.82V linear regulator have same design as +1.53V.

Analysis

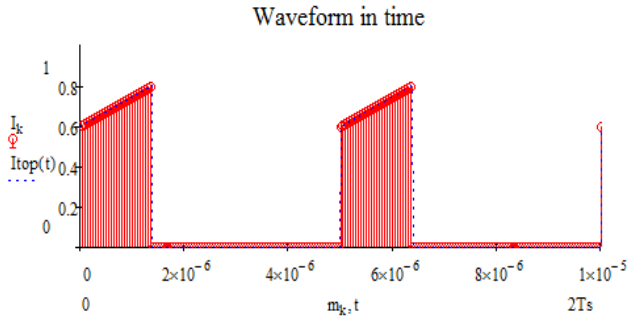
- Preliminary EMI completed
- WCA for digital voltages regulation = ±2.3%

Voltage Regulation WCA Method and Assumptions

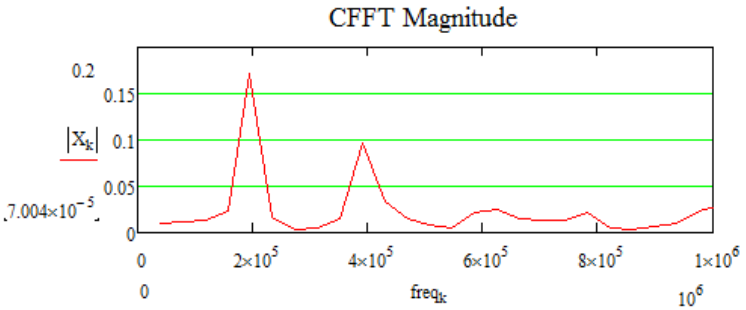


- WCA Method
  - Extreme Value Analysis in Mathcad
- Temperature Range
  - -35C to +65C operational
- Resistors Variation
  - K resistors are 100 ppm (0.8%) + 1% initial tolerance + 2% Aging ≈ 4%
  - E resistors are 25 ppm (0.2%) + 0.1% initial tolerance + 1% Aging ≈ 1.3%
  - Z resistor are 5ppm(0.04%)+ 0.01% initial tolerance 0.16% Aging ≈ 0.2%
- RH1078
  - 100Krad data from datasheet
- PWM5302S
  - 100Krad data from datasheet

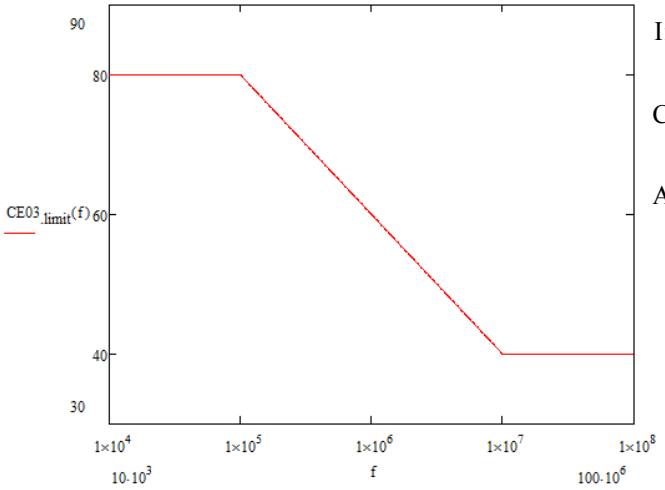
EPI-Lo EMI Analysis



Primary Current in Discrete Time



Primary Current in CFFT

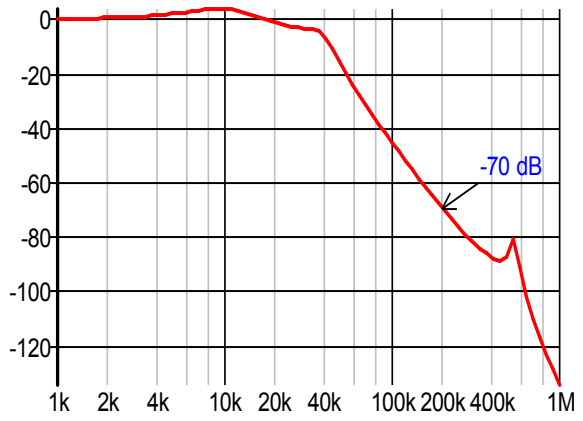


$$Iin_{dB} := 20\log\left(\frac{peak}{\mu A}\right) = 104.725$$

$$CE03_{limit}(200kHz) = 73.979$$

$$Aten := Iin_{dB} - CE03_{limit}\left(\frac{1}{Ts}\right) = 30.746$$

CE03 Limit



EMI Filter Attenuation

Parts

- All parts are rad-hard to >100krad
- Parts submitted to PCB. No issues expected.

Part Number	Description	Manufacture
PWM3052S	PWM IC	Aeroflex
ADC128S102QML	12 Bit-ADC	TI
RH1009MW	2.5V Reference	Linear Tech
RH1078MW	Low power Opamp	Linear Tech
M49470X01335KBB	Stacked 3.3uF Ceramic	Presidio
IRHNM57110	100V N Channel FET	IR
JANSR1N5811US	100V Schottky Diode	Microsemi
JANSR2N2222AUB	NPN transistor	Microsemi
JANSR2N3501UB	NPN transistor	Microsemi
66353	High voltage opto	Micropac
ADCMP600	Comparator	Analog Devices

Plans for Testing

- Follows APL Manufacturing Flow, these are significant highlights
  - Populate Passive Components with Automatic Measurement.
  - Populate Actives and Install Known Tailors or Tailor Flags
  - Install into Flight Frame
  - Execute Test Procedure to Test and Tailor Entire Board
  - ESS Testing
  - Execute Functional Test Procedure
  - Photograph and Conformal Coat
  - Execute Test Procedure to Calibrate and Characterize Board (over temperature)
  - Release to Next Assembly

Status Summary

- EPI-Hi
  - EM PWB is being fabricated
- EPI-Lo
  - EM is in placement & layout phase

Plan Forward

- EPI-Hi
  - Complete testing EM
  - Fabricate flight
- EPI-Lo
  - Fabricate and complete testing EM
  - Fabricate flight
- Finalize all documentation and procedures for flight build
- Build, tailor, calibrate, and qualify flight units

Peer Reviews

- EPI-Hi LVPS: May 2013, 27AI all closed SRI-13-026
- EPI-Lo Power: Aug 2013, 5 AI all closed SRI-13-029
- Major Action Items:
  - EPI-Hi:
    - Shielding over switching circuits
    - Output loads
    - Output regulations
  - EPI-Lo:
    - MCP voltage accuracy
    - LVDS fault mitigation
    - Bias Voltage Zener diode protection