Solar Probe Plus

A NASA Mission to Touch the Sun

Integrated Science Investigation of the Sun
Energetic Particles

Preliminary Design Review

05 – 06 NOV 2013

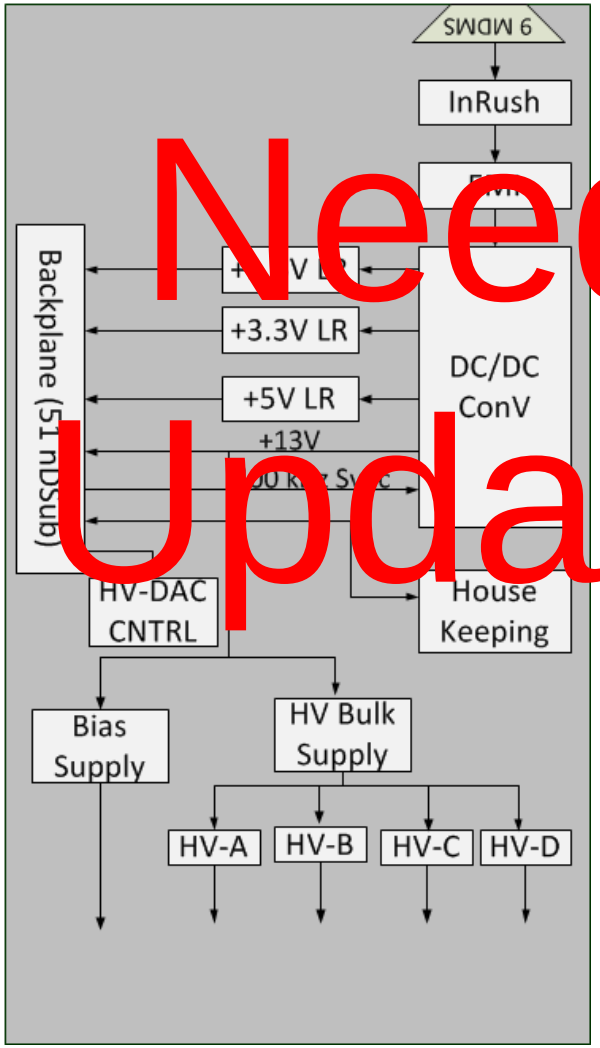
ISIS Power

David Do

Outline

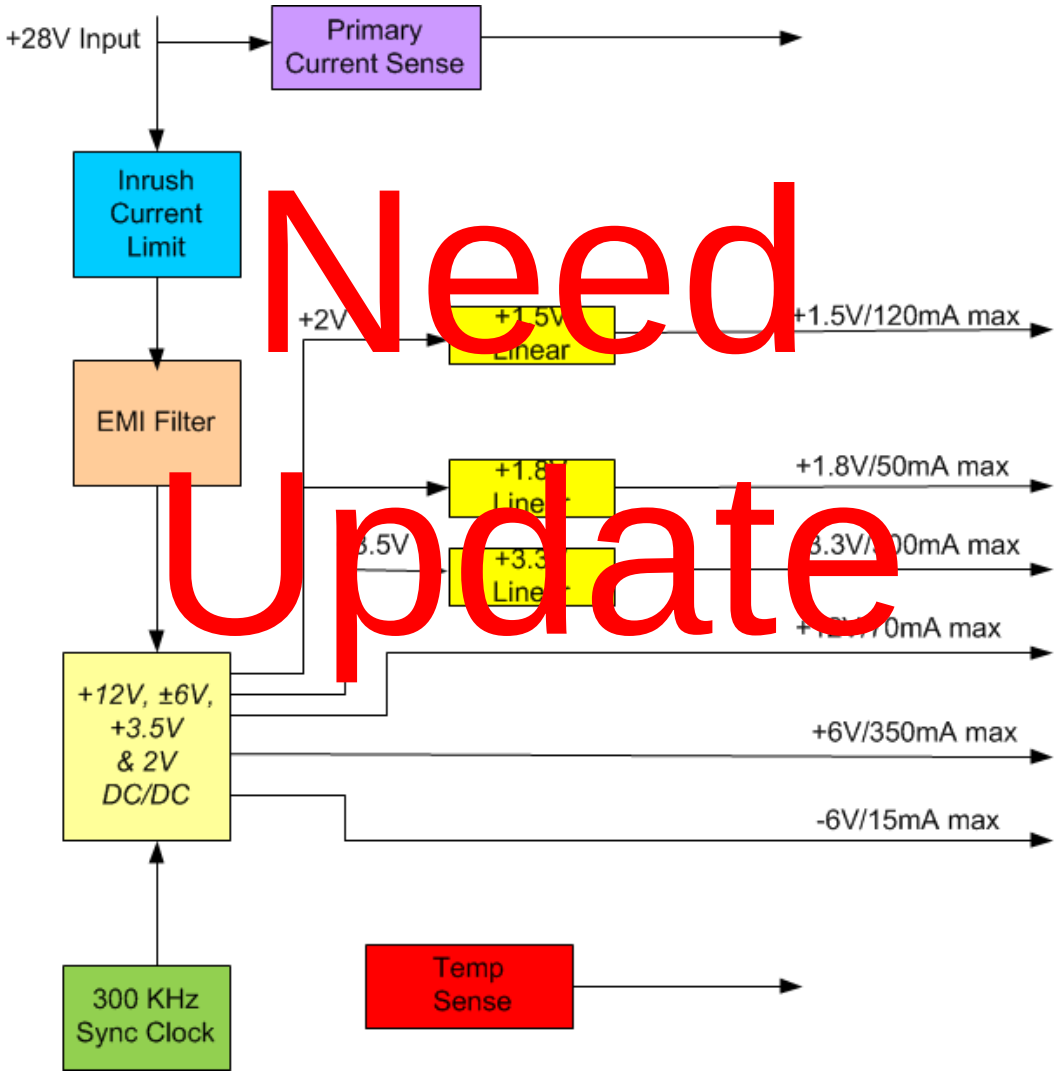
- EPI-Lo and EPI-Hi LVPS
  - Power requirements
  - Block diagrams
  - Circuit topologies and descriptions
  - Circuit margins
  - Packaging
  - Thermal management
- Plans for testing including bench checkout equipment
- Maturity of the design (BB testing, design, analysis completed)
- Preliminary parts lists and any special testing required
- Summary and follow-up from peer review held prior to the instrument PDR

Block Diagram



Need Update

EPI-Hi Block Diagram

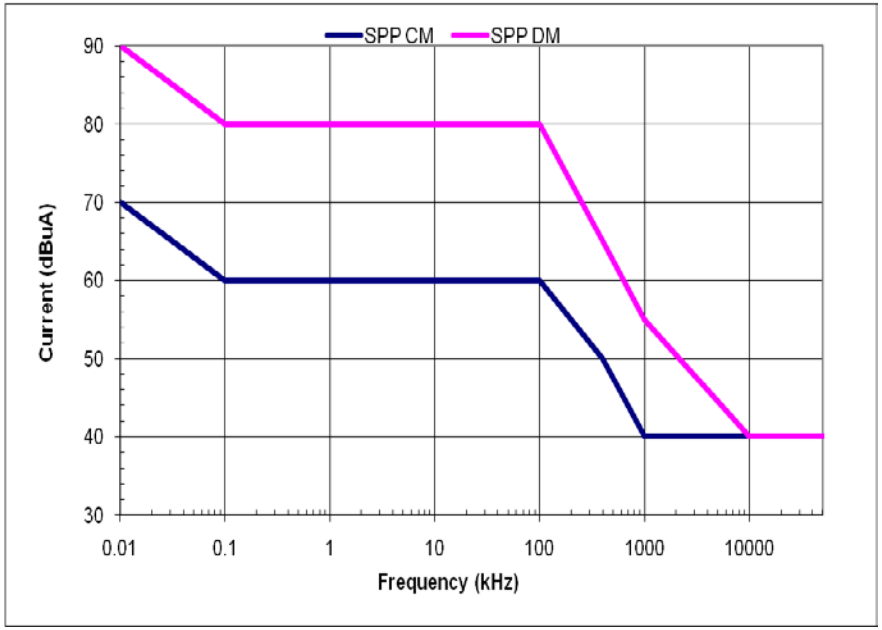


Environment

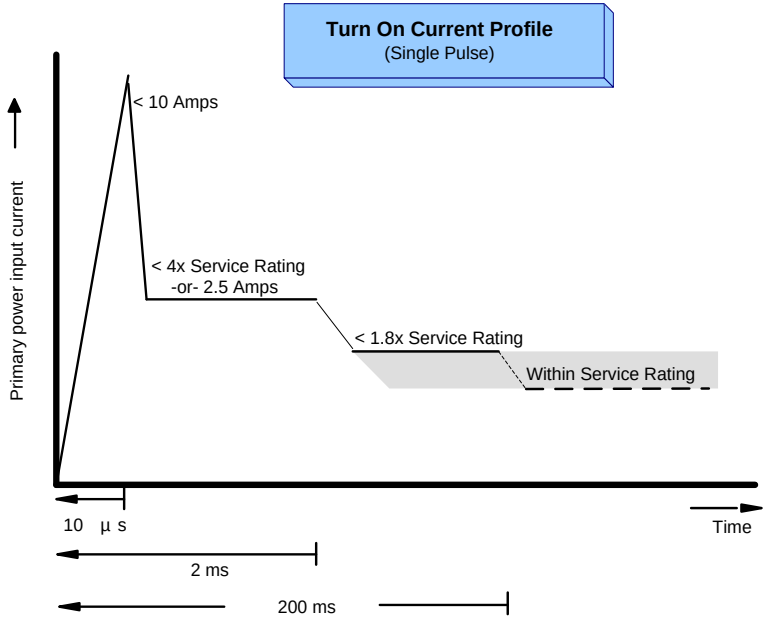
- Operating Temp: -30°C to +60°C
- Radiation: 100Krad, 82MeV

Input Power Requirement

- Input voltage: 24V- 35V, 28V nominal
- 1Mohm isolation minimum
- EMI/EMC
- Inrush Current

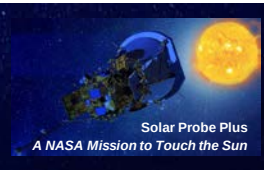


CE01& CE03 Limit



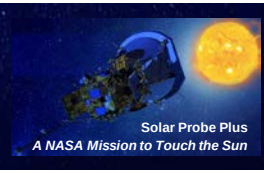
In-Rush Current Limit

Power Topology



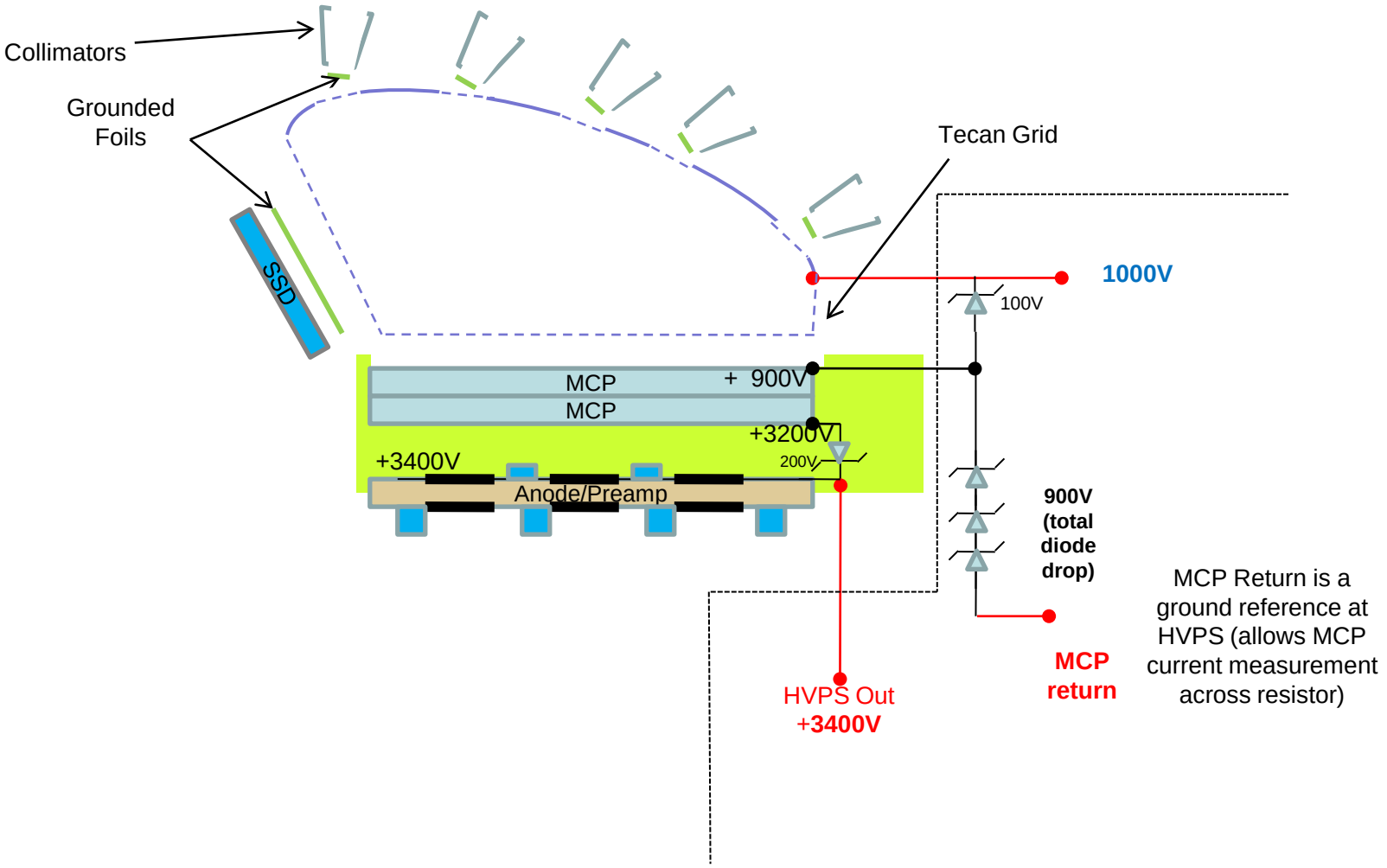
- Main converter is forward with resonant reset operating at 200kHz. Efficiency is >80%.
- Digital voltages are linear regulated
- Bulk high voltage is set at 3.5kV
- High voltages of up to 3.4kV are controlled through Optocouplers

EPI-Lo Output Requirement



	Outputs Regulation	Min Load (mA)	Nom Load (mA)	Max Load (mA)
+1.5V	±3%	45	80	200
+3.3V	±3%	150	200	460
+5V	±5%	115	135	160
+13V	±5%	10	63	90

Sensor Voltages



EPI-Lo HVPS

	Max Output Voltage (V)	Min Load (uA)	Max Load (uA)
Bias	200	0	20
Bulk	3500	0	200
HVPS	3400	0	40
Grid	1000	0	1
MCP	900	0	40

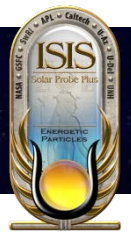
EPI-Hi Output Requirements

	Output Regulation	Min Load (mA)	Nom Load (mA)	Max Load (mA)
+1.5V	±2.5%	50	100	150
+1.8V	±2.5%	20	40	60
+3.3V	±2.5%	145	287	430
+6V	±5%	79	338	500
+12V	±7%	8	16	64
-6V	±7%	6	12.6	19

Thermal Analysis

LVDS Fault Mitigation

- Transformer: primary and 3.3V winding is well isolated
- +3.3V is linear regulated from +3.5V
- +3.5V is monitored on housekeeping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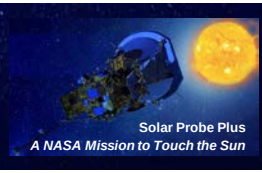
Packaging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Peer Reviews

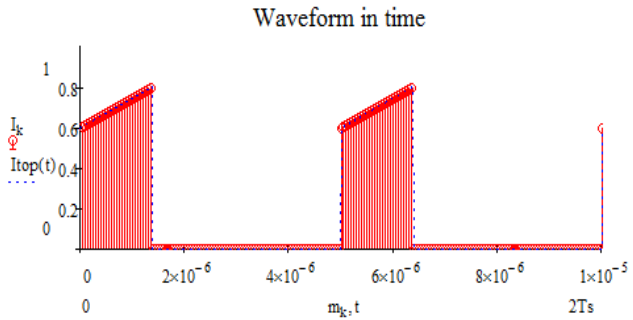
- EPI-Hi LVPS: May 2013
- EPI-Lo Power: Aug 2013
- Major Action Items:
  - EPI-Hi:
    - Shielding over switching circuits
    - Output Loads
    - Output Regulations
  - EPI-Lo:
    - MCP voltage accuracy
    - LVDS fault mitigation
    - Bias Voltage Zener diode protection

Breadboard Testings

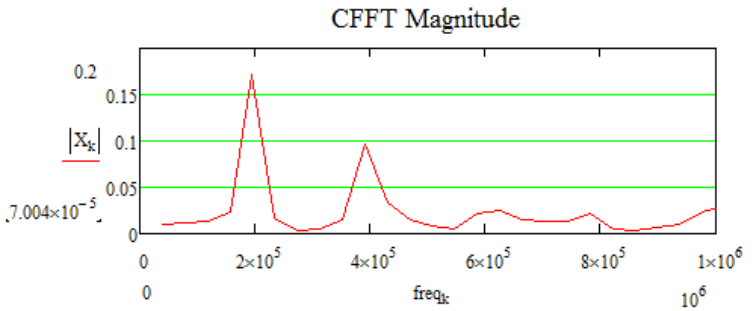
Analysis

- Preliminary EMI completed
- Worst Case analysis for digital voltages completed

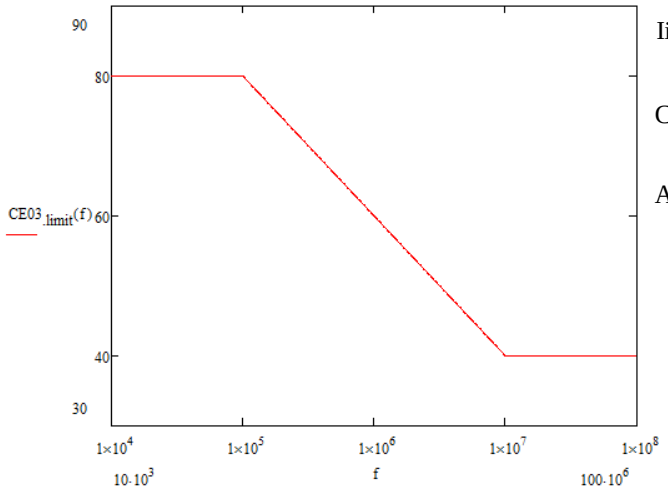
EPI-Lo EMI Analysis



Primary Current in Discrete Time



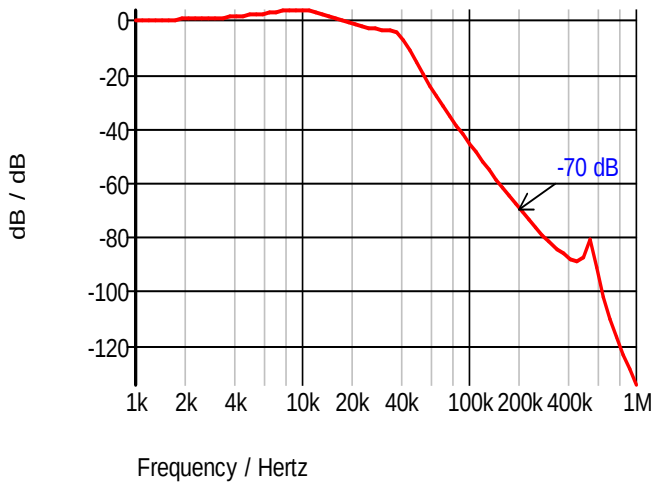
Primary Current in CFFT



$$Iin_{dB} := 20\log\left(\frac{peak}{\mu A}\right) = 104.725$$

$$CE03_{limit}(200kHz) = 73.979$$

$$Aten := Iin_{dB} - CE03_{limit}\left(\frac{1}{Ts}\right) = 30.746$$



CE03 Limit

EMI Filter Attenuation